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A Swift and Slim Flavour Tagger Exploiting the CMOS Sensor Technology

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CMOS sensors are being developed in Strasbourg and Saclay to equip a vertex detector offering the performances required for the ILC physics programme. An overview of the demonstrated sensor performances and on-going activities is provided. Basic parameters of a detector exploiting the features of CMOS sensors are also presented. They account for an improved estimate of the beamstrahlung electron rate, which governs the sensor read-out speed and radiation tolerance requirements.

1. INTRODUCTION

The ILC physics programme is driving an important R&D effort on CMOS sensors in Strasbourg since 1999 [1]. The development is motivated by the perspective of an attractive trade-off between granularity, material budget, read-out speed, radiation tolerance and power dissipation.The sensors are manufactured in standard CMOS technology, offering low fabrication costs and fast turn-over for their development. Moreover, they allow integrating signal processing micro-circuits (e.g. pedestal subtraction, analog to digital conversion, sparsification) on the detector substrate.

The key element of this novel technology is the use of an n-well/p-epi diode to collect, through thermal diffusion, the charge generated by the impinging particle in the thin (typically 5 - 15 μm) epitaxial layer underneath the read-out electronics [1]. The sensor tracking performances are now well established [2]. This report concentrates on performances obtained recently with a new manufacturing process, on the progress made with the design of fast signal processing architectures, on recent achievements in industrial thinning procedures and on the concept of a vertex detector design taking best advantage of the CMOS sensor peculiarities.

2. ESTABLISHED TRACKING PERFORMANCES

The capability of developing high performance CMOS sensors depends on basic manufacturing parameters, such as the epitaxial layer thickness, which may vary substantially from one fabrication process to another. Exploring fabrication processes is therefore of prime importance.

11 different MIMOSA prototypes were designed and fabricated in 6 different sub-micron manufacturing processes from 1999 to Spring 2005. The founder AMS proposed a new fabrication process in 2004, offering a 0.35 μm feature size and a $\sim$ 10 μm thick epitaxial layer. Moreover, the process is optimised for CMOS imaging applications, and offers therefore a reduced leakage current. The prototype MIMOSA-9 was designed and fabricated to characterise this process. It is made of several sub-arrays, each exhibiting a different sensing diode (3.4×4.3, 5×5 or 6×6 μm^2) or pitch size (20, 30 or 40 μm).

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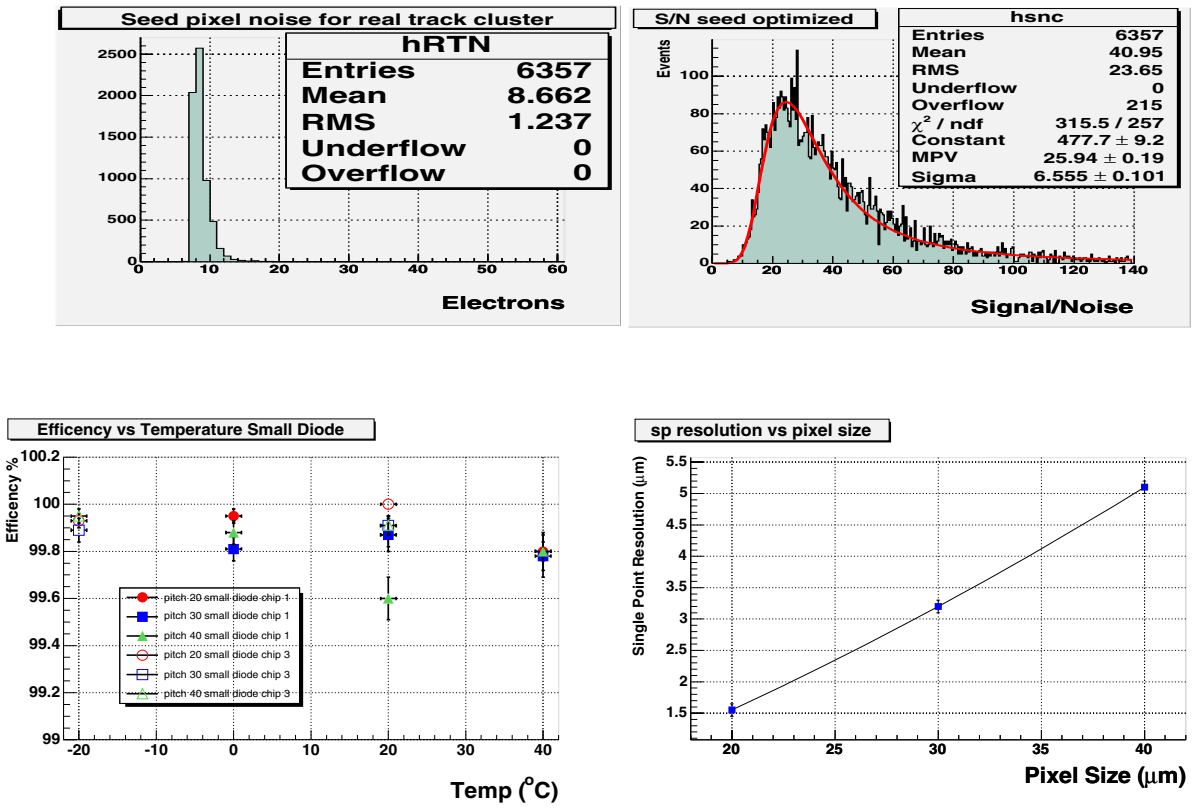

Figure 1: MIMOSA-9 beam tests results. The top distributions show the residual noise after CDS (left) and the signal-to-noise ratio (right) at 0°C for pixels of 20 μm pitch, equipped with a 3.4x4.3 μm^2 diode. The bottom of the figure displays the temperature dependence of the detection efficiency for various pixel pitches and for two different chips (left), as well as the single point resolution as a function of the pixel pitch (right).

Several prototypes were exposed to a $\sim$ 120 GeV/c pion beam at the CERN SPS. Excellent performances were observed [3], as illustrated by Fig. 1. The signal-to-noise most probable value ranges from $\sim$ 15 to $\sim$ 30, depending on the diode size, pixel pitch and operating temperature. This rather comfortable magnitude translates into a detection efficiency exceeding 99.5 %, even in the case of a pitch as large as 40 μm, where charge collection inefficiencies may appear as a consequence of the sizeable path achieved by some charge carriers until the sensing diode. The single point resolution was found to vary from $\sim$ 1.5 μm for a 20 μm pitch to $\sim$ 5 μm for a 40 μm pitch. These results allow to foresee a variable pitch for the vertex detector, ranging from 20 μm for the inner most layer to $\lesssim$ 40 μm for the outer layer, which translates into a reduced data flow and power dissipation.

The tolerance of the prototype to $\sim$ 1 MeV neutrons and to $\sim$ 9 MeV electrons was investigated. Its detection efficiency of the sensors was observed to remain above 99% for a fluence of $10^{12} \mathrm{n}_{eq}/\mathrm{cm}^2$ (i.e. at least two orders of magnitude more than the expected annual fluence), as well as for an integrated dose of $10^{13} \mathrm{e}^-_{9MeV}/\mathrm{cm}^2$ (corresponding to more than 5 years of irradiation with beamstrahlung electrons in the detector inner most layer, as shown in the next section). It is thus quiet reliably established that the sensors can cope with the expected ILC radiation conditions, even if the doses come out to be much higher than the present Monte-Carlo predictions. The validity of this statement may however depend on the operating temperature of the sensor, which should eventually be kept $\lesssim$ 0°C.

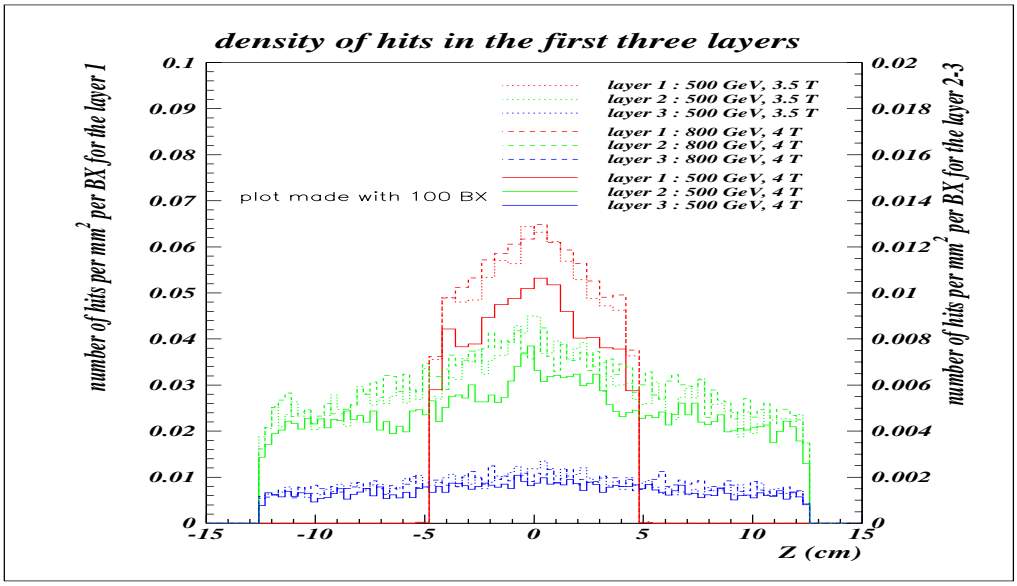

Figure 2: Distribution of beamstrahlung hits in the three inner layers of the vertex detector along the direction parallel to the beam axes. The left vertical scale applies to the inner most layer (red lines), while the right scale stands for the two other layers (green and blue lines). The rates are shown for two different values of the experimental magnetic field (4 and 3.5 T) and of the collision energy (500 and 800 GeV).

3. IMPROVED ASSESSMENT OF RUNNING CONDITIONS

3.1. Improved Beamstrahlung electron rate estimate

The rate of beamstrahlung electrons traversing each detector layer was determined with improved statistical accuracy w.r.t. the TESLA TDR [4] in order to refine the constraints on the read-out speed (due to occupancy) and on the radiation tolerance to electrons. The computation was performed with the GUINEA-PIG simulation, based on 100 bunch-crossings (BX). The hit distribution along the beam directions (z axis) is shown in Fig.2 for the 3 inner layers of the detector, located at radii of 15, 26 and 37 mm. The figure also illustrates how the hit rate varies when modifying the magnetic field from 4 to 3.5 T and the collision energy from 500 to 800 GeV.

The hit density in the inner most layer varies from about 3 hits/cm^2/BX at the acceptance edges to more than 5 hits/cm^2/BX near the vertical to the interaction point. This sizeable difference is due to $\sim$ 10 MeV electrons produced close to 90° and traversing a large number of times ($>$ 10) the inner most layer while they spirale in the 4 T magnetic field of the apparatus. The momenta of beamstrahlung electrons reaching the detector concentrate near 9-10 MeV/c. The hit rate decreases therefore rapidly with increasing radius: it is $\sim$ 8 times smaller in the second layer and is still $\sim$ 3 times smaller in the third layer.

The rates shown in Fig.2 are subject to uncertainties (process generation, etc.) or unknowns which need to be taken into account when deriving constraints on the vertex detector performances. A global safety factor of 3 was applied to the raw Monte-Carlo output for this purpose. The hit density for which the vertex detector should still be fully operational was therefore fixed to 15 hits/cm^2/BX.

3.2. Consequences on the signal processing electronics and the radiation tolerance

The read-out time of the inner most layer was fixed to a target value of $\lesssim 25\ \mu s$, i.e. at least twice shorter than stated in the TESLA TDR. This value is still not comfortable (an occupancy of several per-cent is not excluded), but reflects a compromise which accounts for power dissipation, material budget and detector design considerations. In

order to enhance the capability to afford a high beamstrahlung rate, the read-out time of the outer layers was chosen short enough to keep the occupancy at a low level. A clean track reconstruction can then be performed in these layers; their extrapolation to the inner most layer allows to select the hits of interest on the basis of their matching with the extrapolated impacts. While reading the 3 outer layers in $\lesssim 200\ \mu s$ suits this objective, the second layer needs to be read out in much shorter time (typically $\sim 50\ \mu s$).

The hit rate in the inner most layer translates into an upper limit of $\sim 1.8{\cdot}10^{12}$ hits/cm^2/yr near 90°. Imposing the sensors to keep satisfactory performances after 3 years of operation, translates into a radiation tolerance requirement of $\sim$ 150 kRad. Moreover, assuming a NIEL factor of 30 for 10 MeV electrons, the expected fluence is $\lesssim 2{\cdot}10^{11}$ n_{eq}/cm^2. This value is significantly larger than the predicted fluence induced by the neutron gas circulating inside the experimental apparatus ($\lesssim 10^{10}$ n_{eq}/cm^2/yr [1]).

4. R&D ON SIGNAL PROCESSING ARCHITECTURES

A signal processing micro-circuit is being designed, which provides the short read-out time required for the two inner most layers. It relies on a massively parallel architecture with on-chip data sparsification. For the outer layers, a much less demanding architecture is being developed: it offers on-pixel storage for $\gtrsim 5$ snapshots during a single bunch train crossing, the signal transfer and processing being postponed to the end of the bunch train. This design is unlikely to be applicable to the inner layers because the number of memory-cells to integrate in each pixel ($\gtrsim 40$ in the inner most layer) would require too small, i.e. inaccurate, capacitors.

4.1. Inner layer architecture

Several prototypes were fabricated since 2002. They feature pedestal subtraction inside each pixel (via correlated double-sampling, i.e. CDS), the latter being grouped in short columns read out in parallel. Each column is equipped with a single discriminator handling the signals coming out sequentially from all pixels of the column. The most recent prototype of this type (called MIMOSA-8 [5]) has shown encouraging performances. Manufactured in TSMC-0.25 μm technology, it features in-pixel amplification and CDS, and is organised in 4 sub-arrays of 32 columns read out in parallel. 24 columns are ended with a discriminator. Preliminary tests of the chip show a pixel noise of $\sim$ 13-18 e$^-$ENC and a charge-to-voltage conversion gain of $\sim$ 50-110 $\mu V/e^-$, depending on the architecture variant considered. Moreover, the pixel-to-pixel dispersion comes out to be particularly low ($<$ 10 e$^-$ENC) .

The simultaneous operation of all analog and digital elements is currently being tested. An improved version of this promising architecture is already under study, where each discriminator is replaced by a 4-bit ADC.

4.2. Outer layer architecture

A prototype (called MIMOSA-12) adapted to the outer layers was designed and sent for fabrication by the end of March 2005. It features 4 capacitors inside each pixel (35 μm pitch). The sensor includes 6 different sub-arrays exploring various MOS capacitors (50, 100 and 200 fF). One of the design goals consists in finding the smallest possible capacitors still providing a satisfactory precision in order to integrate the largest possible number of them in each pixel.

[1] This value includes a safety factor of 10 applied to the output of the Monte-Carlo simulation.

5. DETECTOR DESIGN STUDIES

A detector concept taking advantage of the CMOS sensor peculiarities was elaborated. It relies on a geometry similar to the one described in the TESLA TDR (based on CCDs), which assumes 5 cylindrical layers with a polar angle coverage extending to $|\cos\theta| \sim 0.90 - 0.95$.

Some of the prominent characteristics of the detector are summarised in Table I.

Table I: Prominent features of the detector concept based on CMOS sensors. For each layer, the table indicates the layer radius, the pixel pitch, the read-out time ($t_{r.o.}$), the ladder width (W_{lad}) and number (N_{lad}), the number of pixels (N_{pix}), as well as the instantaneous (P^{inst}_{diss}) and average (P^{mean}_{diss}) power dissipations. The average dissipation is based on a detector duty cycle of 5 %. The duty cycle of 1/200 usualy assumed would lead to a 10 times smaller value.

Layer	**Radius**	**Pitch**	$\mathbf{t}_{r.o.}$	$\mathbf{W}_{lad}$	$\mathbf{N}_{lad}$	$\mathbf{N}_{pix}$	$\mathbf{P}^{inst}_{diss}$	$\mathbf{P}^{mean}_{diss}$
L0	15 mm	20 μm	25 μs	7 mm	20	25 M	<100 W	<5 W
L1	25 mm	25 μm	50 μs	15 mm	26	65 M	<130 W	<7 W
L2	37 mm	30 μm	< 200 μs	24 mm	24	75 M	<100 W	<5 W
L3	48 mm	35 μm	< 200 μs	24 mm	32	70 M	<110 W	<6 W
L4	60 mm	40 μm	< 200 μs	24 mm	40	70 M	<125 W	<6 W
Total					142	305 M	<565 W	<29 W

The short read-out time in the inner layers is obtained by reading short columns perpendicular to the beam lines. Since all signal processing functionalities cannot be integrated inside the pixels, a narrow ($\sim$ 2 mm wide) side band is foreseen at the sensor edge, which hosts integrated mixed and digital micro-circuits. This is illustrated on Fig. 3, which displays a sketch view of a ladder equipping the inner most layer.

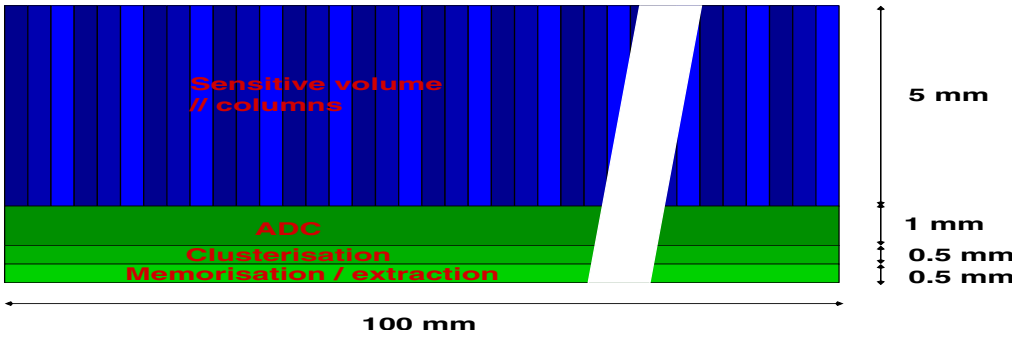

Figure 3: Sketch view of a ladder equipping the inner most layer.

The ladder width amounts to 7 mm, out of which 5 mm are equipped with 20 μm pitch pixels, while 2 mm are devoted to the digitisation, sparsification and signal transfer micro-circuits. Each column is made of 256 pixels. The latter contain all functionalities of the signal processing chain up to the CDS. Each pixel is read out at an effective clock frequency of $\sim$ 10 MHz, which translates into a column read-out time of $\sim$ 25 μs.

The second layer is equipped with pairs of 125 mm long ladders, stitched near the vertical to the interaction point. The ladder width amounts to 15 mm, shared between $\sim$ 13 mm long columns, perpendicular to the beam lines, and a 2 mm wide side band hosting the mixed and digital electronics. The columns are made of 512 pixels of 25 μm pitch, which translates into a ladder read-out time close to 50 μs.

The 3 other layers are also composed of pairs of 125 mm long ladders. They are $\sim$ 24 mm wide ($\sim$ reticle width). Each pixel is equipped with $\geq$ 5 memory cells, read out after the end of each bunch train. Each memory cell collects a charge integrated over < 200 μs. The pixel pitch is 30, 35 or 40 μm, depending on the layer.

Overall, the total surface of the detector is ~ 3000 cm^2, covered by a total number of pixels of ~ 300 millions (like the SLD vertex detector).

The total instantaneous power dissipated by each column is estimated to $\lesssim 1$ mW, based on the fast sensor prototypes already fabricated. For the whole detector, the expected instantaneous power dissipation would amount to $\lesssim 550$ W. Assuming conservatively that the detector can be switched off during at least 95 % of the time separating consecutive bunch trains, the mean power dissipated amounts to < 30 W. This value would become < 3 W with the usal 1/200 duty cycle assumption.

The consequence of the additional material due to the 2 mm side band on the impact parameter resolution was found to be modest: overall, the parameter b entering the canonical expression of the impact parameter resolution ($\sigma_{IP} = a \oplus b/p \cdot sin^{3/2}\theta$), increases by $\sim$ 5-10 %, depending on assumptions made on the remaining contributions to the material budget.

The calculation was performed assuming a sensor thickness of 50 μm. This value is actually supported by thinning attempts made recently in perspective of the upgrade of the vertex detector of the STAR experiment at RHIC [6]. Reticle size sensors (called MIMOSA-5) were successfully thinned down to ~ 50 μm via LBNL collaborators. No mechanical defect was observed posterior to the thinning operation. Electrical tests are under way.

6. SUMMARY

The tracking performances of CMOS sensors were tested extensively as a function of pitch size, charge collecting diode and temperature with a prototype (MIMOSA-9) manufactured recently in a new fabrication process (AMS 0.35 OPTO). Excellent detection efficiency and spatial resolution were obtained. The tolerance to ~ 1 MeV neutrons and ~ 10 MeV electrons was also shown to be satisfactory.

The background influencing predominently the vertex detector requirements, i.e. beamstrahlung electrons, was assessed with improved accuracy, translating into new constraints on the detector read-out time and radiation tolerance. A conceptual design of vertex detector was presented, which accounts for the read-out time requirements and exploits specific aspects of CMOS sensors. It features two different signal processing architectures, one adapted to the fast read-out required for the 2 inner layers and one taking advantage of the low occupancy in the 3 outer layers. The status of the most recent prototypes testing these two architectures was summarised.

Reticle size sensors made of 1 million pixels were thinned down to ~ 50 μm thickness in perspective of the upgrade of the STAR detector. Their first mechanical tests did not show any loss of the sensor performances.

Overall, the sensors have already met many of the detector requirements. One the major issues for the coming years will consist in integrating a fast ADC at each column end, as well as sparsification micro-circuits adapted to the high data flux coming out from the two inner layers.

References

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[6] details can be found on a web page written by Leo Greiner:
http://www.lbnl.leog.org/2005_04_06_ladder_status.htm