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Status of the UK MAPS Project

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We are developing CMOS monolithic active pixel sensors for use in the vertex detector at the future Linear Collider. Thus far, we have successfully produced three test structures designed in 0.25μm CMOS. A fourth, large area device is currently being manufactured. The three structures feature several different pixel types including a Flexible APS (FAPS). The FAPS has a 10 deep pipeline in every pixel. This is specially designed with the beam structure of the TESLA proposal in mind. Here results of a β-source test of the 3MOS, 4MOS and FAPS are presented demonstrating a signal-to-noise ratio between 15 and 20 for the various structures. Also results of an irradiation test are discussed. The devices still perform well up to fluences of 10^{14} p/cm^2 and no significant increase in leakage current are observed. Furthermore, our proposal for a CVD diamond based ladder concept will be outlined.

1. UK MAPS PROGRAM

Use of Monolithic Active Pixels Sensors to detect ionizing radiation is a recent and exciting development [1–4]. Active pixels have many highly attractive features: they can be very thin $\sim$20μm, they yield good signal-to-noise ratio (S/N) at room temperature and they offer the possibility of incorporating in-pixel data processing, making them very interesting for particle physics applications where data sparsification is an issue.

The basic MAPS pixel is a 3MOS pixel. In figure 1 the schematic of a 3MOS pixel is shown. By opening the reset switch the diode is reset. After closing the switch, charge is integrated on the diode. The integrated charge affects the gate voltage on the input source follower and hence the amount of current flowing in the read out branch when the column select switch is opened. In a 4MOS pixel the diode is separated from the reset switch and the source follower input MOS by an extra transistor. This allows a separate measurement of the voltage over the diode directly after the reset and after charge collection. This procedure corrects for variations in the reset voltage over the diode and is known as Correlated Double Sampling (CDS).

In the UK active pixel collaboration we are developing MAPS toward the linear collider vertex detector. Up to now we have successfully produced 3 test structures. The second device, the RALHEPAPS-2, is designed in the 0.25 μm CMOS Image Sensor technology. It has an 8 μm thick epitaxial layer. It contains four pixel types: standard 3MOS, 4MOS, a pixel with charge sensitive amplifier and the Flexible APS (FAPS). The FAPS has a

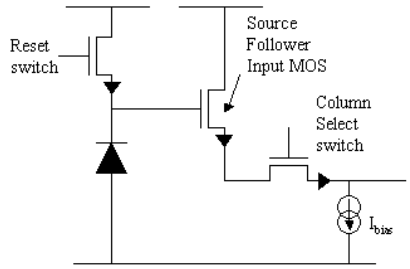

Figure 1: Schematic drawing of a 3MOS pixel.

10-deep pipeline in each pixel[5, 6]. Each pixel type comes in various flavors. The 3MOS and 4MOS each come in 6 different flavors. Their substructures consist of 64×64 pixel arrays with 15 μm pitch. The reference structure, the 3MOS A, has a 3×3 μm^2 diode. The 3MOS B has a smaller diode size, 1.2×1.2 μm^2. The 3MOS C is like B, but with Gate-All-Around (GAA) transistors. The 3MOS D is like B but with the p-well as small as allowed in the design rules. The 3MOS E has four small diodes, 1.2×1.2 μm^2, in parallel. The 3MOS F is like E but with the p-well as small as possible. For the chips produced during the first submission, the 3MOS D and 3MOS F did not work. After resubmission, all structures are working properly. However, those chips arrived too late for inclusion of their test results in this paper.
The 4MOS A, B and C only differ in threshold voltage for the extra transistor. Their diode size is 3×3 μm^2. The 4MOS D, E and F are the same as A, B and C but with GAA transistors.

2. SOURCE TEST

To measure the response of the devices to minimum ionizing particles (MIPs), the devices were illuminated using a ^{106}Ru β-source. The 4MOS pixels were read out like the 3MOS, so no CDS was used. Pedestals were calculated by averaging the signal for each pixel in all events after removing the hits. After pedestal subtraction, a common mode correction was performed for each substructure in each event separately. The noise for each pixel was obtained as the standard deviation of the pixel signal after pedestal and common mode correction and removal of the hits. Next, cluster seeds were looked for. Seeds are defined as pixels with a corrected signal larger than 8× their noise.

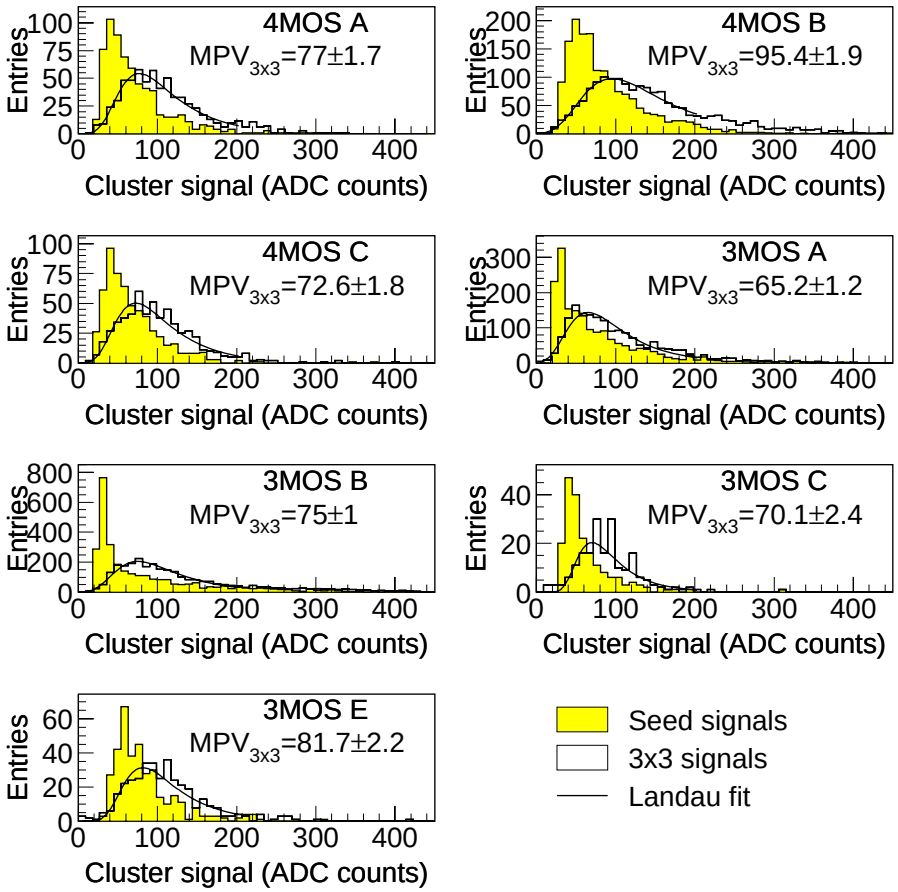

Figure 2: Cluster signal distributions.

Table I: Overview of the noise and signal/noise ratio for the RALHEPAPS-2 substructures.

Type		**N (ADC)**	**S/N**
3MOS E	4 small diodes	5.04±0.01	16.2±0.4
3MOS C	B with GAA	4.68±0.01	15.0±0.5
3MOS B	small diode	3.83±0.01	19.6±0.3
3MOS A	3×3 μm^2 diode	3.30±0.01	19.8±0.4
4MOS C	lower V_T	4.14±0.01	17.5±0.4
4MOS B	higher V_T	4.71±0.01	20.2±0.4
4MOS A	standard V_T	4.50±0.01	17.1±0.4

These pixels are combined into clusters with neighboring pixels carrying a signal larger than 2× their noise. The clusters are typically 2 or 3 pixels in size with a tail towards larger values. The cluster signal distributions are shown in figure 2. Also listed are the most probable cluster signals for cluster of a maximum 3×3 pixel size. The most probable signal is extracted by fitting a Landau distribution. The S/N is calculated by dividing the most probable signal by the average random noise of the substructure. The noise and S/N are listed in Table I.

3. RADIATION TEST

Twenty-four RALHEPAPS-2 devices were irradiated with 24 GeV/c protons using the CERN PS up to a fluence of 10^{15} p/cm^2. The maximum fluence corresponds to half the integrated radiation dose that the ATLAS pixel detectors will have to withstand during the initial planned LHC data taking period. The requirement for the ILC is to withstand 10^{12} p/cm^2. The devices were not clocked during irradiation. After irradiation the samples were kept and tested at -20 ^{0}C. To measure the S/N ratio, the devices were inserted into the source set-up. The analysis discussed in section 2 was repeated using the same cuts. The S/N decreases with increasing fluence. However, the variations between chips were found to be large, which is reflected in the large error bars. The results do demonstrate that the devices are still working reasonably well up to 10^{14} p/cm^2.

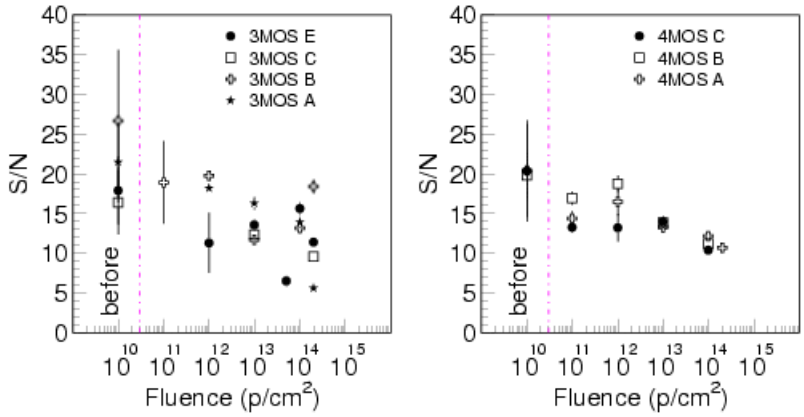

Figure 3: Signal/noise ratio as a function of dose.

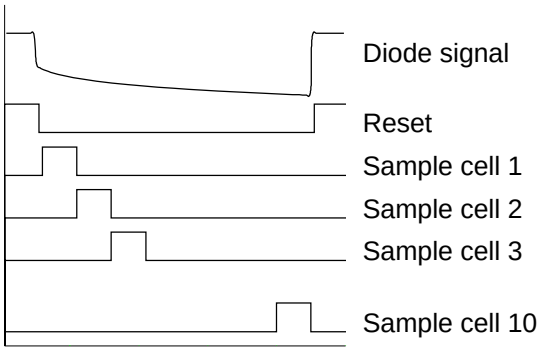

Figure 4: Timing diagram for the FAPS operation.

3.1. LEAKAGE CURRENT

The leakage current was measured by placing the device in the dark, in the fridge at -20 ^{o}C and measuring the pedestal shift while varying the integration time. The integration time was varied between 6 and 200 μs. The slope of the pedestal versus time is a measure of the leakage current in ADC counts/sec. For each substructure the leakage current was plotted versus the dose. An increase in leakage current of 1×10^{-14} ADC/ms$\times$p/cm^2 depending on the substructures, was found. Given the typical integration times used in our experiments, 10-100 μs, the pedestal only changes by less than 1 ADC count at this temperature, which is about 20% of the typical noise.

4. FLEXIBLE APS

The Flexible APS (FAPS) has a 10 deep pipeline on each pixel. This design was developed with the TESLA proposal for the Linear Collider in mind. It allows fast sampling during the pulse train and the readout to take place in between the pulse trains. Its operation is indicated in the timing diagram shows in figure 4. The FAPS is implemented in 5 different flavors. Each flavor consists of 40$\times$40 pixels of 20$\times$20 μm^2. Only results of the FAPS B will be presented here. The FAPS B has a 1.2$\times$1.2 μm^2 diode. The same β-source set-up as before was used to test the FAPS. After resetting, the signal on the diode is sampled sequentially into the 10 memory cells, see figure 4. Note that since the diode is an integrating device, a hit found in memory cell i should also be present in cell $i+1$. Subsequently, the memory cells are read out. The signal of the first memory cell, cell 1, was subtracted from the signals of the other cells resulting in offline Correlated Double Sampling. After correcting the data for the remaining common mode and pedestals, clusters were looked for in the same way as has been done for the other substructures. The cluster cuts used were 8$\times$ its noise for the seed and 2$\times$ their noise for neighbors. Hit finding was done for each memory cell separately. The cluster signal distributions for all 10 memory cells are shown in figure 5. The S/N of the cells 2 until 10 varies between (14.7$\pm$0.4) and (17.0$\pm$0.3). These values are lower than the S/N of the 3MOS B, which has the same size diode. The lower S/N is due to higher noise, which is also higher than expected [8]. The reason for this discrepancy is under investigation.

5. CVD DIAMOND LADDER CONCEPT

We propose a CVD diamond based ladder concept for the ILC vertex detector. MAPS sensors have the advantage that the actual sensor is very thin. A MAPS sensor can be thinned down to the epitaxial layer, resulting is a 20-30μm thick device, which can be operated at room temperature. The heat is mainly produced at the periphery of the device. The sensitive part does not need cooling.

However, this needs to be supported. CVD diamond is very strong and stiff and has a very long radiation length. We want to build a ladder structure out of 200 μm thick CVD diamond by cutting away all the material underneath the sensitive area of the device. Due to the excellent heat conduction of diamond in all directions, the ladder can be cooled by providing a cold contact at the end points of the ladder.
To test this principle we have purchased a prototype CVD diamond ladder, see figure 6. This prototype has dimensions that are optimized to mount the new large area RALHEPAPS-4 chip. It is 12×82 mm. This will be used to measure stiffness, stability and heat conduction. The real prototype ladder for the ILC will be longer and will have thinner rungs[1].

6. CONCLUSIONS & OUTLOOK

We have successfully produced three active pixel test structures in 0.25 μm CMOS technology. Here the results of sets of the RALHEPAPS-2 were presented. A good S/N in β-source tests was observed. The S/N varies between 15 and 20, depending on the type of pixel.
An irradiation test on the RALHEPAPS-2 was performed. Devices were irradiated up to 1×10^{15} p/cm^2. The devices

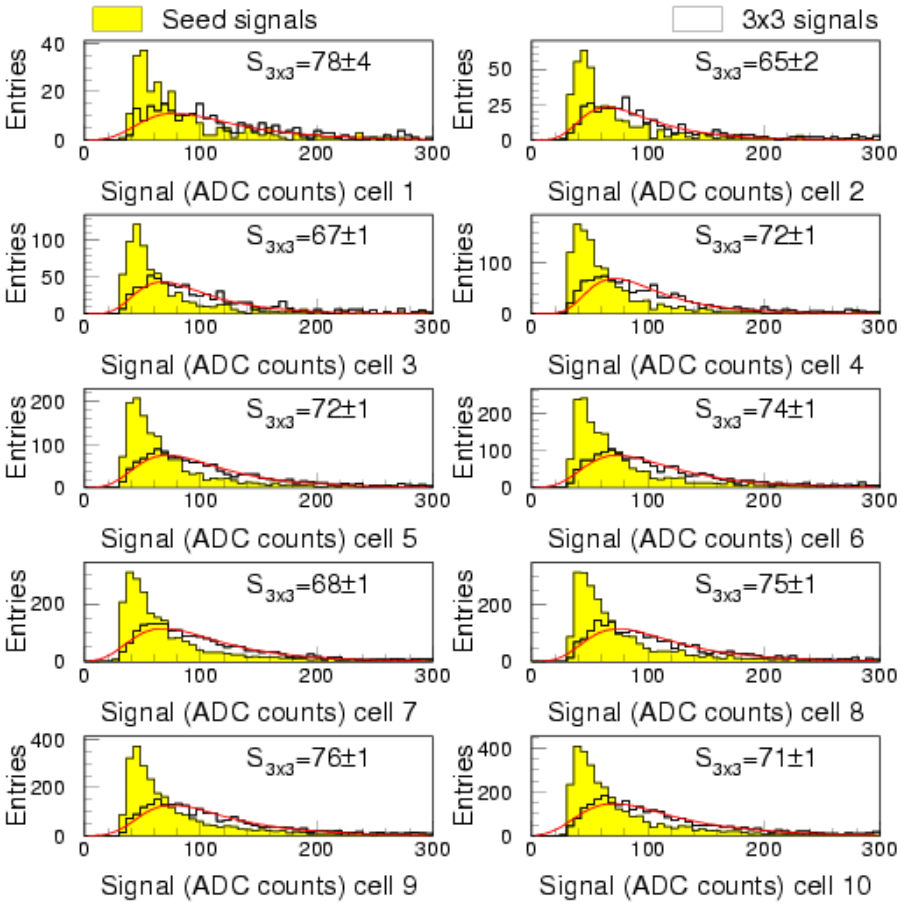

Figure 5: FAPS cluster signal distributions.

[1]The rungs at the end and halfway the ladder were chosen to be large to accommodate the uncertainty in the final RALHEPAPS-4 chip.

Figure 6: Front and rear view of the prototype ladder for the RALHEPAPS-4. The ladder is 82×12 mm.

were still operating reasonably well up to 1×10^{14} p/cm^2. The dependence of the leakage current on the radiation dose was studied. No significant increase in the leakage current was observed at the operating temperature of -20^{0}C up to 1×10^{14} p/cm^2.
Source measurements using the Flexible APS were presented. The S/N for the memory cells varied between (14.7±0.4) and (17.0±0.3). A new large scale device, the RALHEPAPS-4, will become available in the summer 2005. This device will have 1024×384 pixels with a size of 15×15 μm. It is designed in AMS 0.35 μm CMOS Optoprocess with an epitaxial layer thickness greater than 10 μm. This device will be a first step towards a full scale demonstrator pixel for the vertex detector of the ILC.

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