The Active DEPFET Pixel Sensor: Irradiation Effects due to Ionizing Radiation

L. Andricek, G. Lutz, H.-G. Moser, and R.H. Richter
MPI fuer Physik, Halbleiterlabor, 81739 Munich, Germany

A new generation of DEPFET active pixel sensors with ~25µm pixel size has been developed to meet the requirements of the vertex detector at the ILC (International Linear Collider). One of the major challenges is the dominant e+e- pair background from the beam-beam interaction. The resulting high occupancy in the first layer of the vertex detector can be reduced by an extremely fast read out of the pixel arrays but the pair-produced electrons will also damage the sensor by ionization. The expected accumulated dose in the inner layer is 100krad for a 5-year lifetime. The DEPFET[1] is a field effect transistor (MOS-type in the case of the vertex detector for the ILC) with an additional implant underneath the channel and integrated on a fully depleted substrate. It combines the functions of a detector and the first amplification stage in one single device. Like all MOS devices, the DEPFET is inherently susceptible to ionizing radiation. The predominant effect of this kind of irradiation is the shift of the threshold voltage to more negative values due to the build up of positive oxide charges. The paper presents the first results of the irradiation of such devices with hard X-Rays and Gamma rays from a ^{60}Co source up to 1Mrad under various biasing conditions.

1. INTRODUCTION

According to the TESLA Technical Design Report, the dominant background of pair-produced electrons which penetrate the inner layer of the vertex detector imposes a requirement on radiation hardness of about 100krad for a 5 year life time[2]. In addition there is NIEL damage due to the neutron background which is estimated to be at the level of 10^9 1MeV-neutrons/cm^2 per year. Since there is no charge transfer during the operation of DEPFET matrices at the ILC[3,4], damage of the silicon bulk due to NIEL is of minor importance for this kind of devices.

Table I: List of the irradiated devices

Wafer	Transistor	L (µ m)	W(µm)	Source	Biasing during irradiation
PXD4-1	T60-1	60	120	X-ray(Mo)	All terminals grounded
PXD4-1	T60-2	60	120	X-ray(Mo)	All terminals grounded
PXD4-1	T60-3	60	120	X-ray(Mo)	All terminals grounded
PXD4-2	T10-1	10	120	X-ray(Mo)	Transistor „off“
PXD4-2	T20-1	20	120	X-ray(Mo)	Transistor „off“
PXD4-2	A2-1	6	25	^{60}Co	Transistor „off“
PXD4-2	B2-1	6	25	^{60}Co	Transistor „off“
PXD4-2	D2-1	6	25	^{60}Co	Transistor „on“
PXD4-2	A2-2	7	25	^{60}Co	Transistor „off“
PXD4-2	B2-2	7	25	^{60}Co	Transistor „off“
PXD4-2	D2-2	7	25	^{60}Co	Transistor „on“
PXD4-3	T5-1	5	120	X-ray(Mo)	first „off“, then „on“

However, all MOS technologies are inherently susceptible to ionizing radiation. The main total ionizing dose effect, the shift of the threshold voltage to more negative values, is caused by radiation induced charge build up in the oxide and interfacial regions. The threshold shift of MOS transistors with a certain oxide thickness and for a given total ionizing dose in the oxide depends in the first place on the technology and the biasing conditions during irradiation.

2. IRRADIATION CONDITIONS

Twelve DEPFET MOS-type test devices from three different wafers of the current production have been irradiated with ^{60}Co gamma radiation and hard X-rays from an X-ray tube with Molybdenum target to investigate the radiation tolerance of the current technology. The devices under test are exactly the same double-pixel DEPFETs like in the main matrix[3], except for the gate area (gate length L=5µm..60µm and width W=25µm..120µm).

During normal operation at the ILC, the DEPFET is in “charge collection mode”, i.e. fully depleted with empty internal gate and switched off by applying a positive gate voltage with respect to the source. The transistors of a row are only switched on during the short read out period. The ratio T_{off}/T_{on} in the first layer of the ILC vertex detector (assuming a 512x4096 pixel array read out at both sides) is in the order of 1000. Thus the irradiation of six test devices was done with the transistors in “off” state with an empty internal gate to test for the radiation tolerance in this most frequent operation mode. To investigate the implication of the biasing conditions on radiation tolerance, some transistors were also irradiated in “on” state, others with all terminals grounded, and one transistor being first in “off” state then switched to “on” during irradiation. Table 1 lists the irradiated devices, the irradiation source, and the biasing conditions during irradiation.

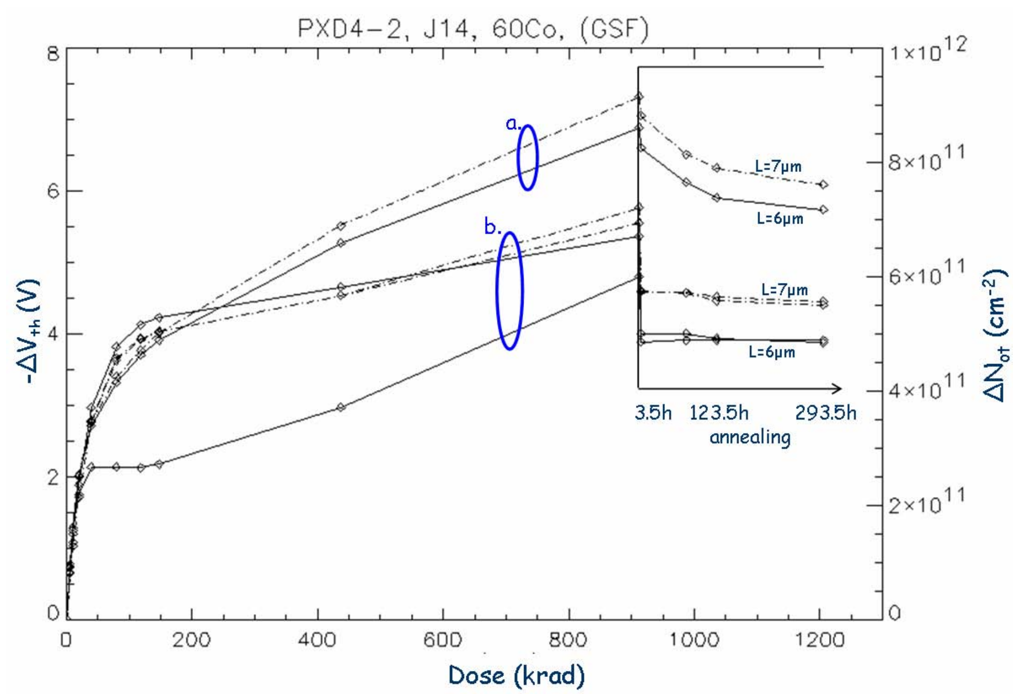

Fig. 1. Threshold shift and generated oxide trapped charge N_{ot} during ^{60}Co irradiation and after short term annealing at room temperature. The two curves labeled a. are from DEPFETs irradiated in “on” status, the curves b. are from 4 DEPFETs irradiated in “off” status.

3. RESULTS AND DISCUSSION

For the ^{60}Co irradiation, the dose rate was 20 krad(SiO_2)/h. The dosimetry was provided by the staff of the National Research Centre for Environment and Health (GSF) by means of a calibrated ionization chamber. The input characteristic of the devices were measured immediately (approximately 1 min) after each irradiation period and the threshold voltage was extracted by a quadratic extrapolation of the $I_{Drain}(V_{Gate})$ curve to $I_{Drain}=0$. Fig. 1 shows the threshold voltage shift and the density of the oxide trapped charge N_{ot} of six DEPFETs, four biased on "off" state and two in "on" state during irradiation, as a function of the total ionizing dose. The irradiation was stopped after 912krad(SiO_2) and the devices were held under bias for annealing at room temperature. For the transistors irradiated in "off" state, most of the annealing took place in the first 3.5h and the threshold voltage shift reaches a stable value of around -4V. The DEPFETs irradiated in "on" state are less radiation tolerant and the annealing has a longer time constant. The threshold voltage shift after 294.5 h annealing at room temperature is about -6V in this case. This difference can be attributed to different field configurations in the gate oxide[5]. Please note that identical DEPFETs under the same biasing conditions during irradiation have almost the same threshold shifts after irradiation and short annealing.

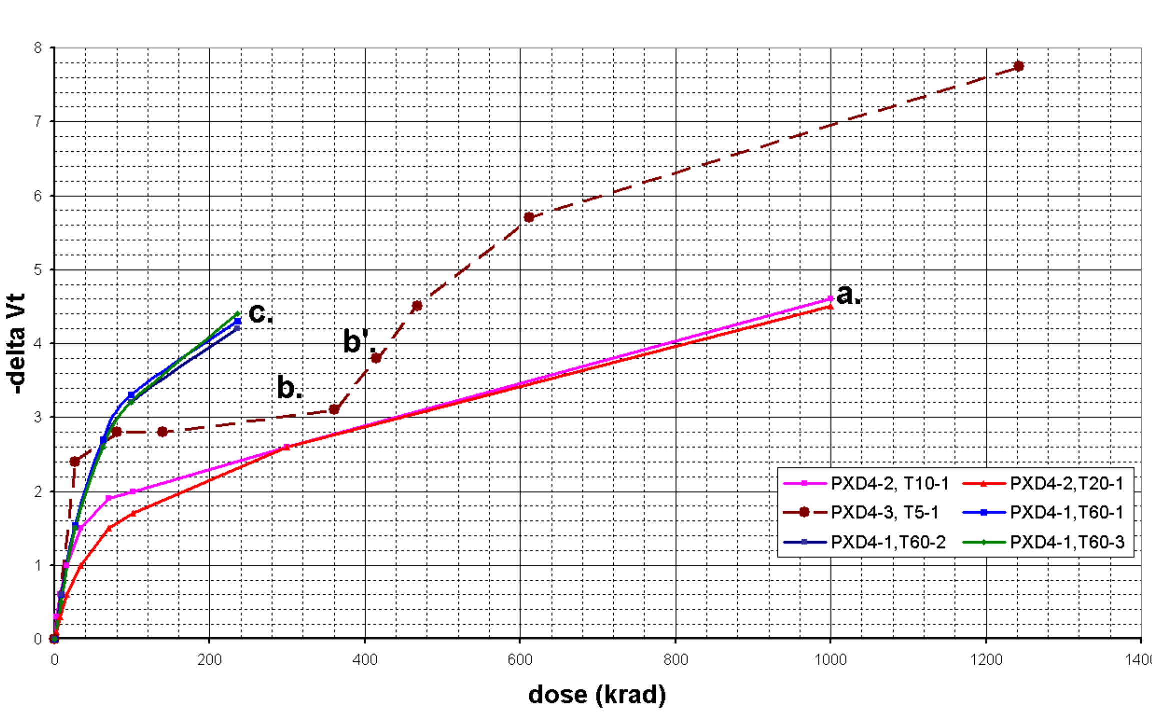

Fig. 2. Threshold shift for two transistors being in "off" state during irradiation (a.), one transistor being in "off" state for 360krad and then switched on for remaining irradiation up to 1.2Mrad was reached (b and b'), and three transistors with all terminals grounded (c.).

In order to cross check these results, the irradiations were repeated using the in house available CaliFa irradiation facility with an X-ray tube with Mo target operated at 30kV. The spectrum of the radiation is given by bremsstrahlung with the characteristic energy peak at 17.44keV of Molybdenum. The dosimetry is based on the measured spectrum and the known absorption coefficient of SiO_2[6]. The dose rate for this irradiation was lower (9krad/h) and there was an annealing step for 18h to 24h after each irradiation step. The results are shown in Fig. 3. The comparable devices, biased in the same way (curve a. in Fig. 3), show about the same threshold shift as in the previous irradiation.

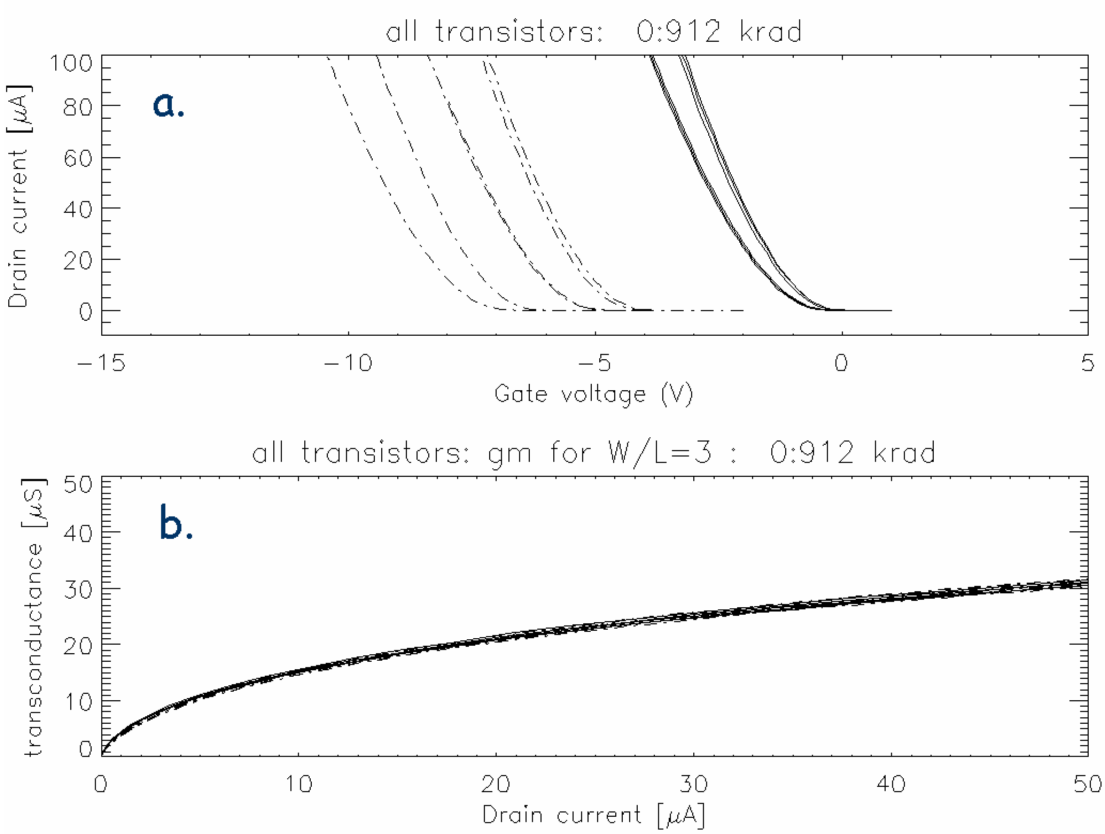

Fig. 3 Input characteristics of six DEPFETs before (solid lines) and after (dashed lines) a total ionizing dose of 912krad 60Co irradiation (a.) and transconductance normalized to W/L=3 of all six transistors before and after irradiation (b.).

4. CONCLUSIONS

Based on these irradiation results we conclude that DEPFETs biased accordingly to the operating conditions in the experiment are remarkably radiation tolerant. After a total ionizing dose of 1 Mrad(SiO_2), which corresponds to a safety factor of 10 for a 5 year operation in the first layer of the vertex detector at the ILC, the threshold voltage shift is only about -4V. The shape of the DEPFET input characteristic and the transconductance are not affected by the irradiation (see Fig. 4). Hence the radiation induced threshold voltage shift can simply be compensated by a gradual decrease of the gate voltage needed for the selection of a pixel row. Although based on a limited number of irradiated devices, it can be stated, that identical DEPFETs biased in the same way during irradiation have very similar characteristics after irradiation.

Acknowledgments

The authors would like to thank C. Hoeschen and W. Panzer at the Institute of Radiation Protection of the National Research Centre for Environment and Health (GSF) for the support and opportunity to use their ^{60}Co irradiation facility ELDORADO.

References

[1] J. Kemmer, G.Lutz, ”New Detetecor Concepts“, Nucl. Instrum. Methods, vol A253, pp. 365-377, 1987
[2] T. Behnke, S. Bertolucci, R. D. Heuer, and R. Settles, Eds., "TESLA Technical Design Report, Part IV: A Detector for TESLA", DESY, Hamburg, Germany, DESY 2001-011, March 2001
[3] R.H. Richter et al., “Design and technology of DEPFET pixel sensors for linear collider applications”, Nucl. Instrum. Methods, vol. A511, pp. 250-256, 2003.
[4] M. Trimpl, et al., "A Fast Readout using Switched Current Techniques for a DEPFET Pixel based Vertex Detector for TESLA", Nucl. Instrum. Methods, vol. A511, pp. 257-264, 2003.
[5] T.P. Ma, P. Dressendorfer, Eds., "Ionizing Radiation Effects in MOS devices and circuits", John Wiley&Sons, New York, 1989.
[6] A. Pahlke, "Einfluss der Oxidqualität auf die Stabilität von Halbleiterdetektoren bei Röntgenstrahlung", Ph.D. Thesis ,TU München, 2003