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Detector R&D at the LCFI Collaboration

Konstantin Stefanov on behalf of the LCFI collaboration
Rutherford Appleton Laboratory, Chilton, Didcot OX11 0QX, UK

The Linear Collider Flavour Identification (LCFI) collaboration has developed Column-Parallel CCDs (CPCCD) and CMOS readout chips to be used for the vertex detector at the International Linear Collider (ILC). The CPCCDs are very fast devices capable of satisfying the challenging requirements imposed by the beam structure of the superconducting accelerator. First set of prototype devices have been designed, manufactured and successfully tested, with second generation chips on the way. Another idea for CCD-based device, the In-situ Storage Image Sensor (ISIS) has also been developed and first prototype designed. The most recent results and plans for the immediate future are outlined.

1. INTRODUCTION

The International Linear Collider (ILC) will require at its heart a vertex detector with excellent performance to demonstrate its full physics potential. In particular, point measurement resolution better than 3.5 μm and low material budget (< 0.1% X_0 per layer) to reduce the error from multiple scattering are needed for pure and efficient flavor tagging and vertex charge measurement [1]. It is widely accepted that the pixel size of the sensor has to be around 20×20 μm^2 to achieve that resolution and to allow two-track separation of 40 μm. The present conceptual design includes 5 concentric layers of sensors arranged around the beam pipe and housed in a low mass foam cryostat. The innermost layer consists of 8 devices with size 100×13 mm^2, read out from both ends. The outer 4 layers are made of "ladders" of 2 devices with size 125×22 mm^2, butted together and read out from one end only.

The detector has to withstand only moderate radiation backgrounds, mostly from pair production (≈20 krad/year) and 10^9 cm^{-2} 1 MeV-equivalent neutrons for the same period. Recently, concerns have been raised about possibly significant beam-related electromagnetic interference (EMI) in the ILC environment, which the vertex detector must tolerate. Although the level of EMI is difficult to quantify at the moment, LCFI takes those issues seriously and makes efforts to address them in the detector R&D work.

One particular constraint posed by the beam structure at ILC relates to the readout rate of the sensors. The integration of all events produced during the 1 ms-long bunch train would cause the detector occupancy to be uncomfortably high. To keep it well below 1% multiple readouts during the beam will be needed, however the acquired information does not necessarily have to leave the sensor, but could be stored in pixel and retrieved later in the 200 ms-long gaps between the bunch trains.

LCFI has adopted two approaches to sensor development, which could satisfy the requirements of the ILC. The more mature one is the Column-Parallel CCD (CPCCD), which can accomplish very fast readout by equipping every column of a custom CCD with separate output, amplifier and an ADC. This makes it possible to read out the 3.3 Mpixel inner layer sensors 20 times during the bunch train and consequently reduce the occupancy to acceptable levels. Clock frequency of 50 MHz is needed for the first layer devices, however 25 MHz for layers 2 through 5 would suffice because of the lower hit density. LCFI has produced and tested the first CPCCD prototype and its readout chip, and currently is working on the second generation devices.

The second approach is to store 20 time samples of the signal charge within the pixel during the beam train and to read them out in the long gaps in between. This is equivalent to complete readout at 50 μs intervals in the CPCCD. LCFI has developed the In-situ Storage Image Sensor (ISIS) concept, based on CCDs, and has designed its first device as a proof of principle.

2. DEVELOPMENT OF THE COLUMN-PARALLEL CCD

2.1. First Generation CPCCD – CPC1

Our first CPCCD (CPC1) was designed and manufactured at e2V Technologies (UK) in 2003. The CPC1 is a 2-phase device with 750(H)×400(V) 20 μm square pixels, optimized for low voltage operation by reduced inter-gate implant barrier. The CCD has two charge transport sections – field-enhanced and standard, and three different output circuits. Selected columns from both sections are served by triplets of 2-stage source followers for high speed testing with discrete electronics. Two banks of 125 single stage source followers and 125 direct connections to the CCD output nodes on 20 μm pitch are also provided for bump-bonding to the CMOS readout ASIC, the CPR1. Every third output has larger pad for wire bonding, matching a corresponding pad in CPR1 and used for tests with limited connectivity.

CPC1 performed very well, showing excellent operation at clock amplitudes of only 1.9 V peak-to-peak and noise of below 60 electrons RMS at 1 MHz column parallel readout. Despite the non-optimal on-chip clock delivery the CPC1 worked at speeds of up to 25 MHz.

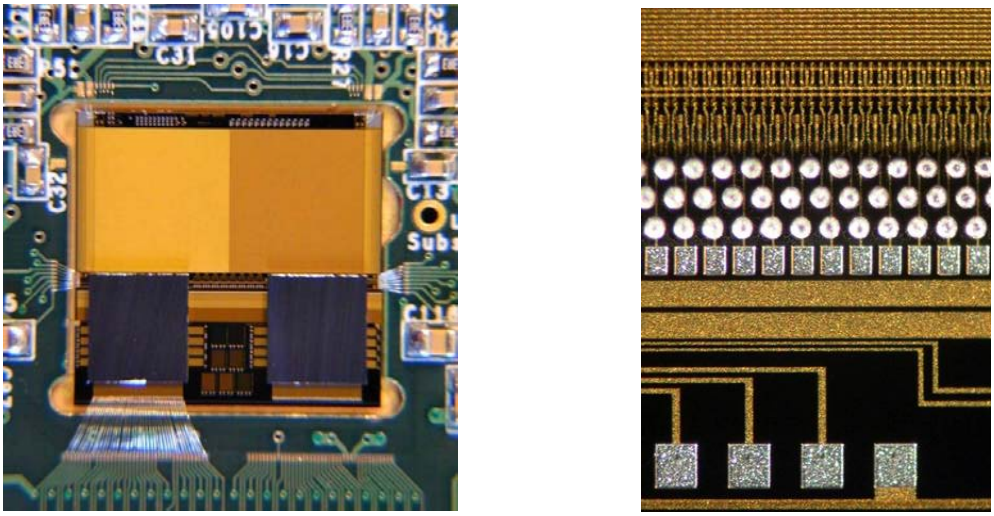
2.2. Readout Chip for CPC1 (CPR1)

A dedicated ASIC for CPCCD readout (CPR1) was designed by the Microelectronics Group at RAL and manufactured on 0.25 μm CMOS process at IBM. The chip contains 125 voltage and 125 charge amplifiers for connection to the single stage source followers and the direct outputs on CPC1. The signals from the amplifiers are passed through a clamp-and-sample Correlated Double Sampling (CDS) circuit and digitized by 250 5-bit flash ADCs. The information from each channel is stored on a 132-deep FIFO for consequent readout.

2.3. Bump-bonded Hybrid Assembly with the CPR1 Readout Chip

After the successful stand-alone tests of CPC1, several chips were bump-bonded to two CPR1 each at VTT (Finland) using eutectic solder process. A picture of the hybrid assembly in a test board is shown on Figure 1(a). A number of assemblies worked well and the first X-ray signals, generated in the CCD and amplified and digitized in the readout chip were soon observed. The noise in the voltage channels was 60 electrons and around 100 electrons in the charge channels, however the gain in the latter was found to be insufficient. Every third charge channel exhibited higher noise due to the parasitic capacitance of the larger wire bondable pad attached to it. All ADCs and charge channels worked fine, however about 20% of all voltage channels did not show any signal in all chips, at random locations. The cause of this is still unknown.

The bump-bonding yield was found to be low, around 30%. The inspection of the bump bonds, shown on Figure 1(b), did not reveal any visible defects. The nature of the problems suggested mechanical damage of the chips during the bonding process, and we are considering measures to avoid that in the future.



(a) (b)

Figure 1: CPC1 with two bump-bonded CPR1 chips in a test PCB (a); and bump bonds on CPC1 after removing a defective CPR1 chip (b).

2.4. Next Generation Devices – CPC2 and CPR2

Following the successful tests of our first CPCCD and its readout chip, the next generation devices CPC2 and CPR2 were designed. CPC2 has got two charge transport sections and reduced inter-gate implant barrier as in CPC1 for further studies on low clock amplitude drive. An important new development is the "busline-free" design for clock distribution. In this architecture the clocks propagate on two metal layers that cover the entire image area of the CCD, separated by an insulating polyimide layer. This drastically reduces the parasitic impedance associated with the conventional CCD buslines and enables efficient clocking of large devices.

Three sensors with common design are being manufactured by e2V Technologies with expected delivery in July 2005. The largest CPC2-70 has an image area of 92×15 mm^2 and total size of 105×17 mm^2, allowing for 2 bump-bonded readout chips. This device is almost the size needed for the outer layers of the vertex detector at the ILC. The middle size CPC2-40 (53×15 mm^2 image area) represents half of the inner layer of the vertex detector and will be used to achieve the design speed of 50 MHz column parallel readout. Some devices will be made on 1 kΩ.cm high resistivity epitaxial layer to achieve full depletion. Initially, miniature transformers will be used to deliver the clock signals from a power RF amplifier, which will evolve into the development of a dedicated IC driver chip.

The next generation readout chip CPR2 builds on the experience gained with CPR1 and has already been designed, manufactured and delivered. In addition to the banks of voltage and charge amplifiers, matched to the outputs of CPC2, CPR2 implements cluster finding logic on 2×2 pixel kernel and sparse readout circuitry. Numerous test features have

been provided, such as direct analog inputs and outputs from selected amplifiers, scan register for independent tests of the sparsifying logic and direct monitoring of every ADC channel. The clock distribution network has been improved to reduce the differential nonlinearity at small full scale range of the ADCs.

3. IN-SITU STORAGE IMAGE SENSOR (ISIS)

Past experience has shown that beam-related EMI can cause noise and even disrupt the operation of the vertex detector [2]. This is a particular concern for the linear collider because of the single pass operation and the nanometer size beams, which necessitates beam diagnostics close to the interaction point. These monitors inevitably disrupt the symmetry of the beam pipe and create potential sources of parasitic Radio Frequency (RF) leakage.

All sensors, converting the signal charge into voltage during the bunch train are potentially vulnerable to RF pickup. This concern triggered the idea of the ISIS [3], shown on Figure 2. In the ISIS the signal charge is collected under a photogate and then shifted every 50 μs to a 20-cell deep linear CCD in pixel during the beam. After that, the stored charge is shifted out and converted to voltage in the 200 ms gap between the bunch trains, completely avoiding the RF pickup. Clock frequency of only 1 MHz, assuming column parallel readout, is required to retrieve all stored charge from the full scale device.

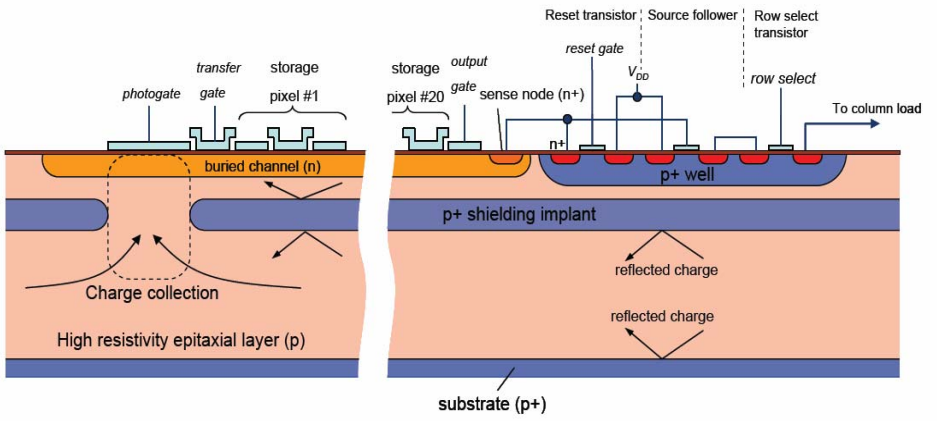


Figure 2. Cross section of the ISIS with linear CCD storage.

In addition to its great immunity to EMI, the ISIS should be orders of magnitude more radiation hard than the CPCCD. The greatly reduced number of transfers (20 instead of 6250) means that a lot less charge will be lost in radiation-induced traps. The ISIS is also much easier to drive due to the low clock frequency, and longer shaping times for readout could be used, leading to reduced noise and more precise hit measurement.

Although a very attractive concept, the manufacture of this device is not straightforward because it combines features usually not found in a single semiconductor process. The implementation of the CCD buried channel, particularly in low voltage CMOS process could be a challenge. The *p*+ shielding implant should be placed at a depth of 2 μm or more, which requires high energy ions.

Together with e2V Technologies LCFI has developed an ISIS device based on standard CCD process, utilizing diffused *p*+ well for charge shielding instead of buried deep implant. The device is an array of 16×16 ISIS cells, each

containing a 3-phase CCD with 5 pixels, reset transistor, source follower and a row select transistor. Due to the limitations of the single level metal process and the feature size, the cells are laid on 40 μm × 160 μm pitch. This device is now in manufacture and will be delivered together with the CPC2 devices.

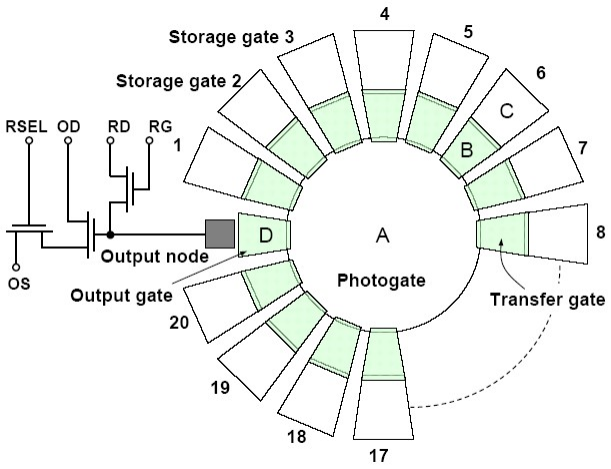


Figure 3. Principle of operation of the Revolver ISIS.

Another possible way to implement the ISIS is using a "revolver" arrangement of gates to transfer and store the charge, shown on Figure 3. Charge collected at the photogate A is shifted via transfer gate B to storage gate C during the beam. On readout the stored charge is moved back from C to B to A and finally via output gate D to the output. The main attraction of the Revolver ISIS is the reduced number of transfers and gates to achieve the storage of the same number of samples, compared to the Linear ISIS. The simulations have shown that in the Revolver ISIS the charge transfer takes about 150 ns because mainly diffusion is involved, but that is considered acceptable.

4. SUMMARY

Our work on the development of the CPCCD for the vertex detector at ILC is well advanced. The first devices and their readout chips have been successfully produced and tested. The devices were bump-bonded and the performance of the hybrid assembly was encouraging. Second generation devices were designed and are currently being manufactured. The forthcoming CPC2 will be almost detector-scale device, which will allow studies of clock propagation and charge transfer in large chips. The ISIS concept offers significant advantages for the ILC environment and will be pursued in the future. The first prototype has been designed and will be delivered together with the CPC2 for tests.

References

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