



Level-1 Regional Calorimeter System for CMS



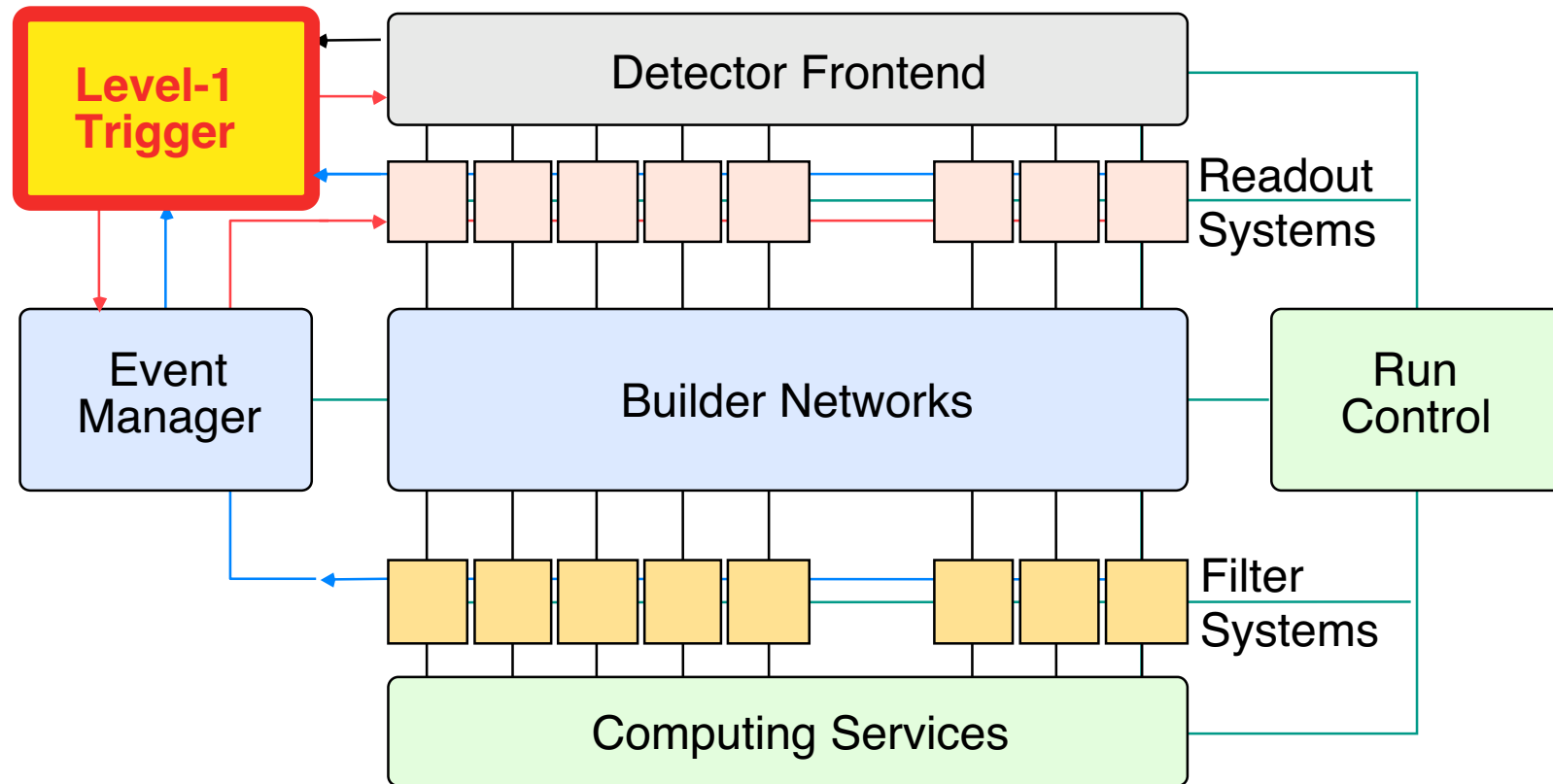
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CHEP
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The pdf file of this talk is available at:
<http://cmsdoc.cern.ch/~pamc/CHEP03.pdf>
See also CMS Level 1 Trigger Home page at
<http://cmsdoc.cern.ch/ftp/afscms/TRIDAS/html/level1.html>

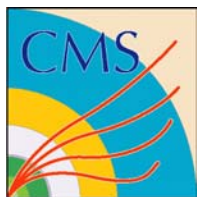


Trigger & DAQ Systems



Level-1 Trigger Requirements:

- Input: 10^9 events/sec at 40 MHz at full Luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$
- Output: 100 kHz (50 kHz for initial running)
- Latency: 3 μsec for collection, decision, propagation



CMS Detector



31 Nations, 150 Institutions, 1870 Scientists

TRIGGER & DATA ACQUISITION

Austria, CERN, Finland, France, Greece, Hungary, Italy, Korea, Poland, Portugal, Switzerland, UK, USA

TRACKER

Austria, Belgium, CERN, Finland, France, Germany, Italy, Japan*, Switzerland, UK, USA

CRYSTAL ECAL

Belarus, CERN, China, Croatia, Cyprus, France, Italy, Japan*, Portugal, Russia, Switzerland, UK, USA

PRESHOWER

Armenia, Belarus, CERN, Greece, India, Russia, Taiwan (PC), Uzbekistan

RETURN YOKE

Barrel: Czech Rep., Estonia, Germany, Greece, Russia
Endcap: Japan*, USA

SUPERCONDUCTING MAGNET

All countries in CMS contribute to Magnet financing in particular:
Finland, France, Italy, Japan*, Korea, Switzerland, USA

HCAL

Barrel: Bulgaria, India, Spain*, USA
Endcap: Belarus, Bulgaria, Russia, Ukraine
HO: India

FEET

Pakistan China

FORWARD CALORIMETER

Hungary, Iran, Russia, Turkey, USA

MUON CHAMBERS

Barrel: Austria, Bulgaria, CERN, China, Germany, Hungary, Italy, Spain,
Endcap: Belarus, Bulgaria, China, Korea, Pakistan, Russia, USA

* Only through industrial contracts

Total weight : 12500 T
Overall diameter : 15.0 m
Overall length : 21.5 m
Magnetic field : 4 Tesla



Calorimeter Trig. Overview

(located in underground counting room)



4K 1.2 Gbaud serial links w/
2 x (8 bits E/H/FCAL Energy
+ fine grain structure bit)
+ 5 bits error detection code
per 25 ns crossing

US CMS HCAL:
BU/FNAL/
Maryland/
Princeton

Calorimeter
Electronics
Interface

US CMS ECAL:
Lisbon/
Palaiseau

72 ϕ x 60 η H/ECAL
Towers ($.087\phi$ x
 $.087\eta$ for $\eta < 2.2$ &
 $.174-.195\eta$, $\eta > 2.2$)
HF: 2x(12 ϕ x 12 η)

US CMS:
Wisconsin

Calorimeter
Regional
Trigger

Receiver
Electron Isolation
Jet/Summary

Copper 80 MHz Parallel
4 Highest E_T :
Isolated & non-isol. e/γ
Central, forward, τ jets,
 E_x , E_y from each crate

UK CMS: Bristol

Cal. Global Trigger
Sorting, E_T^{Miss} , ΣE_T

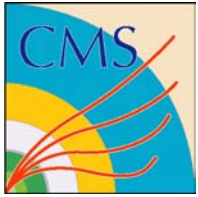
Lumi-
nosity
Info.

CMS:
Vienna

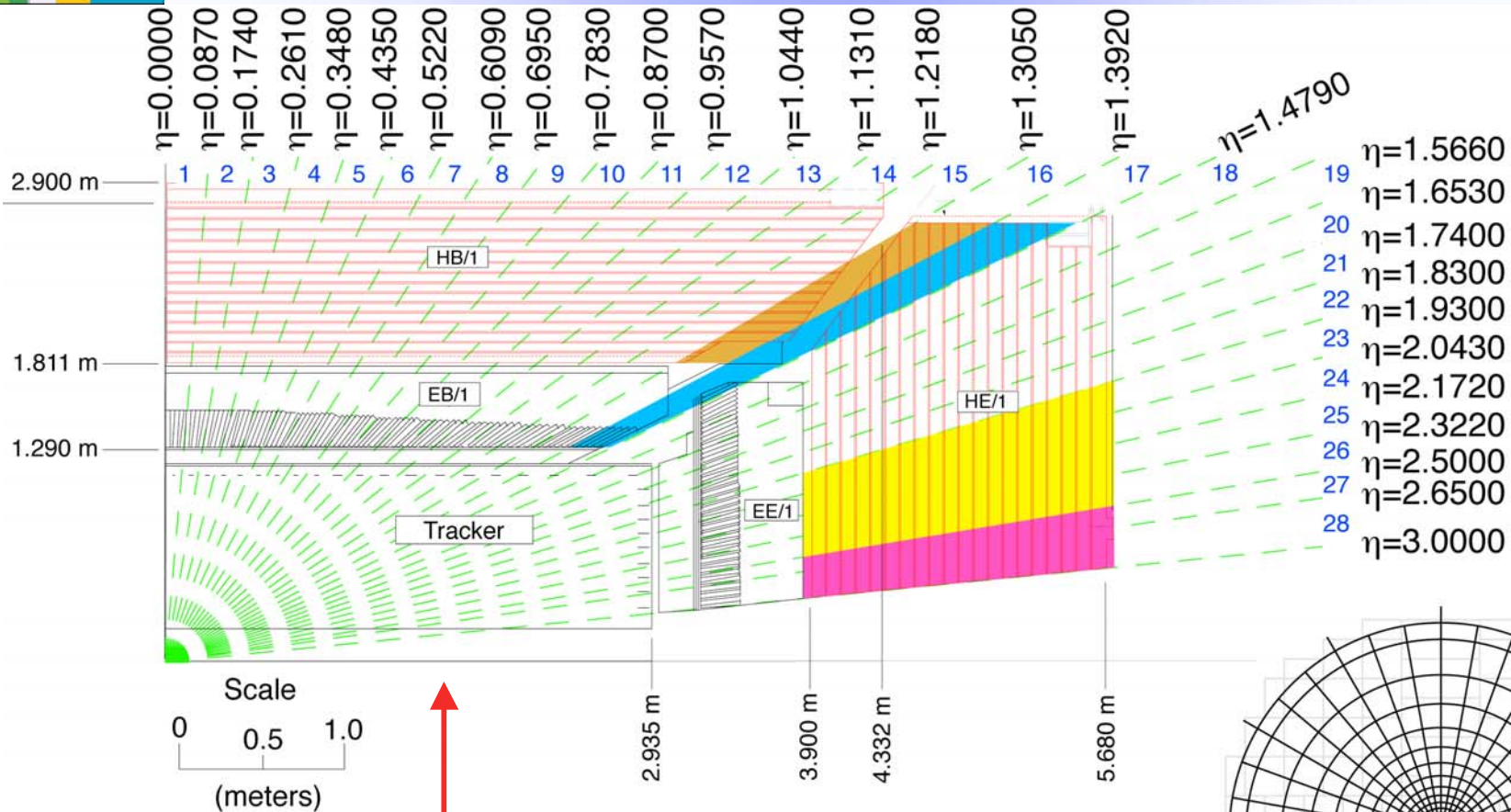
Global
Trigger
Processor

Muon Global Trigger
Iso Mu Minlon Tag

Minlon & Quiet
Tags for
each 4ϕ x 4η region



CMS Calorimeter Geometry



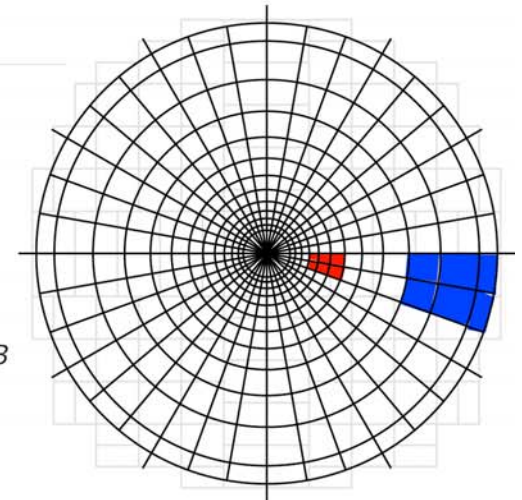
EB, EE, HB, HE map to 18 RCT crates

Provide e/γ and jet, τ , E_T triggers

2 CMS HF Calorimeters mapping onto Trigger System HF Crate

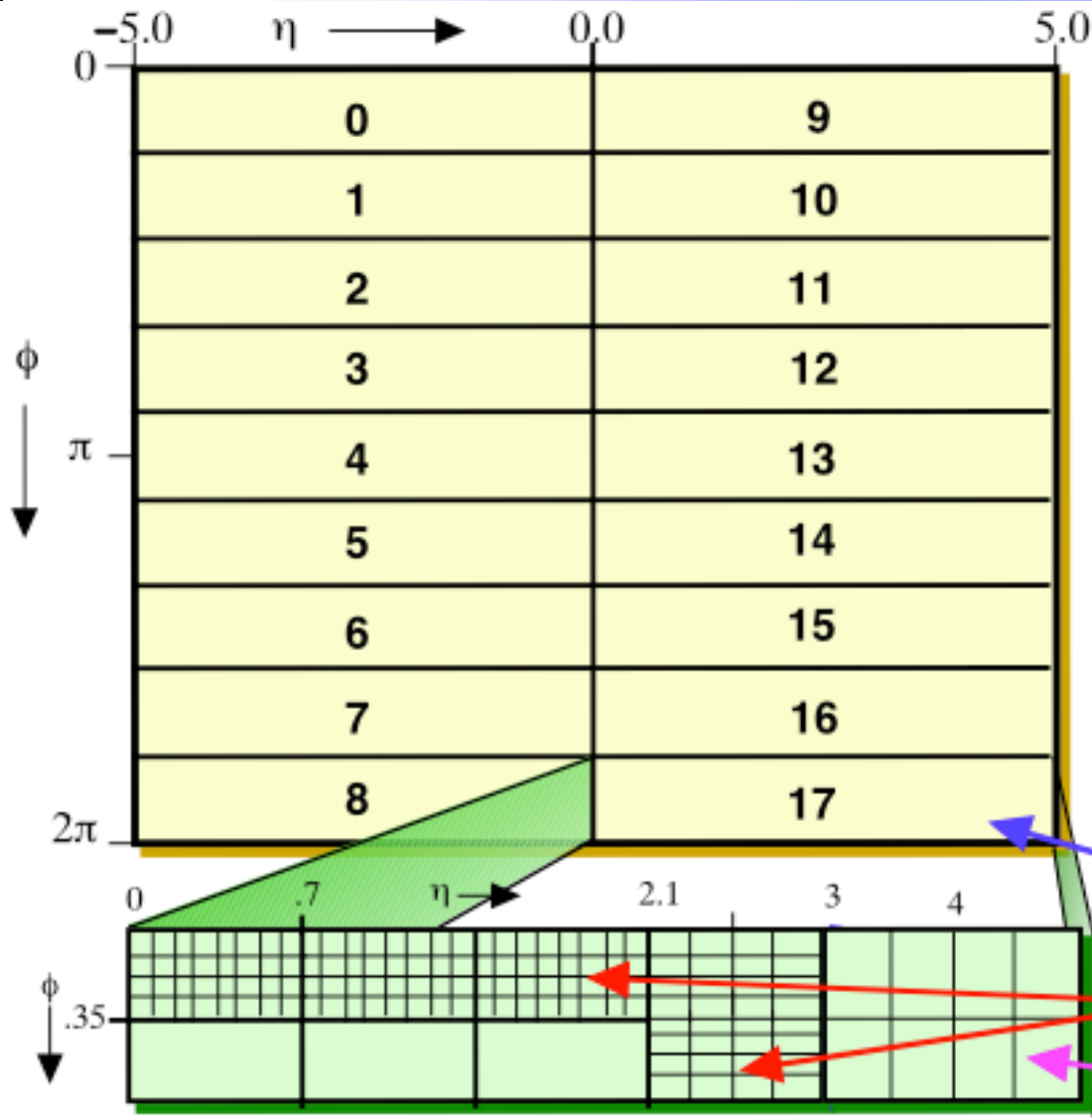
Readout segmentation: $36\phi \times 12\eta \times 2z \times 2F/B$

Trigger Tower segmentation: $18\phi \times 4\eta \times 2F/B$





Trigger Mapping



• 18 crates handle all of the CMS calorimeters seamlessly

• Each crate processes a $0.7 \phi \times 5.0 \eta$ region.

• Each Receiver/Electron ID card pair typically covers a $.35 \phi \times 0.7 \eta$ region

• Single Jet/Summary card handles full crate

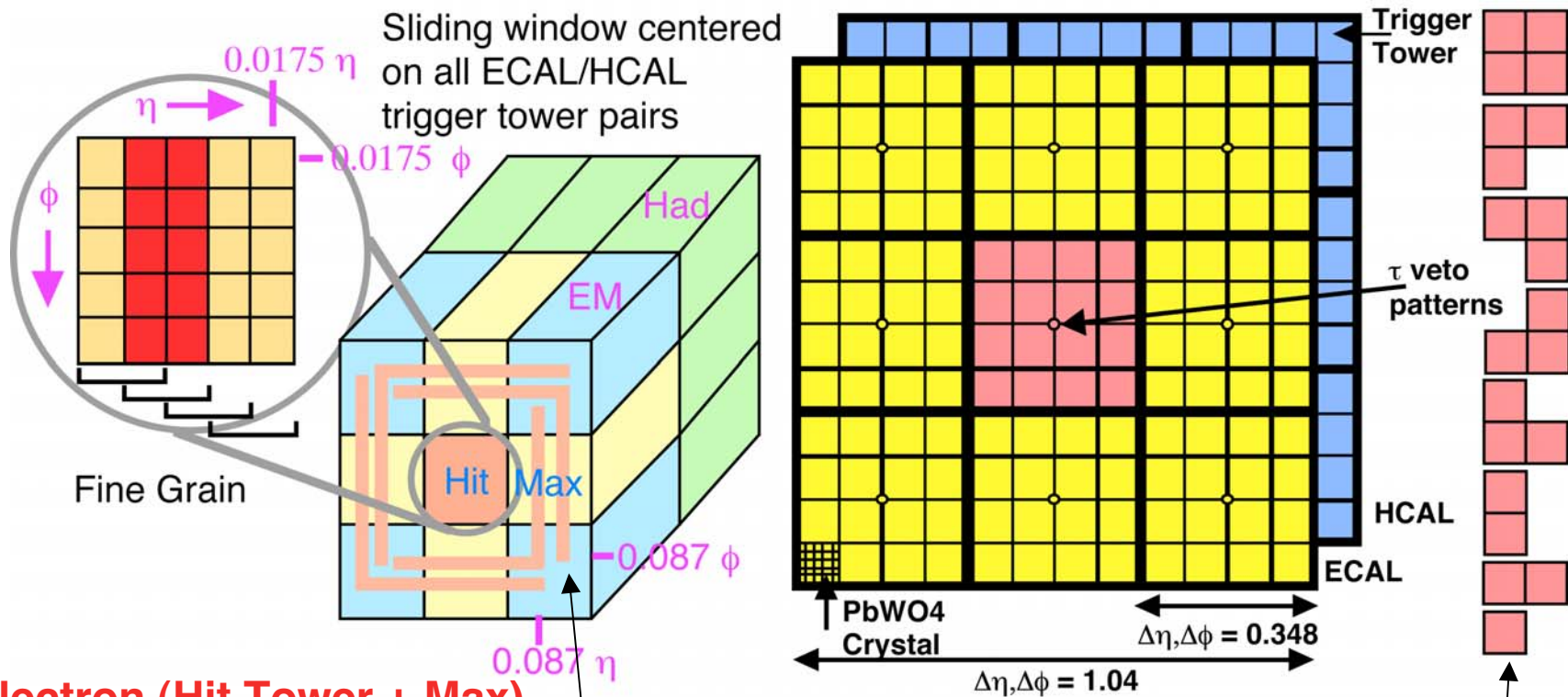
Calorimeter Regional Trigger Crate (18x)

Receiver Cards (x7/crate)

(New) Jet/Summary Card processes HF data ($3 < \eta < 5$)



Calorimeter Trig. Algorithms



Electron (Hit Tower + Max)

- 2-tower ΣE_T + Hit tower H/E
- Hit tower 2x5-crystal strips $>90\%$ E_T in 5x5 (Fine Grain)

Isolated Electron (3x3 Tower)

- Quiet neighbors: all towers pass Fine Grain & H/E
- One group of 5 EM $E_T < \text{Thr.}$

Jet or τ E_T

- 12x12 trig. tower ΣE_T sliding in 4x4 steps w/central 4x4 $E_T > \text{others}$

τ : isolated narrow energy deposits

- Energy spread outside τ veto pattern sets veto
- Jet $\equiv \tau$ if all 9 4x4 region τ vetoes off

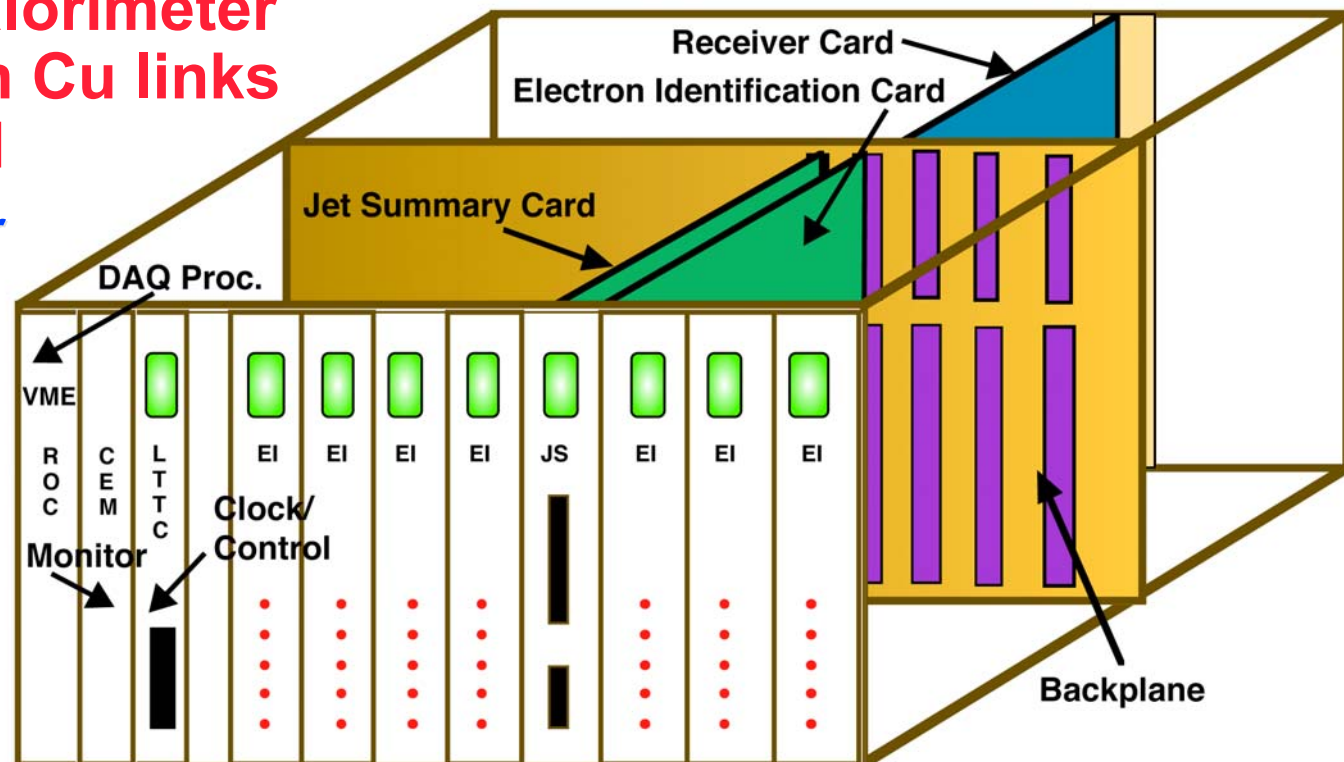


Calorimeter Trigger Crate



**Data from calorimeter
Front End on Cu links
@ 1.2 Gbaud**

**• Into 126* rear
Receiver
Cards**



160 MHz point to point backplane

- **18* Clock&Control, 126* Electron ID, 18* Jet/Summary Cards**

- all cards operate @ 160 MHz

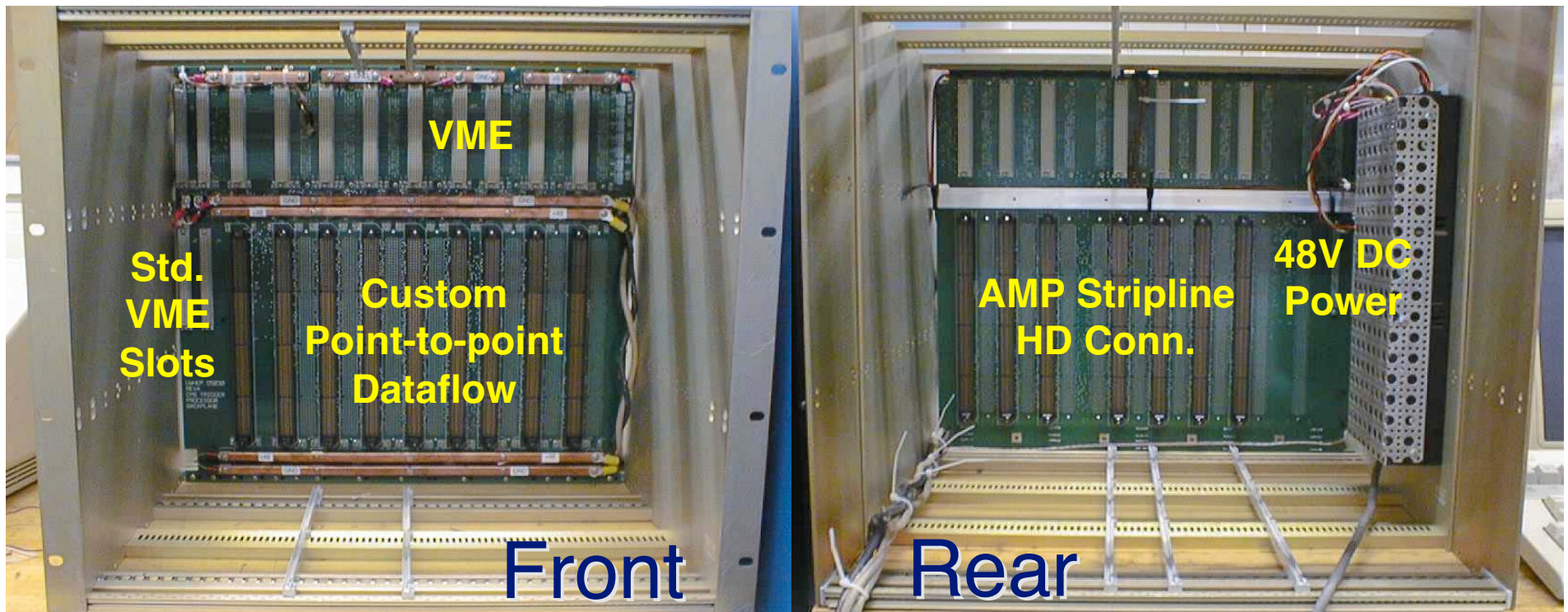
- **Use 5 Custom Gate-Array 160 MHz GaAs Vitesse Digital ASICs**

- Phase, Adder, Boundary Scan, Electron Isolation, Sort (manufactured)

**Spares
not
included*



Crate & Backplane



Designed by J. Lackey

160 MHz differential ECL with 0.4 Tbit/sec dataflow

- Tests indicate good signal quality

Designed to incorporate algorithms

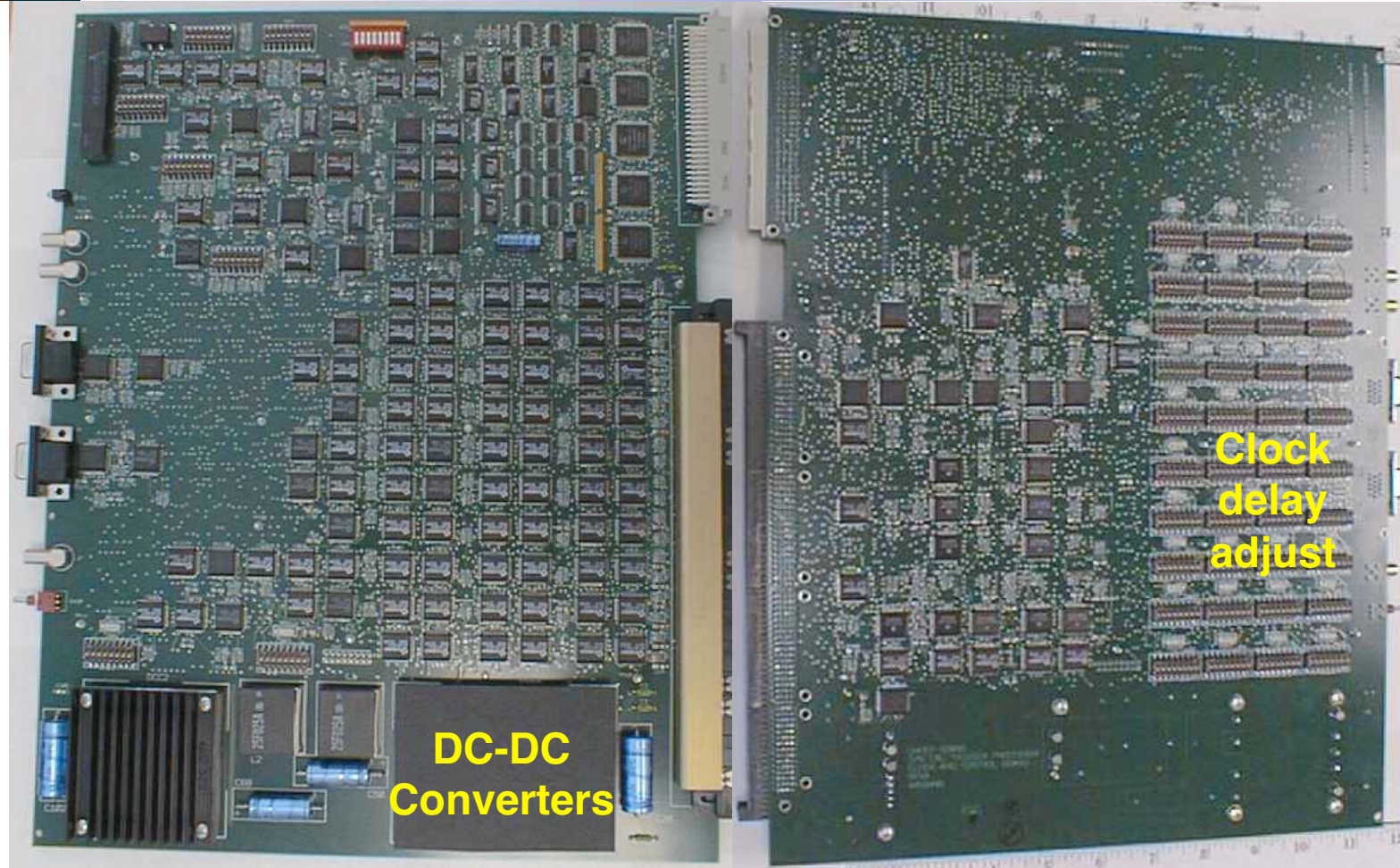
- Non-Isolated Electron, Tau & Jet Triggers



Clock & Control Card



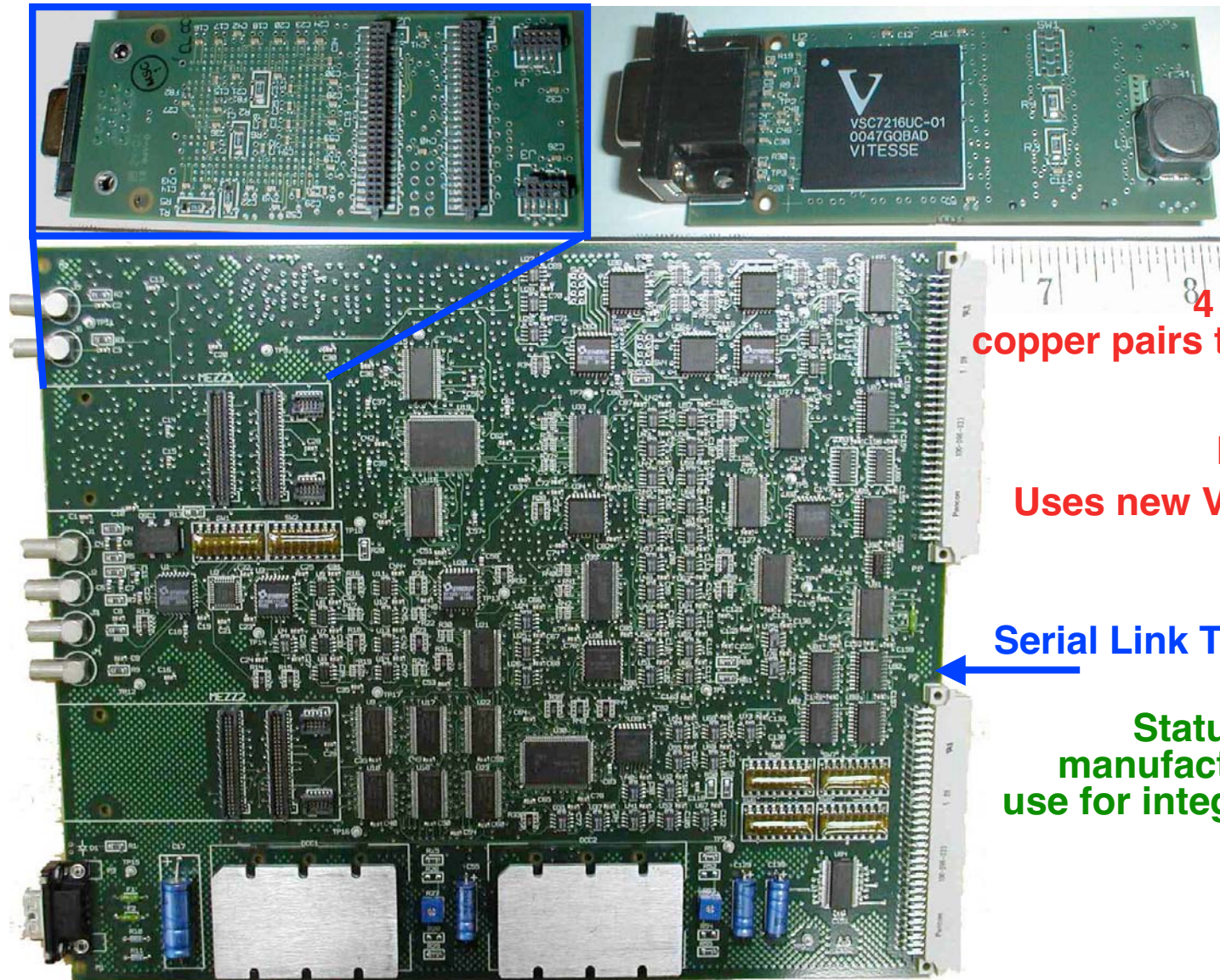
Designed by J. Lackey



**Fans out 160 MHz clock & adjusts phase to all boards
~90% of functionality tested successfully
Clock and Reset timing set with delay adjust**



New Cal. Trig. 4 Gbaud Copper Link Cards & Serial Test Card



8 Compact Mezzanine Cards for each Receiver Card accept 4 x 20 m 1.2-Gbaud copper pairs transmitting 2 cal. tower energies every 25 ns with low cost & power. Uses new Vitesse Link Chips (7216-01).

Serial Link Test Card to check links

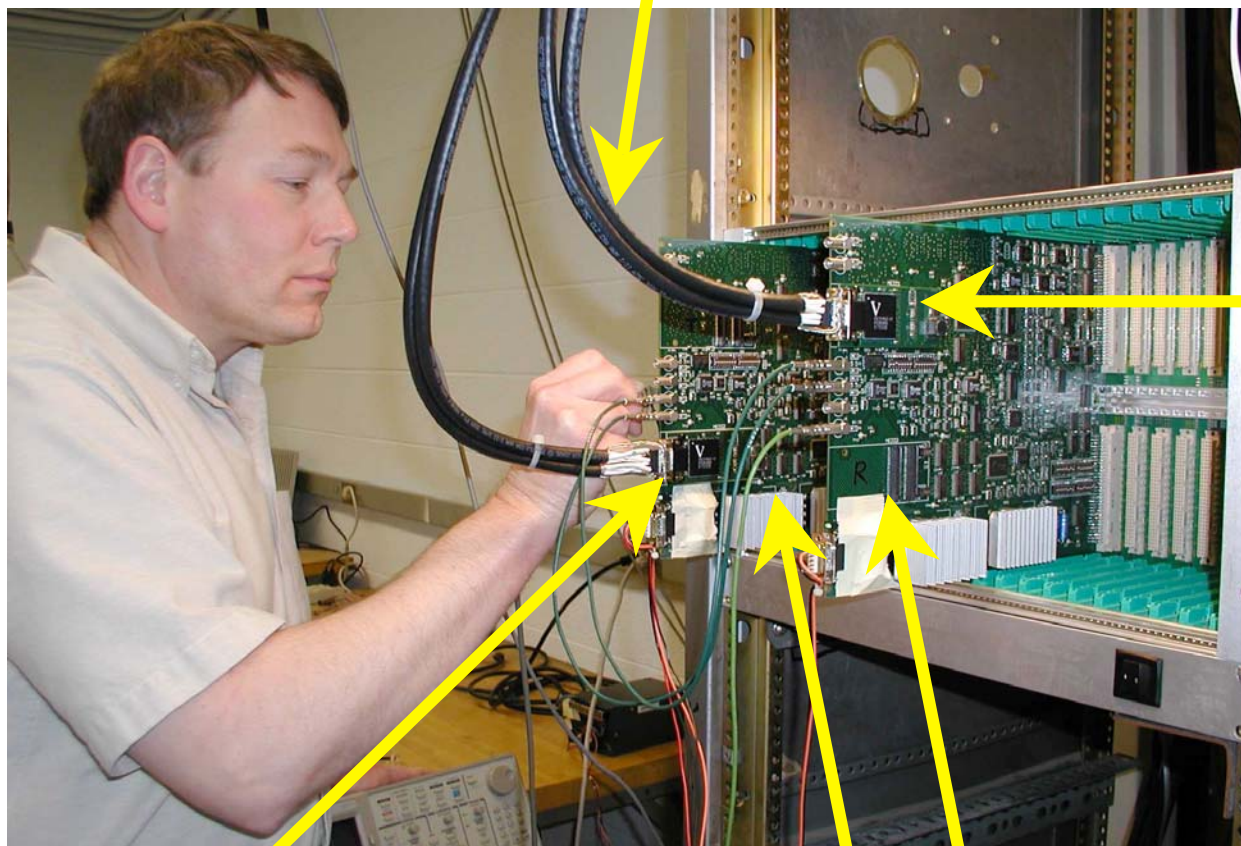
Status: full production manufactured, currently in use for integration with ECAL



4 x 1.2 Gbaud Copper Link Testing



20 m 22 AWG Copper Cable, VGA Connector



Receiver
mezzanine card



Test Transmit
mezzanine card

Serial Link Test Cards

Results:
Bit Error rate $< 10^{-15}$

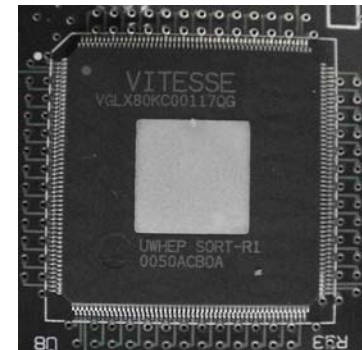


High Speed Custom ASICs



Custom ASICs

- Vitesse FX™ and GLX™ gate arrays utilizing sub-micron high integration GaAs MESFET Technology
- All I/O is 160 MHz ECL, except 120 MHz TTL input to Phase ASIC
- All have JTAG on I/O, except Phase - only on output
- All validated except EISO ASIC - requires a full crate of Receiver Cards
- Phase ASIC
 - Receives four channels of 120 MHz TTL data via V7216-01 deserializer
 - Aligns & synchronizes the data, handles bit error detection
 - Can enable test vectors for checking data routes
- Adder ASIC
 - Sums up the energy in the 4x4 regions
- BSCAN ASIC
 - Drivers for data sharing, differential output
- Sort ASIC →
 - Receives differential input, sorts e/γ and receives region sums (sort is optional)
- EISO ASIC
 - Implements electron isolation algorithms



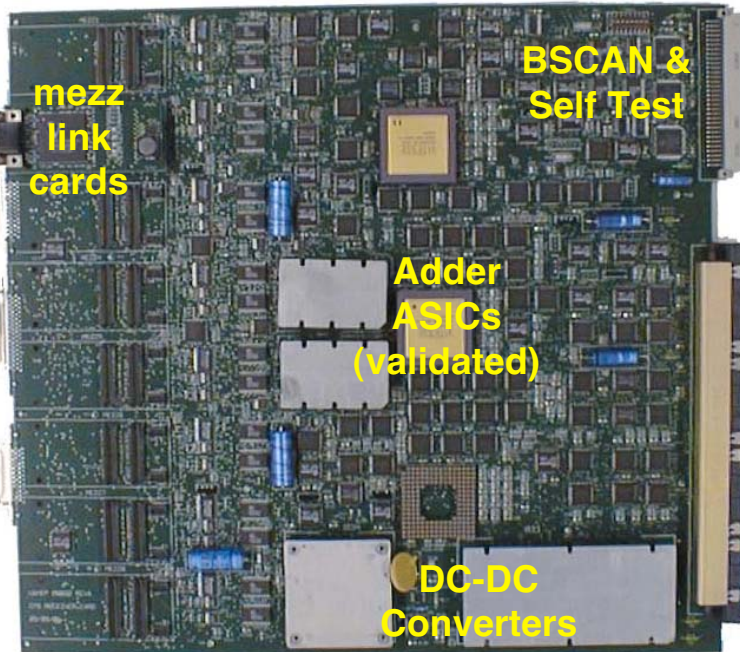


Calorimeter Trigger Receiver Card



Calo In:
4 Chan.
24 bits:
2x9 data
+ 5 error

Designed by J. Lackey

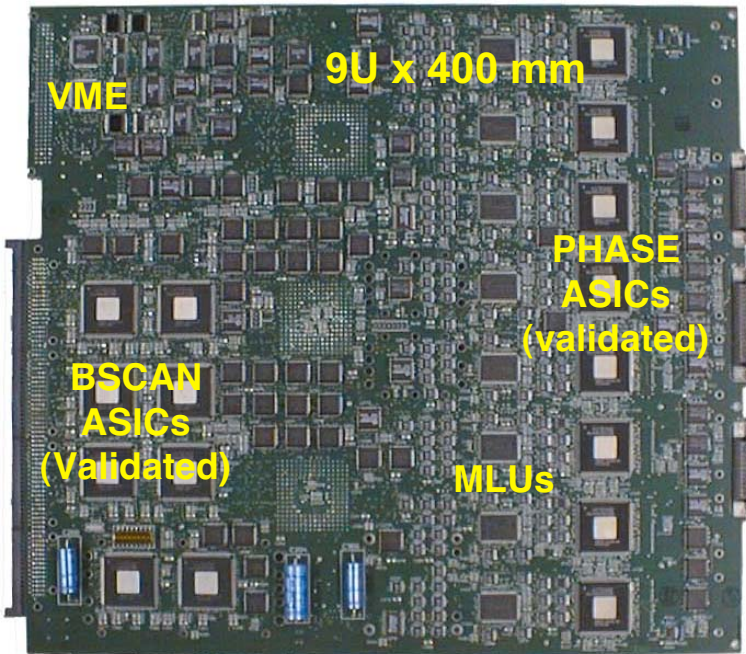


*Top side with 1 of 8 mezzanine cards
& 2 of 3 Adder ASICs*

32 Channels = 4 Ch. x 8 mezzanine cards
with Vitesse 7216-1 1.2 GBaud copper
receivers

V7216-1 deserializes data and sends
120 MHz TTL to front Phase ASIC

**Full featured final prototype board is validated - production underway, boards
manufactured for full crate test, 1422 mezzanine cards being manufactured.**



*Bottom side with all Phase
& Boundary Scan ASICs*

Phase ASIC: Deskew, Mux @ 160MHz

Error bit for each 4x4, Test Vectors

Memory LUT @ 160 MHz

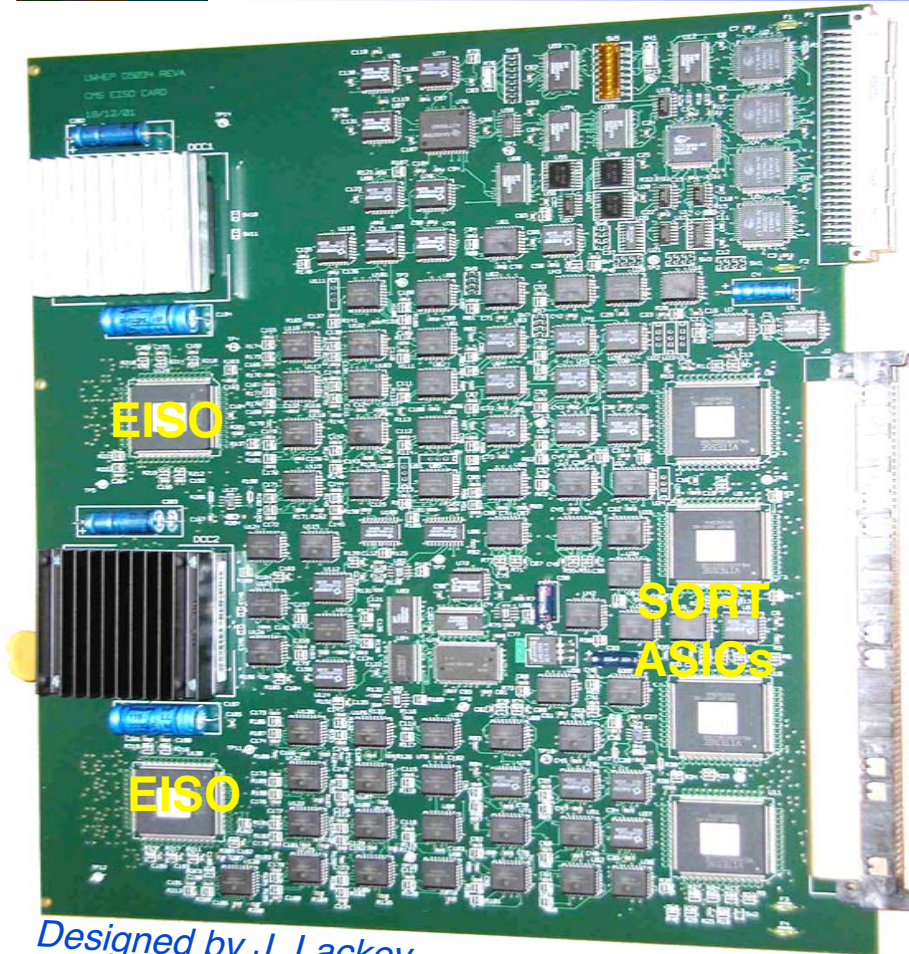
Adder ASIC: 8 inputs @ 160 MHz in 25 ns.

**BSCAN ASIC: Provides Board BSCAN &
Diff. Output @ 160 MHz to backplane**

Inter-
Crate
Sharing
w/cables



Electron Isolation Card



Designed by J. Lackey

Full featured final prototype board is validated and in production.

Processes 4x8 region @ 160 MHz

Uses Sort and EISO ASICs

- Both tested by Vitesse before delivery
- Sort ASIC used for Backplane Receive
 - Validated
- Electron Isolation ASIC
 - Mostly validated
 - neighbor data for e/ γ isolation algorithm needs add'l RCs

Lookup tables for ranking

Highest energy isolated and non-isolated e/ γ per 4x4 region sent to Jet/Summary card for sorting, forwarding to Global Cal. Trig.

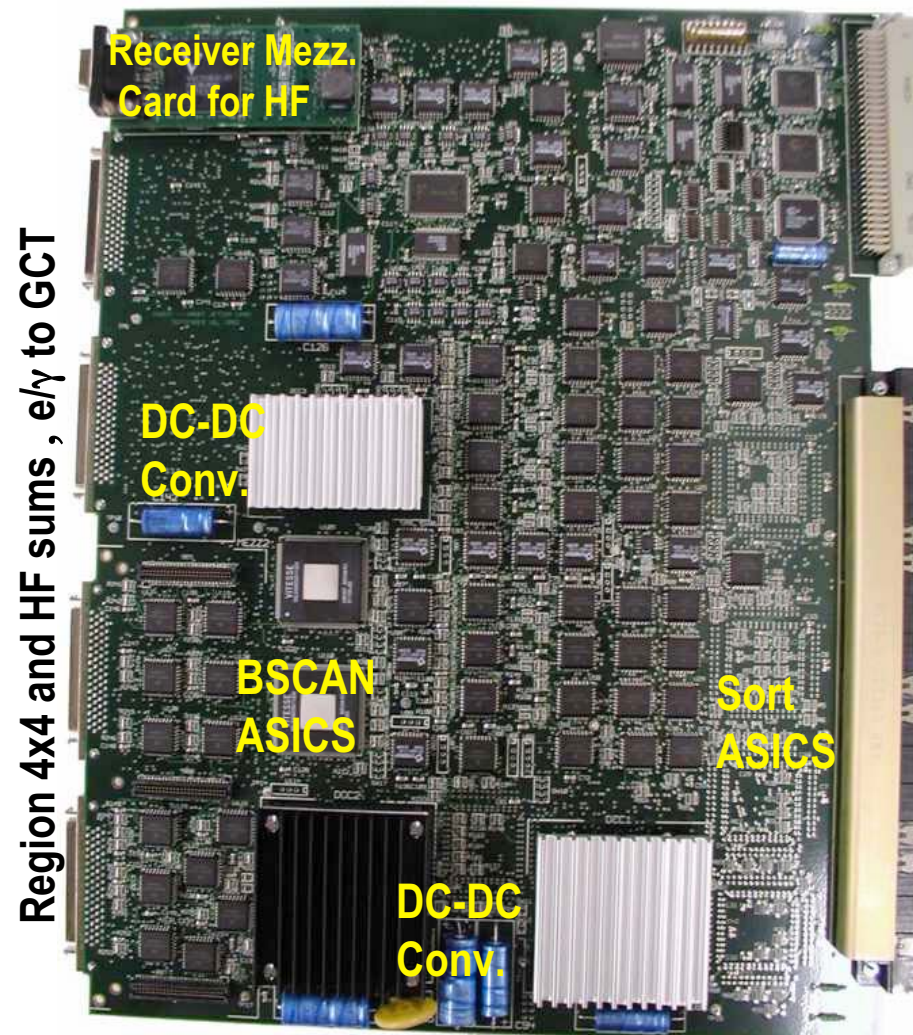


Jet/Summary Card

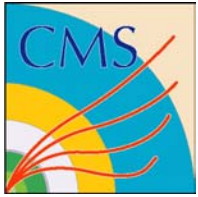


Summarizes full crate:

- **Electron/photon/muon**
 - SORT ASICs receive data on backplane and find top four e/γ (of 14 each isolated and non-isolated)
 - Threshold for muon Minimum Ionizing and Quiet bits (one per 4x4 region)
 - Data to Clustering/GCT
- **Forward Calorimeter (HF) functionality**
 - Reuses Mezzanine Card to read in data directly for inclusion in output
 - LUTs for HF regions
- **Region energies**
 - HF and 4x4 tower sums (regions) to cluster crate for central, τ , and forward jet; calculation of global quantities total and missing E_T
- **Under Test**
 - HF path checked
 - Data seen over backplane at Sort ASICs
 - 4x4 tower sum path checked to output



Designed by J. Lackey



Pre-production Prototype Testing



Hand probing of boards

- Timing of signals/clocks/resets checked
- Data paths checked

Inject known data

- Serial Test Card memories loaded and data sent on prototype cable
- Receiver Card memories loaded & known data sent through Receiver Card and over backplane to Electron Isolation and Jet/Summary cards in "test" mode

Detailed use of JTAG to check data paths on board

- Fully implemented on all boards and ASICs
 - Access JTAG through VME interface
- Use to check ASIC to ASIC data paths in detail
 - Faster location of loose connections, bad solder joints
 - Can check backplane paths as well
- Building JTAG fault library for Receiver, Electron Isolation, and Jet/Summary Cards for production testing
 - Producing code for uniform testing of cards
 - Easily handle multiple cards in a crate

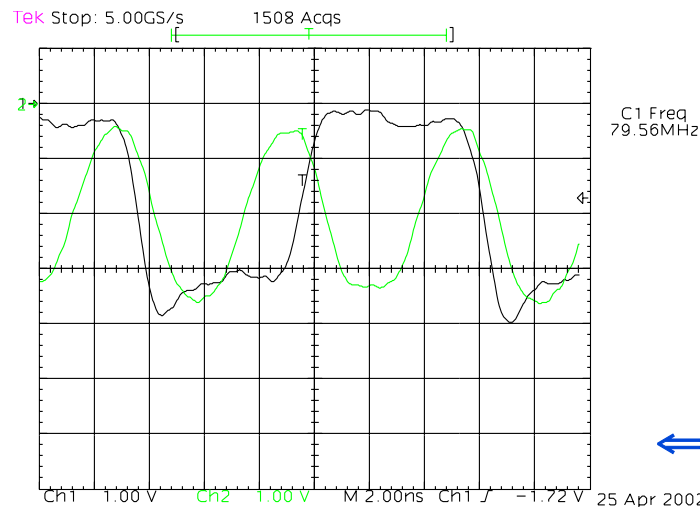
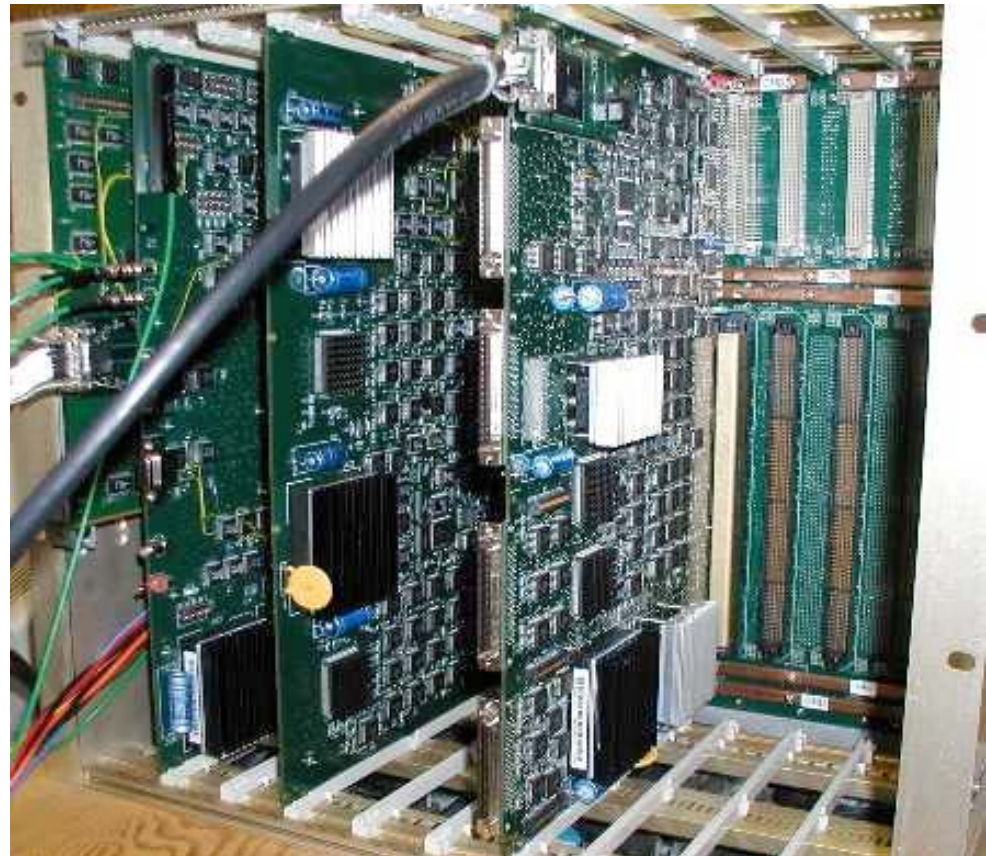


Testing Receiver, Clock, EISO, & Jet/Summary Cards, Crate, & Backplane



Crate Rear:
Loopback
Cables to
test inter-
crate data
sharing

Front: Clock, EISO, and Jet/Sum Cards with
original STC and cable to test HF data transfer
to Jet/Summary card at full speed



← **160 MHz TTL clock** with data **into 200 MHz Memories (2 ns scale)**



Conclusions



Final CMS Regional Calorimeter Trigger in production

- **Receiver Mezzanine Card**
 - Full quantity including spares manufactured
- **Receiver Card and ASICs**
 - Phase, Adder, BSCAN ASICs validated and full quantity procured
- **Electron Isolation Card and ASICs**
 - Sort ASIC validated and full quantity procured, EISO ASIC needs a full crate test to test handling of neighbor data

Completing prototype tests

- **Crate, Backplane, CCC under test**
 - Clock and Control Card nearly validated, Backplane & Crate need full complement of cards
- **Serial Link Test Card & Transmitter MC tested, produced**
 - In use with ECAL serial link electronics
- **Jet/Summary Card under test**

Goals for 2003/2004

- **Complete prototype tests, validate last EISO ASIC, Jet/Summary Card**
- **Full crate test in near future**
- **Test interface with Global Calorimeter Trigger**
- **Continue production and integration tests**