Front-end pixel chips for tracking in ALICE and particle identification in LHCb

K. Wyllie[a], G. Anelli[a], F. Bal[a], M. Burns[a], M. Campbell[a], M. Castro Carballo[a], P. Chochula[a], R. Dinapoli[a], F. Formenti[a], M. Girone[a,b], A. Guirao Elias[a], T. Gys[a], S. Jolly[b], A. Kluge[a], M. Morel[a], H. Muller[a], P. Riedler[a], D. San Segundo Bello[c], W. Snoeys[a], G. Stefanini[a], J. van Hunen[a], E. Watson[a]

[a] *CERN, Geneva, Switzerland*

[b] *Imperial College, London, UK*

[c] *NIKHEF, Amsterdam, The Netherlands.*

Front-end pixel readout chips have been designed for use in the ALICE inner tracking system and the LHCb ring-imaging Cherenkov detector. This paper presents results on the characterisation of the analog and digital circuitry of two generations of chips.

1 Introduction: The two applications, ALICE and LHCB

Pixel detectors will form an integral part of the detector systems of the Large Hadron Collider (LHC) at CERN. The ALICE experiment will use pixel detectors as part of its Inner Tracking System (ITS) [1]. Here, the pixel system will have to track particles in a high multiplicity environment close to the interaction point. The LHCb experiment has chosen the pixel Hybrid Photon Detector (HPD) as baseline photodetector in its Ring Imaging Cherenkov detector (RICH) [2]. This uses pixel sensors and readout chips to detect photo-electrons produced by Cherenkov photons. Although the requirements of the two experiments are quite different, an architecture for a pixel readout chip has been designed which, by means of a selectable mode of operation, can satisfy the needs of both systems.

The most important requirements for the pixel electronics in ALICE are the following. To minimise material, thin (200μm) silicon sensors will be used and hence signals will be $\sim$ 16,000 electrons. Tracking precision is required in the r-phi direction with a resolution of 12μm. Both the Level-1 and Level-2 triggers of ALICE will be applied to the front-end pixel chips, and data should be buffered at both these stages. Data processing and readout is done at a clock frequency of 10MHz. The chips should be tolerant to an ionising radiation dose across 10 years of 500krad, and power consumption should be minimised. Finally, the close proximity of the detector to the interaction point means that there are very tight mechanical constraints on

the electronics. A fuller description of the requirements of the ALICE ITS is given in [3].

The concept of the pixel HPD has been demonstrated with a number of prototypes [4]. Photons incident on an optical input window release a photo-electron from a photo-sensitive cathode layer deposited on the inner surface. These photo-electrons are accelerated within the HPD vacuum by a high potential and electrostatically focussed onto an anode consisting of the pixel sensor and chip. A fuller description is given in [5]. The most important specifications for the pixel electronics are the following. The accelerating voltage applied to the HPDs will be 20kV, which generates a signal of $\sim$ 5000 electrons in the pixel sensor. This can, however, be reduced to $\sim$ 2500 electrons by charge-sharing between channels. LHCb will operate with a 25ns bunch-crossing spacing which defines the time precision required to correctly identify hits. The electrostatic focussing de-magnifies an image on the input window by a factor of 5, so the 2.5mm x 2.5mm channel size required in the RICH maps to a 500μm x 500μm granularity on the pixel sensor. This channel size, however, results in a high time-averaged occupancy of up to 8% in some regions of the RICH detector. LHCb operates with a 1MHz Level-0 trigger which is applied to the pixel chips, and data must be buffered before this signal arrives. To minimise deadtime and match the bunch-crossing rate, the chips must operate with a 40MHz clock. More details of the HPDs and the RICH detectors are given in [5].

This paper describes two generations of pixel chips. The first, known as ALICE1LHCB, has been developed and tested in the last three years and is the baseline chip for ALICE. The second, known as LHCBPIX1, contains all of the features of its predecessor but with improved functionality and is the baseline choice for LHCb.

2 The ALICE1LHCB chip

The chip is fabricated in a commercial 0.25μm CMOS process using 6 metal layers. This offers the advantages of high component density and intrinsic radiation tolerance due to the thin gate oxide of the transistors. The radiation tolerance is further enhanced by the use of enclosed gates for the NMOS transistors to minimise drain-to-source leakage, and guard rings to prevent inter-component leakage and reduce the risk of electrically- or radiation-induced latch- up. All the configuration registers in the chip have been designed to improve their immunity to single-event-upset. Both the analog and digital circuitry operate with a 1.8V power supply, and the total power consumption is 800mW. The sensitive area measures 13.6mm x 12.8mm, and is divided into 8192 pixel cells of 425μm x 50μm. These pixels are arranged in 256 rows and 32 columns. The remainder of the chip consists of peripheral control logic, biasing circuitry, a JTAG serial interface and the input/output blocks, giving a total chip size of 14mm x 15mm. The chip contains around 13 million transistors.

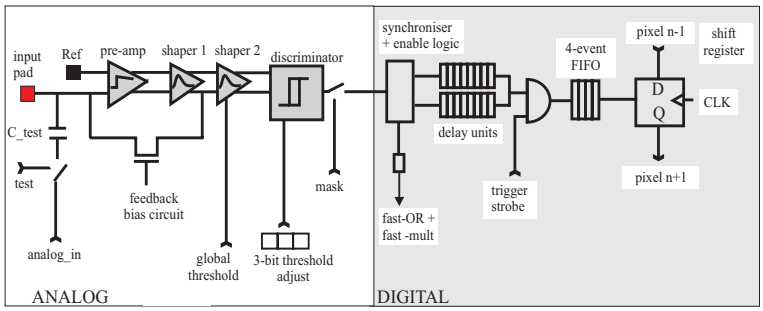

Figure 1: Schematic of the pixel cell.

The pixel cell is divided into an analog and a digital part, as shown in the schematic of Figure 1. The analog front-end is described in detail in [6]. An important feature is the use of a differential preamplifier and shaper to improve the common-mode rejection of the circuitry and to minimise the sensitivity to digital switching noise injected into the front-end through the substrate. A test input can be given to the pre-amplifier using a voltage step applied across a capacitor. The step is generated by a circuit in the chip, triggered by an external logic pulse, and transmitted to all the pixels. A discriminator compares the output of the shaper with a threshold fixed globally across the chip. In addition, each pixel contains three logic bits which can be used to adjust finely the thresholds on a pixel-to-pixel basis.

The discriminator output is fed into the digital part of the cell, described in detail in [7]. The first stage consists of two digital delay units, whose purpose is to store a hit for the duration of the trigger latency. The result of the trigger coincidence is loaded into the next-available cell of a 4-event FIFO, which acts as a multi-event buffer and de-randomiser. Data is read out by means of a flip-flop which forms one element of a column shift register. One feature of note is the use of current-starved logic to reduce the injection of switching noise from the digital circuitry into the sensitive analog front-end. Finally, there are five latches inside the cell whose contents switch on or off the test input to the front-end, mask or activate a pixel, and provide the three bits of threshold adjustment.

With the addition of some extra logic, this architecture can be used for both applications. In ALICE mode, each pixel cell acts as an individual channel and the full matrix of 256 x 32 cells is read out. In LHCb mode, eight pixels in the vertical direction are configured as a 'super-pixel' of 425μm x 400μm, which is close to the LHCb requirements of 500μm x 500μm. The discriminator outputs of the super-pixel are OR-ed together and the sixteen delay units of these eight cells are configured as an array. Four of the 4-event FIFOs are connected together to form a 16-event FIFO. This meets the buffering requirements of LHCb. The FIFO output is loaded into the flip-flop of the top pixel in the group, which bypasses the other seven during readout.

This scheme reduces the matrix to 32 x 32 cells and allows a complete event to be read out in 800ns using a 40MHz clock. The sixteen delay units are necessary for storing the large number of hits which will occur in the high occupancy regions of the RICH. Additionally, the use of the eight separate analog blocks reduces the effective occupancy seen by the front-end. If the occupancy remained high, then there would be a risk of pulse pile-up and a subsequent loss of hits. Thus, the segmentation of the front-end relaxes the requirements on the return-to-zero time of the pre-amplifier and shaper.

3 Results from ALICE1LHCB

The ALICE1LHCB chip has been characterised in detail using electrical test signals.

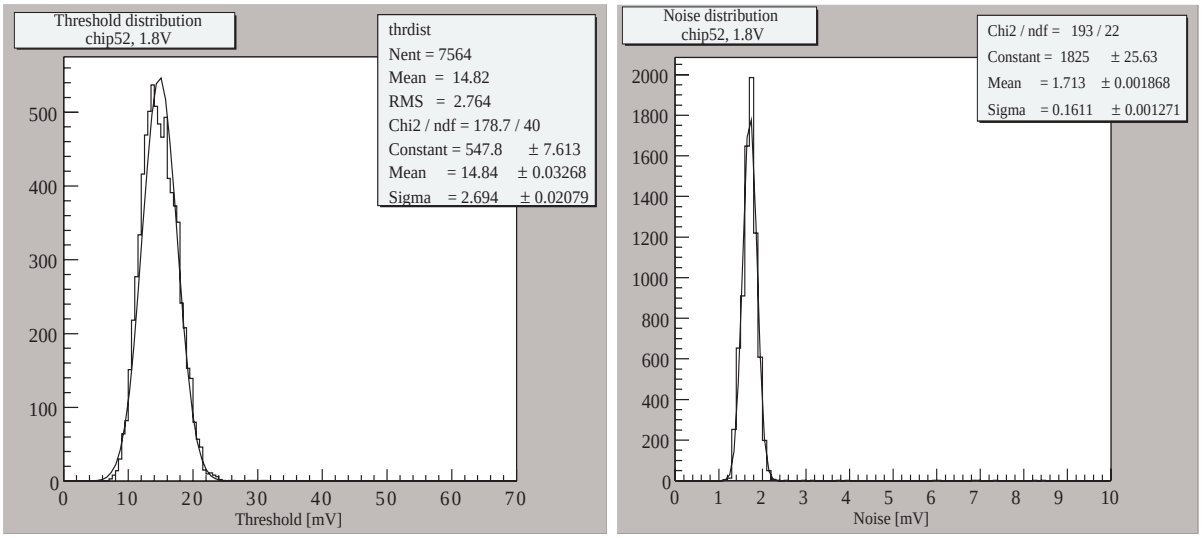

Figure 2: Threshold(left) and noise(right) distributions for ALICE1LHCB. The mean threshold of 14.8mV corresponds to $\sim$ 1000 electrons, and the RMS to $\sim$ 180 electrons. The mean noise of 1.7mV corresponds to $\sim$ 120 electrons.

The two most crucial measurements are those of the threshold behaviour and the noise. Figure 2 shows typical threshold and noise distributions measured across all 8192 channels of a chip. The measurements were made whilst operating at the lowest possible threshold where noise hits occur at a negligible rate. Using a calibration factor derived from subsequent measurements on assemblies of chip and sensor with radioactive sources, the mean of the threshold distribution corresponds to $\sim$ 1000 electrons with an RMS spread of $\sim$ 180 electrons. This represents a uniform

sensitivity for a low global level of threshold and is well within the requirements of both experiments. The mean noise across the pixels is $\sim$ 120 electrons, again within specification.

Tests were also carried out to assess the tolerance of the chip to radiation, both total dose and single event effects. These are described in [8], and indicate a satisfactory resistance to radiation levels in excess of those predicted for the two experiments.

The digital circuitry of the chip functions correctly, and meets the ALICE requirement of operating at a 10MHz clock frequency. However, this frequency is limited to a maximum of 15MHz, and therefore does not meet the LHCb specification of 40MHz. Experimental evidence suggested that this limit was due to inadequate power supply distribution to the digital blocks. The space available for routing the supplies was severely restricted by the strong constraints on the physical size of the chip, in particular the insensitive peripheral area. A model of the parasitic components of the digital power supply distribution was constructed and simulated, and confirmed the experimental observations.

A further limitation on the performance of ALICE1LHCB was a systematic variation in the amplitude of the calibration pulse distributed to the pixels. This was due to the parasitic components of the long lines used to distribute the signals. An accurate calibration using these test signals was therefore very difficult to make, and was only achieved after chips were bump-bonded to sensors and could be tested with radiaoactive sources.

The excellent analog performance of the chip and its functionality at 10MHz clock frequency has led to its use in the various protoyping stages of the ALICE detector system. Numerous bump-bonded assemblies, both with single and multiple chips, have been constructed and results are described in [3].

4 The LHCBPIX1 chip

A second generation of the chip has been designed with the aim of improved functionality, in particular the 40MHz clock frequency needed by LHCb. In this case, the mechanical constraints imposed by the ALICE requirements were considerably relaxed. This extra space was used in a number of different ways. The pixels were stretched to cover an area of 500μm x 62.5μm, resulting in a super-pixel of 500μm x 500μm. The extra space within the superpixel was filled with decoupling capacitors and power routing. Additional peripheral space was added to the top of the pixel matrix and used for extra power routing to the pixel columns and a second row of bond pads. It also contains the calibration circuitry, which is now divided into a distribution block per pixel column to reduce the effect of parasitics. This re-sizing results in a sensitive area of 16mm x 16mm and an overall chip size of 21mm x 16mm.

5 Results from LHCBPIX1

LHCBPIX1 maintains the good analog performance demonstrated by ALICE1LHCB. This is illustrated by Figure 3 which shows the threshold and noise distributions of the pixels. The minimum threshold and RMS spread are still within the specification.

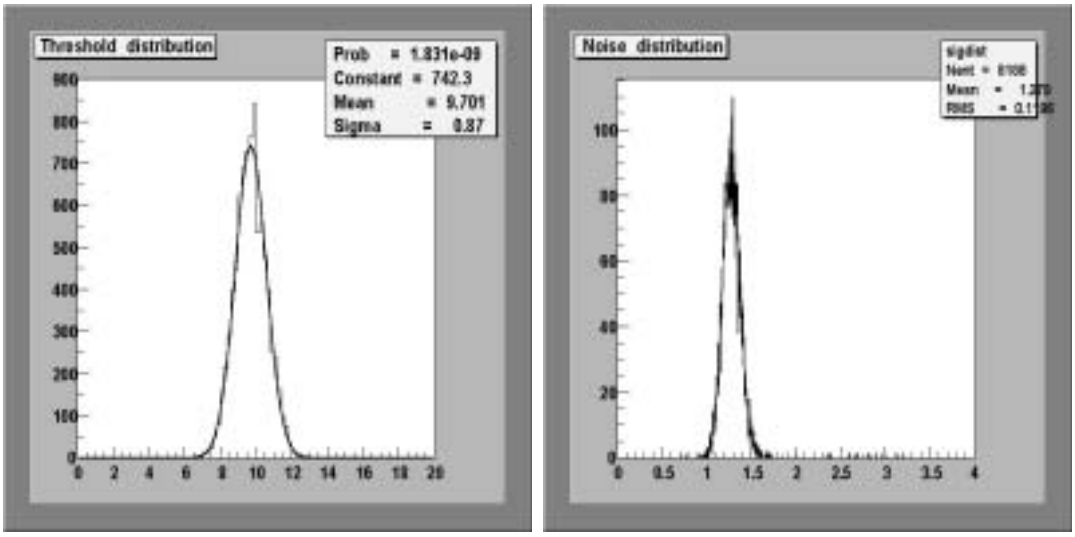

Figure 3: Threshold(left) and noise(right) distributions for LHCBPIX1. The mean threshold of 9.7mV corresponds to $\sim$ 970 electrons, and the RMS to $\sim$ 90 electrons. The mean noise of 1.3mV corresponds to $\sim$ 130 electrons.

Figure 4 shows one of the single-ended outputs of the differential shaper, measured from a test pixel and for an input charge of 5000 electrons. The rise time meets the specification of 25ns and the pulse has fully recovered less than 100ns after the peak, a feature which is important in the high occupancy region of the RICH. The chip is fully functional at 40MHz without any deterioration in the analog behaviour. This is true also when running in a deadtime-free mode where data is processed by the front-end while the previous event is being read out. The calibration circuitry has been improved as illustrated by Figure 5 which compares the geographical threshold distribution between ALICE1LHCB and LHCBPIX1. The systematic left-to-right trend in ALICE1LHCB has been corrected in LHCBPIX1. The increase in clock frequency is reflected in a higher power consumption of 1.7W at 40MHz.

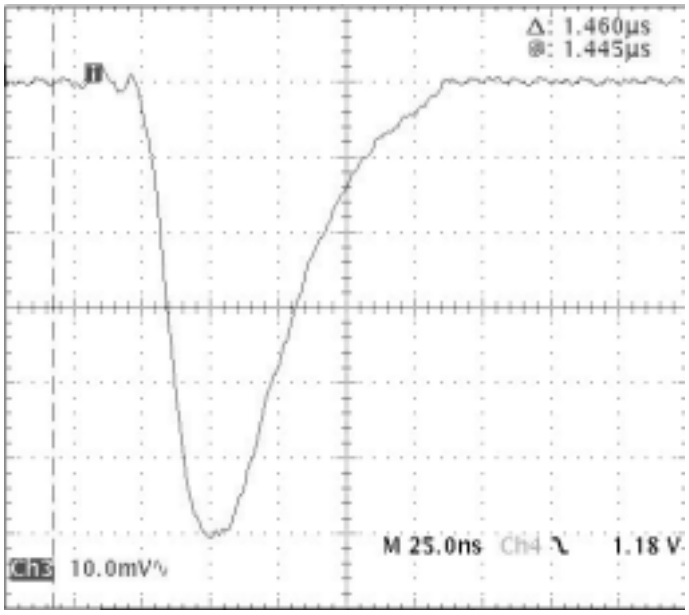

Figure 4: Scope display of the single-ended outputs of the shaper, measured from a test pixel. The input charge is 5000 electrons and the time base is 25ns per box.

6 Conclusions and Future Plans

A chip architecture was designed to meet the requirements of two applications, the ALICE inner tracking system and the LHCb ring-imaging Cherenkov detector. This has been implemented in two generations of chip. The first, ALICE1LHCB, displayed a good analog performance and digital functionality at 10MHz clock frequency. It is the baseline choice for equipping the ALICE detector and is already in use throughout the different stages of the detector prototyping. ALICE1LHCB is also currently being encapsulated within prototype HPDs for tests in 2003. Poor power supply distribution limited its maximum operational clock frequency and hence a second generation of chip, LHCBPIX1, was designed to meet the LHCb specification of 40MHz. This it has achieved whilst maintaining the good analog performance of its predecessor. Bump-bonding to sensors is foreseen for the beginning of 2003, followed by encapsulation within HPDs.

References

[1] ALICE Technical Design Report of the Inner Tracking System (ITS), CERN/LHCC 99-12, June 1999.

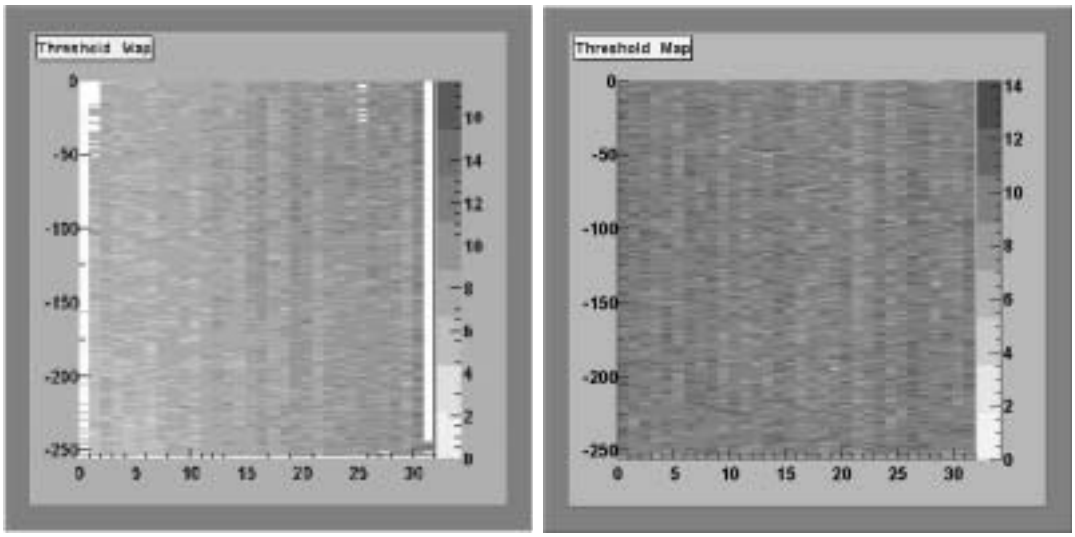

Figure 5: Threshold maps for ALICE1LHCB(left) and LHCBPIX1(right). The x-direction is the column number, the y-direction the row number. The greyscale shading represents the threshold in mV. Columns 0 and 31 in the ALICE1LHCB measurement are dead due to an artifact of the readout system which was later corrected.

[2] LHCb RICH Technical Design Report, CERN/LHCC 2000-037, September 2000.

[3] P. Riedler, The ALICE Pixel Detector, these proceedings.

[4] M. Alemi et al., Nucl. Instr. and Meth. A 449 (2000) 48.

[5] K. Wyllie, Pixel Hybrid Photon Detectors (HPDs) for the LHCb RICH system, these proceedings.

[6] R. Dinapoli et al., An analog front-end in standard 0.25μm CMOS for silicon pixel detectors in ALICE and LHCb, Proceeding of the Sixth Workshop on Electronics for LHC Experiments, Cracow, Poland, 11-15 Sept. 2000.

[7] K. Wyllie et al., A pixel readout chip for tracking at ALICE and particle identification at LHCb, Proceedings of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, CO, USA, 20-24 Sept. 1999.

[8] J. van Hunen et al., Irradiation and SPS beam tests of the Alice1LHCb pixel chip, Proceedings of the Seventh Workshop on Electronics for LHC Experiments, Stockholm, Sweden, 10-14 Sept. 2001.