

# A Silicon Pixel Detector

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## 1. Introduction

Pixelated silicon detectors will be used in the next generation experiments at the LHC. The CMS detector will provide 2 and 3 hit information near the beam interaction region  $0.0 < \eta < 2.5$  allowing (1) reconstruction of secondary vertices from b-decays, (2) providing seed tracks for global tracking, (3) and may be used in L2/3 triggering. The utility of these detectors for efficient tracking and reconstruction of highly complex decays involving Higgs and supersymmetric particles can not be denied. The inner pixel detector will be exposed to radiation as high as  $5 \times 10^{14} \text{cm}^{-2} \text{s}^{-1}$  equivalent 1MeV neutron flux, making for a difficult design. The success of the LHC experiments may well depend on how well these first generation detectors perform. [CERN LHCC 98-6, CMS TDR 5]

In Figure 1 we show a sensor and readout chip bump bonded together. The silicon bulk thicknesses are typically  $(250-300) \mu\text{m}$ . Under each pixel diode a solder bump connects the sensor to a readout input. On the periphery of the readout chip are the data lines, control logic, buffers, and bias voltage. In total the radiation hard CMOS design contains about 400,000 transistors.

The channel counts for these detectors at the LHC is large, containing approximately 50 Mpixels. A formidable challenge lies ahead in areas of (1) sensor layout and radiation hardness, (2) design of a radiation hard readout chip, (3) interconnects and busing, (4) and mechanical/cooling issues.

## 2. Sensor

The harsh radiation environment within 10's of cm of the interaction region will quickly degrade the performance and lifetime of the silicon sensor. Silicon sensors of  $n^+$  implants on n-bulk and metallized p-backside, a double sided fabrication, are being used. After a fluence of order  $10^{12} \text{cm}^{-2}$  the n-bulk will type-invert to begin forming an effective p-substrate. The diode is now

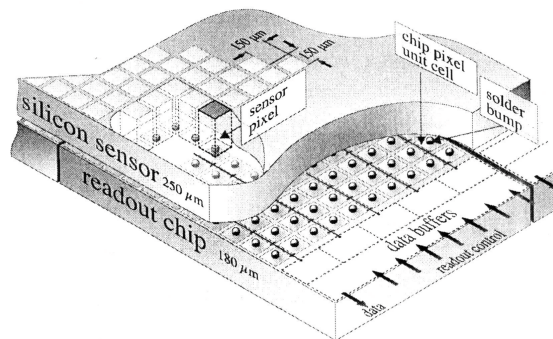


Figure 1: Single pixel detector unit.

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$n^+$  pixel implant on p-substrate. Choice of this double-sided fabrication for operational reasons will lead to low somewhat lower chip yields.

On the n-side of the wafer the charge collecting pixels are defined by n-implants surrounded by isolating p-stop rings. The design of these p-stops are critical to providing pixel-to-pixel isolation and preventing leakage currents. A further charging problems may develop if a pixel is not connected to its readout amplifier. The p-stop design must compensate and dissipate charge build-ups.

On the p-backside of the wafer a diode is implanted with appropriate metallization with several micron passivation layer. Here the sensor is biased by typically (300-500)V and care must be taken in isolating edge of the substrate from readout chip. A series of guard rings must drop the p-side bias voltage to readout chip potential, avoiding any possible breakdown.

We presently believe that oxygenated n-type silicon provides the most radiation hard bulk material for sensor production. Studies of the radiation hardness properties of silicon are ongoing. [ NIM A426 (1999) 1-15]

### 3. Readout Chip

The readout chip is designed in radiation hard CMOS, 1/4 micron SOI techniques provide the most radiation hard solutions. The superior intrinsic device isolation properties of SOI is very advantageous to the mixed analogue/digital readout architecture. The increased noise characteristics of SOI over bulk CMOS is not be a problem for the Si-pixel device in comparison to a much larger capacitance Si-strip detector. The total equivalent noise charge of the analogue front end will be  $\leq 500$  e's even after years of LHC running.

The CMS pixel readout chip is a 53x52 array of readout cells, Figure 2. Each cell contain a a bonding area attached to the analogue low noise pre-amp and a digital readout block in extremely close proximity. As many digital functions are moved to the periphery as possible to decongest and simplify the design. The chip will operate run with a pixel threshold of about 2500 electrons  $> 5\sigma$  over noise. The design generates about 40 $\mu$ W heat per pixel.

The layout of the pixels is a back-to-back configuration with a common signal bus, allowing for a 26 double-column readout scheme. A token scan is performed up-and-down each double-column searching for hit pixels above threshold. A common pixel chip threshold is set by DAC register with 3-bit trim for individual threshold adjustment. Any data is transferred to the periphery in less than 8 bunch crossings (200ns) and can be stored in a 24 deep buffer. In this time there is typically  $< 10^{-3}$  chance of a second hit. Upon receiving a trigger decision (3.2 $\mu$ s latency) the analogue hits are read out through an optical link.

Single event upset (SEU) in the high radiation environment will occur in the digital and analogue sections possibly corrupting data levels, but more importantly upsetting data flow and control electronics, as in DAC-set thresholds. Estimates are as high as  $10^{-6}$  upset per bit-s near the inner pixel tracker. Constant resetting and DAC refreshing of the system under design consideration.

The readout chip design is a difficult task taking many small submissions till the final goals are reached. It has evolved out from the design of the inner pixel units, then to the periphery logic and control. The resultant yield of good readout chips ( as low as 30% believable) fabricated per wafer is an important issue greatly affecting costing.

### 4. Bump Bonding and High Density Interconnects

As mentioned previously the  $n^+$  side of the sensors are bump bonded to the readout chip with little margin of error due to the small pad sizes. The solder bumps are approximately 25  $\mu$ m ball of Indium or Pb-Sn solder, still under investigation. Two methods of bonding are under consideration. (1) In Indium bonding the readout chip and sensor surfaces are prepared for metal evaporation, Figure 3. The sensor and readout chip are then carefully aligned in a flip-chip bonder and then mechanically pressed to form the bond. This process is in favor with low bond failure rates ( $< 10^{-3}$ ) expected. (2) A reflow technique can also be used, in which the the pads are prepared for soldering in a somewhat complex under-bump metallization stage, then solder electroplated on. The chips are aligned and re-heated ( 180°C). The technique is self-aligning to

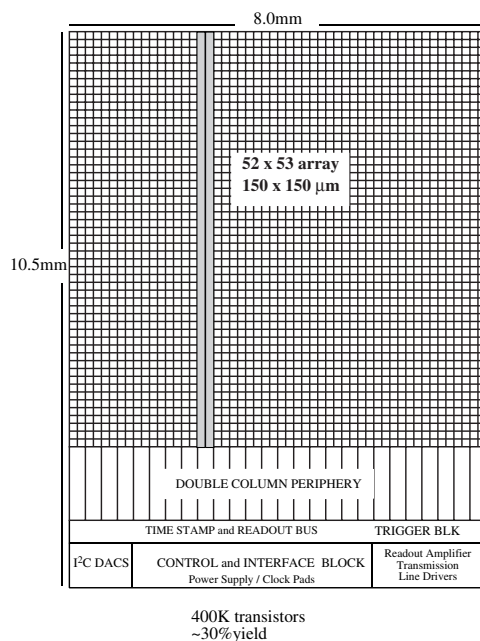


Figure 2: Pixel readout chip.

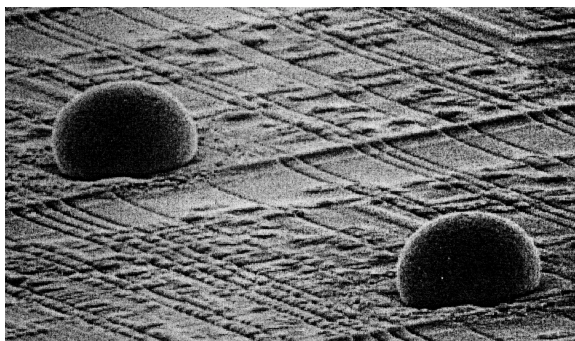


Figure 3: Readout chip with bumps prepared at the Paul Scherrer Institute.

a great degree, because of bonding force of reflow and results in high strength and very reliable bonds common to the chip packaging industry.

The pixel detectors are packaged to form readout+sensor units. The units are glued to a hybrid circuit for placement on the detector. The p-side of the readout unit is glued to a very high density interconnect (VHDI), multilayer copper-on-Kapton flex mounted on to a Si substrate with a matching CTE epoxy. An number of wire bonds must be made to the sensor and readout chip providing bias and signal connections. The VHDI is then mounted to a copper-on-Kapton flex HDI of less complexity and additional wire bonds made. This 2-phase strategy is seen to pay off in the checking and debugging of the individual detector pieces during fabrication steps and then to the final detector unit.

## 5. Mechanical and Cooling

The total material budget of the Si-pixel system can be costly due to the high density of components, busing and chip stacking. The readout chip( 300 $\mu\text{m}$ ), sensor ( 300 $\mu\text{m}$ ), Si substrate ( 300 $\mu\text{m}$ ) and amount to a full 1mm of Si. Adding in the VHDI/HDI kapton flex we come to  $X/X_0 \approx (.010 - .015)$  effective radiation length of material. Back-side thinning of the readout chip may be necessary if 8-inch ( 750 $\mu\text{m}$  thick) wafer technology is used

An additional material budget is imposed by the support structure and cooling. At  $40\text{--}50\mu\text{W}$  per pixels a few tens of kW of power must be removed from the full detectors. Evaporative cooling techniques have not been realized and presently conventional liquid fluorocarbon cooling is envisaged. Some additional savings in material budget can be made with the use of carbon-fiber structures and beryllium, but will heighten the overall cost over more standard eg. aluminium. Estimates of the contributions from support and cooling structures raise the total material budget  $X/X_0 \approx (.018\text{--}.025)$  per tracking layer.

Of course costing and catastrophic failures must be weighed in with material budget concerns and all structural materials, fabrication techniques, and coolants must be carefully chosen and tested for long term radiation properties and reliability.

### Acknowledgments

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