CMOS Pixels for a Vertex Detector at a Future Linear Collider

Grzegorz Deptuch,* Yuri Gornushkin,† and Marc Winter
Institut de Recherches Subatomiques (IReS), Strasbourg
Gilles Claus and Wojciech Dulinski
Laboratoire d'Electronique et de Systèmes Instrumentaux (LEPSI), Strasbourg

Monolithic Active Pixels Sensors (MAPS) have emerged recently as well suited to provide charged particle detection with high signal-to-noise ratio, translating into a detection efficiency close to 100% and excellent spatial resolution ($\sim 1.5\,\mu$m). They respond therefore to demands for a thin and low power dissipating device at a future e^+e^- linear collider. The performances of the first small scale prototypes, called MIMOSA[1], were evaluated with a 120 GeV/c π^- beam at the CERN-SPS, and the results obtained are discussed in the paper. The preliminary results of radiation hardness tests, where the prototypes were exposed to 10 keV photons and 30 MeV/c protons, are also presented and the first plans for a wafer-scale detector prototype are drawn.

1. introduction

Monolithic Active Pixel Sensors (MAPS) constitute a novel technique for silicon position sensitive detectors, which allows integrating on the same substrate the detector element and the read-out electronics. The device architecture resembles CMOS cameras, a recent alternative for the widely used Charged Coupled Devices (CCD) in digital photography and video applications [1]. The basic idea of MAPSs optimised for charged particle detection consists in integrating a sensor in a twin-well process, where an n-well/p-epi layer diode is used for charge collection and the read-out electronics is placed in a p-well over the active detector volume. The charge liberated in a thin and low resistivity (doped up to the level of $10^{15}\,cm^{-3}$) epitaxial layer is collected mainly through thermal diffusion within a typical time of a few tens of nanosecond [2]. Because of the three orders of magnitude between the doping levels of the p-epitaxial layer and of the p^+ well and p^{++} substrate, potential barriers exist at the region boundaries, confining the excess electrons to the epitaxial layer volume. The new detector can be fabricated using a standard, cost effective and easily available CMOS process. In order to validate the presented ideas, four prototype chips[2] with pixel arrays of slightly different design were fabricated. Two prototypes have been fully characterised and the remaining two are currently under tests.

2. Tests with charged particle beam

A detailed description of the MIMOSA I and II chips can be found in [3]. In the current section, the main parameters of the tested chips are recalled. Both chips consist of several independent arrays of active pixels, where the latter have slightly different designs. The array elements are addressed consecutively by a set of shift registers, for a serial read-out, and the analogue signal is transmitted to an external Data Acquisition System (DAS) equipped with a 12 bit resolution Analogue-to-Digital Converter (ADC) unit. Each matrix consists of 64×64, 20×20μm^2 wide pixels. The epitaxial layer thickness amounts to 14 μm and less than 5 μm in the case of MIMOSA I and II, respectively. Both MIMOSA chips were tested with a π^- beam of 120 GeV/c at the CERN-SPS. A beam telescope [4] of 8 planes of high precision silicon strip detectors, grouped in pairs and providing two orthogonal coordinates, was used to determine the intersection point of the particle

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*corresponding author: deptuch@lepsi.in2p3.fr; visitor from: Dep. of Electronics UMM, Cracow
†visitor from: the Joint Institute for Nuclear Research, Dubna, Russian Federation.
[1]standing for *Minimum Ionising MOS Active pixel sensor.*
[2]The MIMOSA chips I, II, III, IV were fabricated in 0.6 μm, 0.35 μm, 0.25 μm and 0.35 μm (without epitaxial layer) processes, respectively.

Table I Summary of particle tracking performances of MIMOSA I and II. The noise is shown after off-line CDS processing and pedestal subtraction.

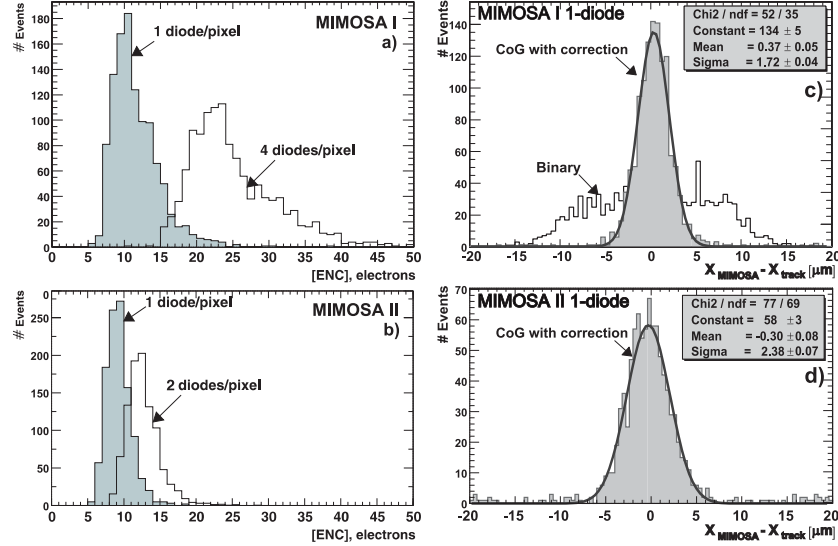| Fabricated prototype	Single pixel noise [e^-ENC]	3x3 cluster mean collected charge [$\#e^-$]	Spatial resolution [μm]	Detection efficiency [%]
MIMOSA I (1-diode)	12-14	896	1.4±0.1	99.5±0.2
MIMOSA I (4-diode)	25-30	1155	2.1±0.1	99.2±0.2
MIMOSA II (1-diode)	9-12	315	2.2±0.1	98.5±0.3

Figure 1: Distribution of Equivalent Noise Charge for two configurations of MIMOSA I -a) and II -b). Residual distribution between the track intersection (X_{track}) from the telescope and the reconstructed impact position (X_{MIMOSA}) from the sensor response, for 1 diode pixel configurations of MIMOSA I -c) and II -d).

track with the MIMOSA plane. The precision on the extrapolated intersection point was within $\sim 1\,\mu$m. A pair of small scintillator counters provided the trigger for the DAS, based on a VME/OS-9 processor. MIMOSA I and II were read-out with clock cycles of 2.5 MHz and 5 MHz, respectively. The off-line signal processing started with Correlated Double Sampling (CDS) [5] to eliminate correlated noise components, i.e. mainly kTC noise due to the pixel reset performed after each trigger. The remaining noise entering the signal-to-noise ratio (S/N) calculus was estimated from the first 250 events of each run. The sensor spatial resolution was determined by comparing the track intersection derived from the telescope information with the impact position calculated from the sensor response. The latter was taken either as a the centre of the seed pixel (binary resolution) or as the centre-of-gravity of the distribution of the charges collected within a 3×3 pixel cluster. A detailed summary of the results obtained with this procedure is presented in table I and figure 1.

3. preliminary radiation hardness results

MIMOSA I and II were irradiated with 30 MeV/c protons and 10 keV X-ray photons. The study of irradiation effects was based on the position of the 5.9 keV peak from an ^{55}Fe source. Significant effects were only setting in above 10^{11}p/cm^2. A diode leakage current rise of about a factor of 5 and a 40% charge loss are seen after about 5×10^{11}p/cm^2. The test data summary for the MIMOSA II chip (which obeys the rules for radiation tolerant submicron design) is given in table II. Studies with photon irradiation show an increase of leakage currents by more than an order of magnitude and 40% charge loss for doses of 10 keV X-ray photons around 600 kRad. Although the observed radiation tolerance should be sufficient for a future linear collider environment, the fact that effects are seen below the level at which LHC sub-micron electronics shows irradiation

Table II Preliminary results of radiation hardness tests with a 30 MeV/c proton flux. The leakage current is measured as a voltage drop, which corresponds to the combination of leakage currents of the diode and of the reset transistor.

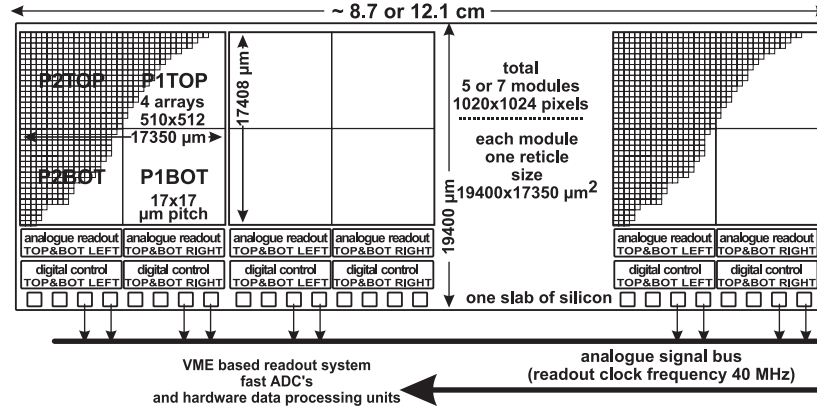| Fabricated prototype	Increase of leakage current after $2.5 \times 10^{11} p/cm^2$	Increase of leakage current after $5 \times 10^{11} p/cm^2$	Charge loss of seed pixel after $2.5 \times 10^{11} p/cm^2$	Charge loss of seed pixel after $5 \times 10^{11} p/cm^2$
MIMOSA II (1-diode)	2.2	4.6	20%	47%
MIMOSA II (2-diode)	2.6	6.1	15%	36%

Figure 2: Schematic layout of the MIMOSA V prototype.

degradation calls for further investigation. Moreover, tests with pure neutron sources are being made, in order to distinguish between ionisisation and bulk damage effects.

4. Conclusions and perspectives: wafer scale CMOS pixel detector

The beam tests demonstrate that the detection technique using MAPS devices works efficiently and provides excellent tracking parameters. This makes them an attractive candidate for vertex detectors in future particle physics experiments, as well as in other domains requiring charged particle imaging. Several requirements for a vertex detector at a future linear collider experiment are already fulfilled with the sensor prototypes tested. Some other requirements are still to be met. They concern mainly increasing the read-out speed with possible on-line data sparsification and device thinning. The radiation hardness issue needs further investigation to understand the damage processes. However, the radiation test results already obtained are satisfactory, offering a security margin at least one order of magnitude above the radiation doses predicted at future linear colliders (TESLA specifications: 100 kRad for the ionising dose and a neutron fluence of 5×10^9 integrated over five years of operation). The performances obtained with small prototypes need to be reproduced with a large (wafer-scale) device, such as the MIMOSA V chip, shown in figure 2. Its basic unit is a one reticle size ($19400 \times 17350 \, \mu m^2$) chip made of 4 arrays of 510×512 active pixels laid down with a pitch of $17 \, \mu m$. This structure is repeated 5 or 7 times in one direction on the wafer, with an interface band of $100 \, \mu m$, resulting in of 8.7 cm or 12.1 cm long slabs. The read-out electronics is placed at the bottom of each unit, occupying a band of ~ 2 mm width. The chip is equipped with some read-out options allowing fast array scanning where only each third pixel is read-out, or summing signals from three consecutive pixels. The serial analogue output of the chip will be read by a VME based DAS equipped with an on-line processing unit now under test. The device will be used for yield studies as well as for testing thinning procedures.

The detection principle described in this paper is commonly used [6] for consumer imaging devices driving the technological development of the processes with epitaxial layer and ensuring future long-term access.

References

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