AN IMPROVED CONTROL MEMORY
FOR THE PDP9 COMPUTER

A review of the maintenance record of our PDP-9 computer revealed that 80% of the CPU failures were caused by intermittent problems in a single module, namely, the control memory MC09 (also referred to as G920). This module has been replaced three times in the past, but these replacement units as well as the original unit all showed marginal performance and were all sensitive to mechanical vibrations. An improved module was built and is described here. The major change is in the use of single pieces of small toroid cores instead of pairs of large E-cores, as were used in the original design.

The control memory is a quadruple-height module containing a 64-word by 36-bit read only memory. There are 64 word lines, each threaded in a different pattern through 36 ferromagnetic cores. Upon a read request, one of the word lines is driven by an 8x8 current source and current sink address matrix (G210 modules), and the induced voltage on the secondary windings of the ferromagnetic cores are gated and latched by sense flip-flops (B213 modules). Thus the state of these 36 flip-flops is determined by the pattern into which the currently addressed word line is threaded.
A schematic of the improved module is shown in Figure 1. The word lines are shown as horizontal lines. The secondary windings, or sense lines, are shown as vertical lines. A diagonal dash at their intersection indicates that the particular word line is threaded through that particular core. The directions of the windings are such that positive pulses are induced on the sense lines when the word lines are pulsed in the forward directions of the diodes. The sense lines are biased to \(-3\) V (logic 0) and will go to 0 V (logic 1) when pulsed. The components used in the circuit are listed in Table 1. The component layout is almost identical with the original module with the exception of the following:

(a) All the hardware that was used to hold the E-core is eliminated. The word lines and the sense lines are enough to hold the small toroid in position.

(b) The diodes at the CMP end of each word line are replaced by resistors R4.

(c) The number of diodes in the bias reference is increased from 2 to 4.

(d) The resistors that were used to pull the CMP end of each word line to \(-15\) V are eliminated.
(e) The resistors that were used to pull the CMP end of each word line to ground are connected to -15 V instead.

(f) There are 8 additional resistors $R_5$ at the CMP end.

This improved module has been tested on the PDP-9 for five hundred hours with MAINDEC diagnostic programs. The sense line outputs are also checked with a scope while the CPU is looping on all instructions (including EAE) and all console key functions. Figure 2(a) and (b) show two typical sense line output pulses together with the strobe pulses which are used to gate the sense flip-flops. Figure 2(c) and (d) show the same signals when the original MC09 rather than the improved version is used on the PDP-3 computer. The higher signal-to-noise ratio obtained on the improved module is quite evident in these photographs. It is believed that the intermittent problems in the original module are caused by the air gaps in the E-core pairs, and are aggravated by the low signal-to-noise ratio.
Table 1. List of Components

1. Board: Two Digital Equipment Corp. Flip Chip W999 blank double-height modules bolted together. Pin designations on the board are enclosed in parentheses in Fig. 1.

2. Capacitors:
   - C1: 3.5\mu F 18V electrolytic
   - C2: 0.1\mu F 25V ceramic
   - C3: 7.\mu F 6V electrolytic
   - C4: 0.1\mu F 25V ceramic, 6 required

3. Diodes: IN3064, 59 required

4. Resistors: 1/4W 5% carbon composite
   - R1: 150\Omega
   - R2: 1500\Omega
   - R3: 470\Omega, 36 required
   - R4: different value for each word line
     short for 05
     10\Omega for 22, 56
     15\Omega for 42, 53, 55, 66, 73, 75
     20\Omega for 03, 14, 41, 65, 67, 72
     27\Omega for 01, 02, 06, 07, 21, 23, 25, 32, 50, 51,
     52, 70, 71, 74, 77
     30\Omega for 11, 12, 13, 16, 34, 36, 43, 57, 60, 61,
     62, 64
     36\Omega for 10, 24, 26, 30, 37, 54, 63
     39\Omega for 17, 20, 31, 33, 40
     51\Omega for 76
     open for 00, 04, 15, 27, 35, 44, 45, 46, 47
   - R5: 33\Omega, 8 required
   - R6: 470\Omega, 8 required

5. Transformers: 36 required
   - (a) Core: Ferroxcube toroid core 265T125-3E2A
   - (b) Primary: 30-130 Kynar wire, one turn (thread through) for cores marked with a slash on Fig. 1, and zero turns (bypass) for cores not marked.
   - (c) Secondary: 30-130 Kynar wire, six turns in the direction which will induce positive pulse at CMSL when the word lines are pulsed in the forward direction of the diodes.

6. Transistor: 2N3060
Fig. 2 Scope Traces of MC09 Sense Line Output
Horizontal: 50 ns/sq.
Vertical: 3 V/sq. Center line is -3 V for top traces and 0 V for lower traces.
Top traces: CM strobe pulses
Bottom traces: Sense line output showing a logic 1 followed by a logic 0.
(a) Sense line 04 of improved MC09
(b) Sense line 30 of improved MC09
(c) Sense line 04 of original MC09
(d) Sense line 30 of original MC09