SPS High Bandwidth Transverse Feedback System Testing and Setup

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1. **Nov. 26, 2012** - The feedback channel arrived to CERN and the equipment was unpacked. Care was taken to remove all popcorn packing material from inside the feedback chassis. We blew compressed air inside the box to remove any small pieces of packing material. The equipment was transported to the SPS Faraday cage.
2. Initial powering of system and interfacing with the PC via USB:
 - (a) We had issues interfacing the feedback system with the PC via USB.
 - (b) A file needed to be configured with identification numbers of the hardware for interface. The ID numbers were found by exploring the hardware properties on the PC:
 - i. VID_04B4
 - ii. PID_8613
 - (c) The file cyusb.inf (size 3 kB) was modified with these ID numbers.
 - (d) Location of file on PC: C:\CYPRESS\CYPRESS SUITE USB 3.4.7\DRIVER\BIN\WLH\X64\CYUSB.INF
3. Check input signal levels:
 - (a) Synchronization clock @ 1.6 GHz: $2.3 V_{pp} = 11 \text{ dBm}$
 - (b) Revolution fiducial trigger: 5 ns width, 1 V amplitude
 - i. Note: This was changed on Thursday, 11/29. No note on the new level.
 - ii. Recheck this level during the Jan 2013 MD
 - (c) Injection trigger: Attenuated by 6 dB at input of feedback chassis. No recorded level.
4. Initial test of the feedback excitation function
 - (a) Set strobes to monitor the fiducial (#4) and injection (#3) triggers.
 - (b) Test excite mode. Had some trouble with this function initially because of a software bug. The SW TRIGGER toggle on the CSRS panel would not untoggle. Some observations while diagnosing the issue:
 - i. For sine 200 MHz signal over 16 samples (32 total samples with 16 zero samples), two sine signals were observed separated by 16 zeros. The EXCITE RETRIGGER MODE was set to SINGLE mode during this time. The two sine signal behavior was not observed when in RETRIGGER mode.
 - ii. During this time, we realized the SW TRIGGER was enabled (indicator yellow). We could not untoggle it. In essence this toggle should be non latching, it should be clicked once to trigger then fall back to its original state. The excitation system software works this manner.

Figure 1: Several screen captures taken when trying to diagnose the SW TRIGGER issue. Notice that the excitation signal (Ch3) is played out regardless of the injection trigger. The excitation file has 10 warmup turns (no signal) followed by 10 sine 200 MHz turns.

- iii. Upon a power cycle of the system, the SW TRIGGER returned to its default state (untoggled). We noted to not touch this, since the state could not be changed back to the default without cycling power. With this untoggled, the two sine signal disappeared described above disappeared.
 - iv. The signal played out regardless if there was an injection trigger, which make sense since the SW TRIGGER was always enabled. The signal played out continuously, repeating once the end of the .cfg file was reached, which is similar to how the system should run in RETRIGGER mode. Figure 1 shows several scope screenshots of the behavior. Ch2: injection strobe, Ch3: excitation signal, Ch4: fiducial strobe.
- (c) Jeff and John D were able to temporarily fix the toggle issue with a new version of the control software, which was implemented on 11/27.
 - (d) After the reboot we checked the trigger thresholds
 - i. In the TRIGGER CONTROL window, the trigger thresholds can be set individually for the injection and fiducial, however upon refreshing the screen, the last input value will appear regardless of whether fiducial or injection is selected.
 - ii. For the excitation function to work, the trigger thresholds must be set at the outset. When the excitation file is loaded, previous loaded trigger thresholds set back to 0 V and must be reset by the user to operate properly. It would be worthwhile to have the default value 0.5 V as is in the software for the SPS beam excitation system.
 - iii. Fiducial: Trigger lost for threshold setting above 0.5 V. Trigger on noise at threshold 0.2 V.
 - iv. Injection: Trigger lost for threshold setting above 0.3 V.
 - (e) Check injection delay. Move by 1 increment, look at change on scope, output signal moves correspondingly with injection delay.
 - (f) Check fiducial delay. Signal moves correspondingly with the fiducial marker.

- (g) Figure 2 shows a scope screen capture for an injection delay of 4, fiducial delay of 200 and signal length of 10 turns. File: 121116_221155. Ch2: Injection strobe, Ch3: Excitation DAC signal, Ch4: Fiducial strobe.

Figure 2: 121116_221155.png - ID: 4, FD: 200, 10 turns. Ch2: Injection strobe, Ch3: Excitation DAC signal, Ch4: Fiducial strobe.

5. **Nov. 27, 2012** - Check synchronization between old excitation system and new feedback system.
 - (a) Setup strobes to monitor fiducial and injection triggers, and monitor DAC signal of old excitation system and new excitation system.
 - (b) Create .cfg file with signal playback of 10 turns. Load file to both systems. Remember that the trigger thresholds need to be reset in the software upon file load.
 - (c) In looking at both DAC outputs on the scope, we see synchronous signals. Minor difference in timing ($\Delta t = 400$ ps) probably arising from different cable lengths from each respective DAC out to the scope.
 - (d) Scope screen capture for injection delay in Figure 3: 10, fiducial (bunch) delay: 0. 121127_093902. $50\mu\text{s}/\text{div}$ showing injection delay. Ch1: Old excitation DAC, Ch2: Injection strobe, Ch3: New excitation DAC, Ch4: Revolution strobe
 - (e) Changed the injection delay to 0 on both systems 121127_094035 $1\mu\text{s}/\text{div}$. multiview zoom: 121127_094138, 121127_094308
6. With both DACs behaving consistently, setup the output channel, shown schematically in Figure 5
7. Check hybrid for isolation
 - (a) Remove new DAC signal from port B, look at port B on the oscilloscope, Ch3. Look at sum signal out of port C with Ch1. Play old DAC signal through port A,
 - (b) Measure port C, 60 mV_p . Measure port B, 1 mV_p . 1:60 isolation.
8. With entire back end cabled up, we see about a 20 ns (4 bucket) difference in DAC signals.
 - (a) Adjust the bunch delay to move the excitation signal closer to the fiducial strobe. Change the bunch delay to 4608 in the excitation DAC and the fiducial delay to 4606 in the feedback DAC.

Figure 3: 121127_093902 - ID: 10, FD: 0, 10 turns, Ch1: Old DAC out, Ch2: Injection strobe, Ch3: New DAC out, Ch4: Fiducial strobe

Figure 4: Multiview zoom showing synchronization of old and new DAC excite signals. The difference in time between the two signals is 400 ps.

Figure 5: Backend channel

Note: the bunch delay in the excitation software for the excitation system has the same function as in the excitation software for the feedback system. These should be named the same to avoid confusion. Now both signals within $\Delta t = 10$ ns.

- (b) Set excitation DAC bunch delay to 4610 and feedback DAC fiducial delay to 4606, with each programmable delay 0.0 ns. The output signal from the hybrid looks pretty well time aligned. Screen capture in Figure 6: 121122_104851 - Ch1 hybrid sum signal, Ch4 fiducial strobe. Amplitude of signal is 120 mV_p. When one signal is turned off, the amplitude reduces to 60 mV_p. This concludes the synchronization between the two DACs.

Figure 6: Ch1 - hybrid sum signal of old and new DAC in time alignment. Ch4 - fiducial strobe. 121127_104851

9. Search for ADC sampling region, referenced to the fiducial strobe.

- (a) Use an arbitrary function generator to search for the location of the sampling region in the ADC. Pulse signal with 21 μ s period (just under revolution period, 23 μ s), 20 μ s pulse width, 70 mV amplitude.
- (b) Trigger the function generator with the revolution fiducial (generator needs TTL pulse)
- (c) Split generator signal with a tee (to see signal also on scope, set scope to 1 M Ω high impedance)
- (d) Use -10 dB attenuator on the output of the tee to the ADC. Bypass the delay card and splitter internal to the feedback system and send signal directly to the ADC since delay card does not have DC response.
- (e) Design an FIR filter with Claudio's MATLAB routine for a pass through filter (e.g., 1 0 0 ... 0), SPSFeedback_Nov-27_1146.cfg
- (f) In software, on CSRs panel, switch CSR1 $\rightarrow$ MODE $\rightarrow$ FEEDBACK and enable
- (g) Monitor feedback DAC output on scope Ch1. Reduce pulse width of generated signal until signal out of DAC disappears. Width reduced to 400 ns, signal disappears
 - i. Measure the time between the rise of the fiducial strobe signal to the end of the generator signal as a reference
 - ii. Set ADC FIDUCIAL DELAY on the FEEDBACK CONTROL panel to ADCFD = 100. A corresponding time difference of $\Delta t = 448$ ns, is measured between the fiducial strobe and generator signal.

- iii. For $\text{ADCFD} = 50$, $\Delta t = 195$ ns
- iv. For $\text{ADCFD} = 30$, $\Delta t = 88$ ns. Screen capture: 121127_120439 - Ch1 is new DAC, Ch3 is generator signal to ADC, Ch4 is fiducial strobe.
- v. We now have a reference for where the ADC sampling region is with respect to the fiducial.

Figure 7: Searching for the sampling region of the ADC: 121127_120439 - Ch1 is new DAC signal, Ch3 is signal generator to ADC, Ch4 is fiducial strobe.

10. Mimic the pickup signal to the feedback ADC with the excitation DAC

- (a) Use excitation DAC signal to drive the feedback ADC input as shown schematically in Figure 8

Figure 8: Setup for testing the front end of feedback system.

- (b) Excitation DAC signal level 60 mV_p , using about $1/4$ the dynamic range of the ADC.
- (c) Connect the old DAC to the ADC input. See DAC signal out, but not time aligned. On the DSP filters panel, do an ADC reset to clear messy (spider) signal. On MMCM Phase Control panel, set ADC system clock phase: 15, ADC Reset Clock Phase: 10, DAC system clock phase: 16.
- (d) Adjust the programmable delay on the Excitation DAC to 0.9 ns.
- (e) On the FEEDBACK CONTROL panel, set ADC FIDUCIAL DELAY: 30, INJECTION DELAY: 0, DAC FIDUCIAL DELAY: 0. (On excitation system gui, BUNCH DELAY: 2)
- (f) View Feedback DAC output on scope, Ch1. We can see the 200 MHz sine wave generated by the Excitation DAC pass through the FIR to the Feedback DAC. Move ADC fiducial delay by one to 29 or 31, see signal in scope disappear. Thus, we are no longer sampling the region in time where the signal is located.

- (g) Change the ADC FIDUCIAL DELAY to 35, BUNCH DELAY on the excitation system gui to 7. We see the signal on the scope. We can move the sampling region, and move the excitation signal simultaneously and maintain time synchronization between the two, tracking between two system buckets seems to work fine.
 - (h) On the FEEDBACK CONTROL panel change the DAC FIDUCIAL DELAY from 0 to 1 to move the signal 5 ns in time. Change from 0 to 4608 to move the signal to just after the fiducial strobe.
 - (i) Great, we are able to sample a signal with the ADC, pass it through the FIR, and play out with the DAC!
11. Test DSP/FIR CONTROL function
 - (a) Check swapping coefficients, use a pass through filter with two different gains.
 - (b) There is 1 turn delay in the coefficient swap. So, if SWAP TURNS is 10, expect to see 11 turns with coefficients of one set, then the second set will start.
 - (c) SWAP WAIT will play out the data using the second set of coefficients for the selected number of turns, then go switch back to the first set of coefficients.
 - (d) Seems to be working fine.
12. Check FIR filter response, fine tune front end timing.
 - (a) Set up mock pickup signal with the excitation system. Signal: Mode 0, AM, 0.1 tune constant, 1000 turns.
 - (b) Set up FIR filter: 5 tap, $\phi = 90^\circ$ @ 0.1, gain just less than 1.
 - (c) Figure 9 shows the mock pickup signal as processed by the 5 tap FIR filter in Ch1. Ch2 shows the injection strobe and Ch3 shows the fiducial strobe.

Figure 9: Ch1 shows the Feedback DAC signal from a mock pickup signal of rectangular width at 0.1 tune and processed by a 5 tap FIR filter. Ch2 shows the injection strobe. Ch4 shows the fiducial strobe. File: 121127_161653

Table 1: Results of the FIR filter phase sweep at 0.1 tune, monitoring the resulting shift in the zero crossing of the feedback signal, Δt

ϕ ($^\circ$)	Δt (μs)	File (screen capture)
0	322	
31	295	162950
60	290	
90	263	162508
140	227	
160	213	162247
180	217

Figure 10: Results of the FIR filter phase sweep at 0.1 tune, plotted as phase as a function of time where DAC signal crosses zero. This should be a linear function, however, for the precision of this test, the results are not bad.

- (e) Record a screen capture showing the feedback signal from the mock pickup signal provided by the Excitation DAC in Figure 11 Same DAC signal as above, rectangular wave, AM, (mode 0). File 121127_201347 - Ch1 the Feedback DAC signal, Ch2 the Excitation DAC signal, Ch4 the fiducial strobe.

Figure 11: Screen capture of the mock pickup signal from the Excitation DAC (tune = 0.1, mode 0, AM) in Ch2, The feedback signal from the Feedback DAC using a 5 tap FIR filter with frequency 0.1, gain 1 in Ch1. File 121127_201347

- (f) Increase the number of taps on the FIR filter: 10 taps, $\phi = 90^\circ$ @ 0.1 tune. Saved the waveforms for 1050 turns:
- i. 121127.201728
 - ii. 121127.201912
- (g) Using the same FIR filter, change the mock pickup signal to sine 200 MHz (mode 1) with 0.1 tune. File 121127_202304.wfm. With this mock pickup signal, we noticed that the correction signal is a bit out of phase.
- (h) Adjust programmable delay of the new ADC, from 0.5 ns to 0 ns. Still too much delay so we must make a more course change. On the FEEDBACK CONTROL panel, change the ADC FIDUCIAL DELAY from 28 to 29 and set programmable delay to 3.5 ns. Save waveforms and screen capture. Figure 12 shows a screen capture of the feedback signal, Ch1, for the time adjusted ADC with sine 200 MHz mock pickup signal, Ch2.
- i. 121127_203327.wfm
 - ii. 121127_203343.png
 - iii. 121127_204022.wfm
- (i) The timing can be further refined, by simulating a pickup signal of higher frequency. Use a mode 2 (sine 400 MHz) signal. Adjust slightly the programmable delay to 3.6 ns. The alignment of the signal looks good in Figure 13.
- i. 121127_203814.wfm
 - ii. 121127_203836.png
- (j) We repeat this process for an input pickup signal of mode 3 (sine 600 MHz) and mode 4 (sine 800 MHz) shown in Figure 14. At mode 4, at the 3 dB point of the programmable delay, so there's a loss of signal.

Figure 12: Ch1 shows the feedback signal for a mock pickup signal of sine 200 MHz (Ch2). File: 121127_203343

Figure 13: A screen capture showing the Feedback DAC signal (Ch1) with a sine 400 MHz mock pickup signal (Ch2). File 121127_203836

(k) End of tests and measurements, Nov. 27, 2012.

i. Mode 3

A. 121127_204303.wfm

B. 121127_204357.png

ii. Mode 4

A. 121127_204754.wfm

B. 121127_204816.png

Figure 14: Screen captures showing the Feedback DAC signal (Ch1) for a sine 600 MHz and sine 800 MHz mock pickup signal (Ch2). Very good timing between the front end and back end displayed. File 121127_204357, _204816

13. **Nov. 28, 2012** - Check gain of the feedback system.

- Inject a 200 mV DC signal into a resistive splitter, monitor both outputs on scope $\rightarrow 100 \text{ mV}_{\text{DC}}$. Nominally, this is a 6 dB splitter (and we see this) and will be used to split the raw delta signal from the hybrid in order to monitor the signal on the scope, and inject the signal to the front end receiver before the ADC (Bessel filters, equalizer, attenuators, amplifier).
- Connect each output of the splitter directly to each ADC card bypassing the splitter and delay board internal to the feedback chassis (no DC response).
- Design an FIR filter for pass through of gain 1. With 100 mV supplied to each ADC card, the corresponding DAC signal measured: 93 mV, 5 ns width.
- Design an FIR filter for pass through of gain -1. With 100 mV supplied to each ADC card, the corresponding DAC signal measured: -87 mV, 5 ns width.
- Increase the gain of the FIR to 2 (-2), DAC output, 185 (-179) mV. DSP not yet saturated.
- Increase input signal until we see DSP SATURATED indicator light on the chassis front panel. Saturates with DAC signal of 228 (-222) mV, gain set at 2 (-2).
- Set gain to -0.5, saturate ADC. 507 mV to splitter, 254 mV to each ADC, see -110 mV out of DAC.
- Now, use excitation system to provide sine 200 MHz signal to ADC to replace signal produced by function generator to resistive splitter. Signal out of Excitation DAC through the resistive splitter, 100 mV_p . Signal at input of each ADC card, 50 mV_p . (The signal passes through a programmable delay line, and internal splitter and delay line).

- (i) Provide sine 400 MHz signal: Signal out of Excitation DAC through resistive splitter, 88 mV_p. Signal at input of ADC card, 40 mV_p
- (j) Change gain back to 1. Monitor Feedback DAC signal after hybrid. Output of Excitation DAC through resistive splitter, 54.4 mV_p. Signal at various points from the Feedback DAC backend chain are listed in Table 2. Note: the hybrid should only have insertion loss of 3 dB, but it looks like we have more like 6 dB. Why? For a continuous 400 MHz signal we have 3 dB attenuation, but for a burst 400 MHz signal we have 5-6 dB.

Table 2: Output of the Feedback DAC with a 200 MHz and 400 MHz signal of level 100 and 54.4 mV_p at output of the resistive splitter

Measurement location	Signal level (mV _p)	
	Sine 200 MHz	Sine 400 MHz
Directly DAC out	115	21.4
DAC out → -6 dB att.		10.6
DAC out → -6 dB att. → Prog. delay	50.4	8.4
DAC out → -6 dB att. → Prog. delay → hybrid	28.8	4.2

- 14. Noise measurement of new DAC channel and associated backend chain: 2.0 mV
- 15. With beam, setup receiver front end chain.
 - (a) See screen captures of the delta signal with various filtering elements in Figure 15.
 - i. Delta signal from the hybrid, 121128_190118
 - ii. From hybrid + 800 MHz Bessel Filter, 121128_190359
 - iii. From hybrid + equalizer, 121128_190731
 - iv. From hybrid + equalizer + Bessel, 121128_190954
 - v. From hybrid + Bessel + equalizer, 121128_191151
 - vi. From hybrid + Bessel + equalizer + Bessel, 121128_191538
 - (b) A block diagram of the front end receiver chain is in the MD configuration in Figure 16, and the associated hardware details listed below.
 - i. Colby programmable delay, HPDL-100A-10.23ns, DC – 12.5 GHz
 - ii. 800 MHz Bessel low pass filter
 - iii. Equalizer
 - iv. MITEQ amplifier AM-3A-000115, 35 dB gain, 1 – 1500 MHz
 - v. Mini-Circuits Switch ZASW-2-50DR, DC – 5 GHz
- 16. Move orbit to observe potential signal level to the ADC from pickup, see Table 3. We will use the setting -0.5 mm.
- 17. With the inclusion of the receiver, we must again check the timing of the ADC sampling.
 - (a) On the scope, monitor the fiducial strobe and the pickup signal as processed through the front end receiver electronics (supplied to chassis front panel), $\Delta t = 77$ ns, very close to yesterday's 88 ns when searching for the sampling region. We are close.

Figure 15: Delta signal from hybrid, with various filters. Left to right First row: i, iii, v. Second row: ii, iv, vi

Figure 16: Front end receiver electronics as used for the MD

Table 3: Signal levels measure at the output of the resistive splitter (raw delta signal) and at the output of the front end receiver chain.

orbit (mm)	Signal Levels (mV)	
	Raw delta signal	Full front end receiver processed signal
-0.85	-80 – 45	-500 – 625
+0.5	-15 – 20	-320 – 0
+0.6	-18 – 20	-250 – 0
+1.4	-30 – 60	-700 – 0

- (b) Reconnect the pickup signal to the chassis front panel ADC IN, view the DAC signal through the delay and hybrid, Ch1. Fine tune the ADC FIDUCIAL DELAY to 27 from the FEEDBACK CONTROL panel. Adjust the programmable delay, 5 ns. Setup FIR filter in pass through mode to see the equalized bunch signal out DAC. First real beam signal through new hardware, Figure 17! This completes the front end timing until the back end is timed up.
- 121128.210923.png
 - 121128.210851.wfm, saved 1000 turns. With this data, Claudio tests his centroid finder routine.

Figure 17: Pickup signal through the feedback hardware, FIR filter in pass through mode