LabVIEW DAQ of NE213 Liquid Scintillator
LabVIEW DAQ Manual

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Front Panel as seen on PC

Control Circuit Diagram

CAMAC Notes

C.A.M.A.C. - Computer Automated Measurement And Control

Uses of CAMAC:

1. Data Acquisition
2. Remote Trigger
3. Logic Application

CAMAC crate consists of 25 stations. To reference a module in the crate, the station number is specified. The Crate controller is placed on the 25th station; it is referenced as station 30. All other modules are referenced according to their station number.

Registers for establishing communication and defining function for execution

- N: Module, or Station, Number. CAMAC crate is numbered 1-25 stations
- A: Modules have different sections to perform various functions; these are addressed by register A. There are no more than sixteen of these sections
- F: Function performed on specified sections of selected modules. 32 Functions total; Function 0-7 are read commands and 16-23 write commands

LAM

Look-At-Me register. LAM is set when module requires attention. Attention is required when a process has completed and awaits further processing by PC. Each station in CAMAC crate has an independent LAM wired to crate controller.

ADC

12 channels on the ADC. A: 0-11 refers to the analog channels. Set analog signal to 1 of 2048 digital channels

GPB 3988 Crate Controller VI's

GPB 3988 Crate Controller VI's can be found in the following directory:

C:\Program Files\National Instruments\LabVIEW 7.0\inst.lib\aks 3988old\ks3988

Digital I/O Board

1. Only accepts TTL signals
2. All terminals are set to binary 1 (5 Volts) unless a wire is place to the terminal

Circuit Diagram

The circuit diagram on page 4 does not present a TTL to NIM conversion of the output port of the Digital I/O Board

The LabVIEW-based DAQ software has three main sequences of events, each designed to execute an organized algorithm.

Data Acquisition System

First Sequence

Initialization and Configuration of CAMAC

- GPIB Address Initialization
 1. The GPIB address is specified in the front panel
 2. The GPIB crate controller has 4 prongs on the circuitry of the physical module. Arrangement of prongs defines the address of the GPIB. If all prongs are set to 1, then the GPIB address is to 16. The address of the GPIB is stored in the pink line below.
 3. The following VI sets the Z register – initializes all modules of CAMAC system

- Clear CAMAC Registers
 1. Clears all CAMAC Registers. Registers of Concern:
 - C: All registers are cleared
 - Z: All modules in the CAMAC crate are initialized
 - I: Inhibit Gate to S2 time with F set as 25
 - Q: Indicates status of module during DATAWAY
 - X: Set to 1 if module recognizes command
 - L: LOOK-AT-ME or LAM.
 - B: Indicates whether DATAWAY is busy
 2. N is set to 30. Defines the station number of the crate controller
 3. F: 17. 16 bit write
 4. A: 0
 5. Control/Status Register Bits set to 64, i.e. 7th bit is set. This sets register C to clear CAMAC registers. Essentially clears the set Z register so CAMAC system does not keep reinitializing

Initialization and Configuration of Digital Input/Output Board

- Configures the input and output ports of the Digital I/O Board
- Port number – Label the Ports
 - o Output port: 0
 - o Input port: 1
- 8 in the diagram below refers to the number of bits assigned to each port
- Line Direction(the line entering the Port Config. VI's from below): 0 : Input
-1 : Output
- The two lines labeled write and read are the Task ID lines. They carry necessary information to perform write and read commands

Port Write

- Write zero to output terminal
 - o This sets 0 voltage at the stop terminal of the Gate Generator - refer to circuit diagram
 - Setting stop terminal to 0 inhibits circuitry
 - o The line coming in from the right leads into the Task ID terminal. This line has information so that the port write function understands what to execute and to what bits of the Digital I/O Blocks

File Header

- Creates the file header. Includes following information
 - o File header as specified by user
 - o Authors Names
 - o Time
 - o Date
- If user does not prefer to write to file the following will not be executed

Create an Array for Data Storage

- Creates an array of 2048 elements, all set to value zero

Second Sequence

Port Read

- Check to see if TTL signal is high from the Gate Generator
 - If high, circuitry is inhibited -ADC is ready to be read – loop ends
 - If low, circuitry is not inhibited and loop will continue until TTL is high
- Line coming in from the left is called the Task ID In, and the line stretching to the far right is the Task ID Out
- As soon as all 8 bits of the input port are set to 1, i.e. 255 is read, the loop ends and ADC is read

Why 255? First of all, all unwired lines on the block are set to 1. If a wire applied to one of pins is a low signal, ~ 0V, the bit registers a binary 0. The 0th pin of the input port, pin 31, is wired to the TTL output terminal of the Gate Generator. If the Gate Generator is not triggered with a signal, its output terminals constitute a low voltage. The Gate Generator is in latch mode. So, if the Gate Generator (GG) is not triggered, then pin 31 is set to a zero and the 8 bits of the input port is read to be 254. If the GG is triggered, then pin 31 is set to a 1 and the input port is read to be 255. If the GG is triggered, and the stop terminal receives a high signal, then pin 31 is set to 0 and the input port is read to be 254. If the GG is triggered then a gate can be expected to be waiting at the terminal of the ADC waiting to be read. So if the input port is read to be 255 the while loop is broken and the “Read ADC / Check for Hang Up A.K.A Crash” sequence is executed.

- The “Iteration of Trigger Loop” is a debugging tool used to see how many times the port read function must execute until a gate is detected

Read ADC / Check for Hang Up A.K.A Crash

- The sub VI in the upper left corner of the diagram is a 16 bit read function from the CAMAC crate

- The blue line coming from the left of the sequence into the sub VI from above, defines the station number of the ADC
- F: 2. Reads all 12 channels of ADC and clears the ADC after the 11th channel is read
- A: 0. The sub-address of the ADC containing information to execute an F: 2 read
- The pink line coming into the VI from the left is the GPIB address, 16
- The blue line coming directly to the left of the sub VI defines the total number of channels the ADC carries, 12
- The lower half of the sequence checks to see if the program has hung up attempting to read from the ADC
 - If the ADC cannot be read properly within 2 seconds then a set of sequences is activated to initialize the CAMAC modules and clear the CAMAC Registers. This jump starts the program and allows the DAQ to read the ADC properly. Note that the Digital I/O Trigger method has not shown reason to have this “jump start,” it is only placed for percussion purposes

Allow for Next Gate to Flow Through

- This sequence sets the stop terminal of the Gate Generator to 1 and then quickly back to 0
- This allows the next gate to flow to the ADC terminal

Histogram

- If the "Operate Graph" switch is turned off then the function below is executed
 - o The following creates updates an array of 2048 elements with each detected event
- If the "Operate Graph" switch is turned on then the only difference from what is shown below is the histogram VI is attached to the end of the sequence of VI's. The histogram VI displayed the recorded data on a plot shown on the front panel of the DAQ system

Conditions to Break Second Sequence

- Number of desired events is reached
- Desired time is reached
- Switch to take data is turned off. This switch is necessary if the user is running the program and desires to stop data taking. If the user hits the red stop button provided by the LabVIEW editor then the information collected would not be stored to file. If the user flipped the switch labeled "Take Data," then the program will stop taking data and also finish the rest of the programs sequences which include writing to file

Third Sequence

Extract Total Number of Events According to Scaler

- N: 17
- A: 0 and 1
- F: 2. Read all channels and clears the module

- 48 bit read from channels 0 and 1. Channel 0 reads as if it is the first 24 bits and channel 1 as the last 24 bits. The scaler module, LeCroy model 2551 requires internal modifications for such functionality.
 - The integer 16777216 is equal to 2^{24} . Multiplying 2^{24} to the values read from channel 1 shifts the bits up 24 bits. The two values are then added and act as if the Scaler has a built in channel capable of 48 bit reads. Look up scaler manual for further information

Storing More Headers and Experimental Data

- Stores elapsed time in seconds, number of detected events, total number of events that are detected by Scaler from first discriminator
- Writes the array containing the experimental data to the file

Digital Input/Output Board

Digital I/O Board and HB-100 Connector Block

The Digital I/O Board, National Instruments PCI-DIO-96, is a standard PCI card placed in the computer. An external NB5 ribbon cable connects the I/O board to a CB-100 connector block. The connector block is an interface between the I/O board and the CAMAC and NIM systems. The NB5 ribbon cable consists of two ribbon cables, each a set of 50 wires. Each wire represents a different bit, as shown in the figure on page 11. The connector block is simply a device that allows the 100 wires to attach to their own personal terminal or pin.

From the two blocks there are two ground lines, two 5V power supply lines, and 96 variable lines. The 96 digital lines are divided up into 12 sections or ports. The 12 resulting ports consist of 8 bits each. For our purposes, only two ports are used, one defined as the input and the other the output port. Furthermore, we are only using one terminal or pin from each port, pins 47 and 31. Pin 31 is the 0th bit of the 8 bit wide input port. Pin 47 is the 0th bit of the 8 bit wide output port. When an event triggers the Gate Generator, a TTL signal is sent to the Digital I/O Board, signaling the PC that the circuitry is inhibited and an event is waiting for reading from the ADC. When the TTL signal is sent to the I/O board, the pin 31 is set to 1. The Digital

I/O Board also sends signals to the circuitry through pin 47. A high signal (+2.2 - +5.3 Volts) applied to a pin of the connector block is processed as a binary 1; low signals (-0.3 – +0.8 Volts) indicate a binary 0 and vice versa.

HB-100 Connector Block - Bit Arrangement

PC7	1	2	GND
PC6	3	4	GND
PC5	5	6	GND
PC4	7	8	GND
PC3	9	10	GND
PC2	11	12	GND
PC1	13	14	GND
PC0	15	16	GND
PB7	17	18	GND
PB6	19	20	GND
PB5	21	22	GND
PB4	23	24	GND
PB3	25	26	GND
PB2	27	28	GND
PB1	29	30	GND
PB0	31	32	GND
PA7	33	34	GND
PA6	35	36	GND
PA5	37	38	GND
PA4	39	40	GND
PA3	41	42	GND
PA2	43	44	GND
PA1	45	46	GND
PA0	47	48	GND
+5 V	49	50	GND

National Instruments Corporation – PCI-DIO-96 User Manual

The pin configuration tabular is shown on page13. It describes the pin layout of all 100 terminals.

Each port is composed of 8 pins. A port's 8 pins are labeled bits 0-7. The information provided is from the pin configuration tabular on port 2.

1, 3, 5, 7, 9, 11, 13, 15	APC<7..0>	2	Bidirectional data lines for port C of PPI A—APC7 is the MSB, APC0 the LSB.
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The bits arrangement is as follows, note that the bit arrangement is done “backwards”

Pin	1	3	5	7	9	11	13	15
Bit	7	6	5	4	3	2	1	0

HB-100 Connector Block – Pin Configuration

Pin	Signal Name	Alternate Port ID*	Description
1, 3, 5, 7, 9, 11, 13, 15	APC<7..0>	2	Bidirectional data lines for port C of PPI A—APC7 is the MSB, APC0 the LSB.
2, 4, 6, 8, 10, 12, 14, 16	BPC<7..0>	5	Bidirectional data lines for port C of PPI B—BPC7 is the MSB, BPC0 the LSB.
17, 19, 21, 23, 25, 27, 29, 31	APB<7..0>	1	Bidirectional data lines for port B of PPI A—APB7 is the MSB, APB0 the LSB.
18, 20, 22, 24, 26, 28, 30, 32	BPB<7..0>	4	Bidirectional data lines for port B of PPI B—BPB7 is the MSB, BPB0 the LSB.
33, 35, 37, 39, 41, 43, 45, 47	APA<7..0>	0	Bidirectional data lines for port A of PPI A—APA7 is the MSB, APA0 the LSB.
34, 36, 38, 40, 42, 44, 46, 48	BPA<7..0>	3	Bidirectional data lines for port A of PPI B—BPA7 is the MSB, BPA0 the LSB.
49, 99	+5 V supply	—	+5 Volts—These pins are fused for up to 1 A total of +4.65 to +5.25 V.
50, 100	GND	—	Ground—These pins are connected to the computer ground signal.
51, 53, 55, 57, 59, 61, 63, 65	CPC<7..0>	8	Bidirectional data lines for port C of PPI C—CPC7 is the MSB, CPC0 the LSB.
52, 54, 56, 58, 60, 62, 64, 66	DPC<7..0>	11	Bidirectional data lines for port C of PPI D—DPC7 is the MSB, DPC0 the LSB.
67, 69, 71, 73, 75, 77, 79, 81	CPB<7..0>	7	Bidirectional data lines for port B of PPI C—CPB7 is the MSB, CPB0 the LSB.
68, 70, 72, 74, 76, 78, 80, 82	DPB<7..0>	10	Bidirectional data lines for port B of PPI D—DPB7 is the MSB, DPB0 the LSB.
83, 85, 87, 89, 91, 93, 95, 97	CPA<7..0>	6	Bidirectional data lines for port A of PPI C—CPA7 is the MSB, CPA0 the LSB.
84, 86, 88, 90, 92, 94, 96, 98	DPA<7..0>	9	Bidirectional data lines for port A of PPI D—DPA7 is the MSB, DPA0 the LSB.

National Instruments Corporation – PCI-DIO-96 User Manual

The DAQ system sets Port 0 as the Output terminal, and Port 1 as the Input terminal. Pin 47 of the output terminal is the determining factor to veto the flow of circuitry, and pin 31 the determining factor to whether the ADC is ready to be read.

Module Manuals

Crate Controller – KineticSystems GPIB 3988

<http://nstx.pppl.gov/nstx/Controls/specs/3988.pdf>

Digital Input/Output Board – National Instruments

<http://www-corot.obspm.fr/COROT-ETC/Files/PCI-6503.pdf>

ADC – LeCroy 2249W

<http://www-esd.fnal.gov/esd/catalog/main/lcryn timer/2249w-spec.htm>

Gate Generator – LeCroy 2323

<http://www-esd.fnal.gov/esd/catalog/main/lcryn timer/2323-spec.htm>

Discriminator – LeCroy 623B

<http://www.fnal.gov/projects/ckm/jlab/623b-spec.htm>

Logic Unit – Phillips Scientific 754

<http://www.jlab.org/~segal/manuals/phillips/ps755/755.htm>

Level Adapter – LeCroy 688AL

<http://www-esd.fnal.gov/esd/catalog/main/lcryn timer/688al-spec.htm>

Scaler – LeCroy 2551

<http://www-esd.fnal.gov/esd/catalog/main/Lcryn timer/2551-spec.htm>

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Instruction Manual – GPIB Crate Controller – Model 3988-G3A/D3A
KineticSystems Corporation

Users Manual – Digital I/O Board – PCI-DIO-96
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