Design Considerations for a Si/W EM Cal. at a Linear Collider

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SD Detector
• SD designed for excellent energy flow performance – with well-understood and somewhat constrained cost (see Snowmass Orange Book for details)

• Si/W ECal
  – 5mm transverse segmentation
  – [ 2.5 mm W (0.7 X₀), 0.4 mm Si ] x30
  – \( R_m = 9\text{mm } (1 + \text{gap(mm)}/2.5) \rightarrow \text{Keep gaps small!} \)

In this talk:
• Some architecture and readout issues
• Dynamic range and some electronics issues
• Next steps
Si/W Readout-SD

- ~50 M pixels, 5x5 mm²
- Do NOT scale electronics by this number
- 1 chip per wafer
- 1 chip per ~1 m² of wafers
Noise

- GLAST Si electronics: $20e/pF + 200e \rightarrow \approx 2000e$ (fine)

Cooling

- NLC duty cycle is $\sim 10^{-4}$
  \hspace{1cm} \rightarrow$ Assume $10^{-3}$ power duty cycle
- GLAST elec. power: 2 mW/chan.
- For standard W alloy, can cool one edge of W plate
  \hspace{1cm} \rightarrow \approx 2^\circ$ rise (fine)

Dynamic Range

- MIPs
- 500 GeV Bhabha electrons
- EGS study: $\approx 2000$ MIPs
- Maintain low-end resolution
  \hspace{1cm} \rightarrow$ 3 ranges of 12 bits
EGS Setup

- Use the G. Lindstrom, et al., recommendations* for $E_{\text{cut}}$ in thin sampling layers. (Good accuracy with finite CPU time.)

- Reduced $E_{\text{cut}}$, $P_{\text{cut}}$ in thin regions near the Si

- Step size small (0.3%) everywhere

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- Broad shower max in depth $\sim 6.5 \pm 1 \ X_0$

- Fraction of energy in central $1\text{cm} \times 1\text{cm}$ is $\sim$independent of $E_e$:

$\Rightarrow$ need big pixel size reduction to change dynamic range requirement significantly
- Charge amp. with ~ 10pf feedback cap.
- 3 ranges @ 12 bits
Next…

- Further design work
- Prototypes:
  - Silicon wafer with 5mm pixels and metallizations for wafer readout chip
  - Wafer readout chip
- The other readout chips
- A one wafer wide, full depth module for test beam