The Read-Out System of the ALICE Pixel Detector

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for the ALICE Pixel Detector Collaboration

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Presentation scope

• Read-out Architecture
• ASIC development and test systems
• Physical implementation
ALICE Pixel Detector

pixel chip

2 ladders = half stave

r/o elec.

Image: INFN(Padova)
System Requirements

- L1 after 6 μs, L2 after 100 μs
- L1 rate 1 kHz, L2 rate 40-800Hz
- Readout upon L2
  - ~ 1 GB/s raw data
- Small physical implementation
- 10 MHz system clock
- Configurable by JTAG
- Radiation: < 500 krad, neutron flux 3 x 10^{11} cm^{-2} (10y)
- SEU safe
OPS implementation

Pixel chips 9

Pixel chips 0

Pixel pilot

Pixel control transmit

G-link

 Serializer & optics

Pixel control receive

Pixel transmit

Pixel converter

Pixel control and link receiver

L1, L2y, L2n, testpulse, JTAG

Converter and control daughter card

Pixel router

Pixelbus

Pilot MCM

Control room

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OPS implementation

pixel pilot core

pixel bus

data control

pixel transmit

G-link

pixelcontrol receive

pixel MCM

opt. links

opt. link

link receiver

pixel converter

pixelcontrol transmit

pixel converter and control daughter card

L1, L2y, L2n, testpulse, jtag

pixel router

control room

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OPS implementation

pilot MCM

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receive

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converter and control daughter card

data control

pixel router

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OPS transmission principle

- Event info
- Pixel data bus
- Data control
- Signal feedback

- clk10
- clk40
- Cycle

MUX 4:1

32 x 10 MHz
16 X 40 MHz
Link receiver / data converter

pilot MCM

control room

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Link receiver / data converter

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HDMP 1034

FIFO

encode+

format

RAM
ASIC Development
Pilot MCM

12 mm

PIL
ana

PILOT
digital

GOL

Laser +
2 Pin diodes

50 mm

1.4 mm
ASIC implementation

- IBM 0.25 \( \mu m \) ASIC designs (rad tolerant design)
- No on detector data processing, no memory on detector
- Use of already developed Glink chip GOL
- Only 3 optical connections
  - No GND loops
Digital Pilot chip
GOL

File   Control   Setup   Measure   Analyze   Utilities   Help

Acquisition is stopped.
8.00 GSa/s

1) On  2 mV/div  2) (1 & 2 Combined)  3) On

Histogram | Color Grade | Scales

scale: 250 mhits/div
mean: No data
std dev: No data
p-p: No data

offset: 0.0 hits
median: No data
hits: No data
peak: 0.0 hits

μ±1σ: No data
μ±2σ: No data
μ±3σ: No data

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XILINX VIRTEX II 840 Mb/s LVDS

[Image of a graph showing various measurements and hits, with data points and statistical values provided.]
Analog Pilot chip
Optical package

1.2 mm
6 mm
16 mm
OPS Test system

pilot_in
clk_opt_in
data_opt_in

clk_opt
pilot

clk_opt_out
data_opt_out

50
44

FPGA

clk40

RAM
128k 48

JTAG
OPS Tester
pixel bus

pixel pilot

pixel chip 9

pixel chip 0

pixel control transmit

pixel control receive

pixeltransmit opt.

g-link

serializer &

optics

busy, jtag

link receiver

pixel converter

pixel control

daughter card

pixel router

L1, L2y, L2n,
testpulse, jtag

converter and
control daughter card

cell

control room

pilot MCM

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G-link & optics

link, L1, L2y, L2n, testpulse, jtag

pixel control and transmit converter and control daughter card

pixel transmit

opt. link

pixel control receive

pixel control transmit

pixel transmi

pilot MCM

control room
G-link
serializer &
optics
L1, L2y, L2n,
testpulse, jtag
pixel
pilot
pixel control
transmit
G-link
serializer &
optics
link
receiver
pixel converter
pixel control
transmit
L1, L2y, L2n,
testpulse, jtag
pixel router
pixel control
transmit
pixel control
transmit
pixel control
receive
pixel control
receive
pixelchip 0
pixelchip 9
pixelchip 0
pixelchip 9
pixelbus
pilot MCM
control room
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G-link
optics
L1, L2y, L2n, testpulse, jtag
Pixel chip 0
Pixel pilot
Pixel chips

Pixelbus
Pilot MCM
Control room

Pixel control
transmit

Link receiver
Pixel converter
Converter and control daughter card

Opt. links

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G-link
serializer &
optics

testpulse, jtag
pixel
pilot
chip 0
pixel
chips
pixel
chip 9

G-link
Serializer &
Optics
Busy, JTAG
Pixel Transmit

Pixel Transmit

Opt. Link

Link Receiver
Pixel Converter

L1, L2y, L2n,
Testpulse, JTAG
Converter and
Control Daughter Card

Pixel Router

Pixel Control
Transmit

Pixel Control
Receive

Pixelbus
Pilot MCM
Control Room

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Physical implementation
Pixel carrier & extender (side)
Pixel carrier & extender (side)
Pixel carrier & extender (side)

- Analogu PILOT
- Digital PILOT
- GOL
- Opt Receiver
  Trans
Pixel carrier & extender (side)

PIXEL_CARRIER

Analogu PILOT  Digital PILOT  GOL  Opt Receiver Trans
10 chips on a carrier
10 chips on a carrier
10 chips on a carrier
10 chips on a carrier
10 chips on a carrier
Pilot MCM

- 12 mm
- 50 mm
- 1.4 mm

Components:
- PIL ana
- PILOT digital
- GOL
- Laser + 2 Pin diodes
Pixel Readout Test System

- Pixel bus
- Pilot MCM
- FPGA
- Memory
- Link receiver
- Pixel converter
- VME bus
Component Status

Pixel chips

Pixel carrier

Pilot MCM

Laser + 2 Pin diodes

HDMP 1034

Pixel converter

Pixel control tx

Pixel converter daughter card
Component Status

Pixel chips

Pixel carrier

Pilot MCM

Laser + 2 Pin diodes

GOL

PILOT digital

PIL ana

Pixel control tx daughter card

pixel converter

HDMP 1034
Component Status

Pixel chips

Pixel carrier

PIL
PILOT
GOL
Laser + 2 Pin diodes

Pilot MCM

HDMP 1034
pixel converter
depixel control tx
dpixel converter
dughter card
Component Status

Pixel chips

Pixel carrier

HDMP 1034

Pixel converter
daughter card

pixel converter
digital
GOL
Pilot MCM

Laser + 2 Pin diodes
Component Status

Pixel chips
- Pixel carrier

Pixel converter daughter card

HDMP 1034
- Pixel converter
- Pixel control tx

PIL ana
- PILOT digital
- GOL

Laser + 2 Pin diodes

Pilot MCM
Component Status

Pixel chips

Pixel carrier

PIL

PILOT

digital

GOL

Laser + 2 Pin diodes

Pilot MCM

HDMP 1034

pixel converter
daochild
card

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Component Status

Pixel chips

Pixel carrier

Pilot MCM

Laser + 2 Pin diodes

HDMP 1034

Pixel converter
daughter card

Pixel control tx
Component Status

Pixel chips

Pixel carrier

Pilot MCM

Laser + 2 Pin diodes

HDMP 1034 Pixel converter

pixel control tx
Component Status

Pixel chips

Pixel carrier

Pilot MCM

Laser + 2 Pin diodes

Pixel converter daughter card

HDMP 1034

Pixel converter

Pixel control tx
Component Status

- Pixel chips
- Pixel carrier
- Pilot MCM
- Laser + 2 Pin diodes
- HDMP 1034
- Pixel converter
- Pixel control tx
- Daughter card
Conclusion

• Structured on detector read-out architecture
• Hard physical implementation constraints
• Prototypes exist but not the final versions
• Positive Progress