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The Industrial I/O Pack (IP) Series IP445 module is a bus isolated 32-channel output module. The IP445 provides control for 32 solid state relays which are bipolar and may be used to switch positive or negative voltages. Four units may be mounted on a carrier board to provide up to 128 channels of output control in a single system slot. The IP445 offers a variety of features which make it an ideal choice for many industrial and scientific applications as described below.

### 1.0 GENERAL INFORMATION

**Key IP445 Features**

- **High Channel Count** - Individual control of up to 32 (SPST-NO) bipolar Solid State Relays (SSR’s) is provided. Four units mounted on a carrier board provide 128 channels in a single system slot.
- **High-Speed/0 Wait States** - No wait states are required for all read/write cycles (all cycles complete in 250nS.) and hold states are supported.
- **Optically Isolated** - Individual bipolar SSR’s provide isolation. The IP445 contains four groups (ports) of eight channels which include separate port commons to ensure port to port isolation. Individual ports are isolated from each other and from the IP logic.
- **Low-Side or High-Side Switch Configuration** - Each group of eight channels can be connected directly to positive or negative supplies for high (hot) side switching. Alternatively, each group of eight channels can be connected to common for low side switching. Socketed pull-up resistors are provided for low side switching applications.
- **TTL Compatible** - When configured as a low side switch will sink 27mA at 0.4 volts. Sourcing is controlled by the installed pull-up resistor.
- **Power Up & System Reset is Fail-safe** - For safety, the outputs are turned OFF upon power-up and a system reset. Thus, the SSR’s will be disabled after a power-up or system reset.
- **Wide Range Bipolar Voltage Outputs** - Outputs are rated from 0 to ±60 volts. The bipolar solid state relays allow both AC and DC switching.
- **Output Readback Function** - Readback buffers are provided that allow the output channel registers to be read back.
- **Loopback Compatible with IP440 Digital Input Module** - The P2 field I/O pin assignments of the IP445 output module correspond with those of the Acromag IP440 Bus Isolated Input module. This provides direct closed-loop monitoring of the output states.
• No Configuration Jumpers or Switches - All configuration is performed through software commands with no internal jumpers to configure or switches to set.

INDUSTRIAL I/O PACK INTERFACE FEATURES
• High density - Single-size, industry standard, IP module footprint. Four units mounted on a carrier board provide up to 128 isolated output points in a single system slot. Both VMEbus and ISA bus (PC/AT) carriers are supported.
• Local ID - Each IP module has its own 8-bit ID signature which can be read via access to the ID space.
• 8-bit I/O - Port register Read/Write is performed through 8 or 16-bit data transfer cycles in the IP module I/O space.
• High Speed with No Wait States - Access times for all data transfer cycles are described in terms of "wait" states - 0 wait states are required for all read and write operations of this model. See Specification section for detailed information.

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag AVME9630/9660 3U/6U non-intelligent VMEbus carrier boards). Additionally, Acromag's APC8600 ISA bus (PC/AT) carrier board is also supported. A wide range of other Acromag IP modules are also available to serve your signal conditioning and interface needs.

The following cables and termination panels are also available. Consult your carrier board documentation for the correct interface product part numbers to ensure compatibility with your carrier board.

Cables
Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The "-X" suffix of the model number is used to indicate the length in feet.

The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Model 5029-900 APC8600 High-Density Cable: A 36-inch long interface cable that mates the high-density (25mil pitch) 50-pin I/O connectors of the APC8600 ISA bus carrier board, to the high-density connectors on the APC8600 Termination Panel (described below).

Termination Panels:
Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Model 5029-910 APC8600 High-Density-to-Screw-Terminal Termination Panel: This panel converts the high-density ribbon-cable connectors coming from the APC8600 carrier board (Acromag cable Model 5029-900) to screw terminals, for diret-wired interfaces.

Transition Module:
Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-550 or 5025-551).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. Example software functions are provided for both VMEbus and ISA bus (PC/AT) applications. All functions are written in the "C" programming language and can be linked to your application. For more details, refer to the "README.TXT" file in the root directory on the diskette and the "INFO445.TXT" file in the appropriate "IP445" subdirectory off of "VMEIP" or "PCIP", according to your carrier.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.
CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions. Module IP445 digital output boards have no hardware jumpers or switches to configure. Software configurable control registers are provided for control of all modes of operation. Refer to section 3 for programming details.

This module is built with socketed output pull-up resistors installed. These may be used when the SSR's are applied as low side switches. Resistor values may be changed if needed, and the resistors may be removed for high side switching (see IP445 Resistor Location Drawing 4501-606).

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board).

<table>
<thead>
<tr>
<th>Pin Description Number</th>
<th>Pin Description Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 1 1</td>
<td>Port 1 2</td>
</tr>
<tr>
<td>Port 1 3</td>
<td>Port 1 4</td>
</tr>
<tr>
<td>Port 2 5</td>
<td>Port 2 6</td>
</tr>
<tr>
<td>Port 2 7</td>
<td>Port 2 8</td>
</tr>
<tr>
<td>User Supply 1 9</td>
<td>User Supply 1 10</td>
</tr>
<tr>
<td>User Supply 2 11</td>
<td>User Supply 2 12</td>
</tr>
<tr>
<td>User Supply 3 13</td>
<td>User Supply 3 14</td>
</tr>
<tr>
<td>User Supply 4 15</td>
<td>User Supply 4 16</td>
</tr>
<tr>
<td>User Supply 5 17</td>
<td>User Supply 5 18</td>
</tr>
<tr>
<td>User Supply 6 19</td>
<td>User Supply 6 20</td>
</tr>
<tr>
<td>User Supply 7 21</td>
<td>User Supply 7 22</td>
</tr>
<tr>
<td>User Supply 8 23</td>
<td>User Supply 8 24</td>
</tr>
<tr>
<td>User Supply 9 25</td>
<td>User Supply 9 26</td>
</tr>
</tbody>
</table>

The output channels of this module are divided into four ports of eight channels each. All channels within a port share a common signal connection with each other. Isolation is provided between the ports and the IP logic. In addition, bus isolation is provided between ports.

P2 pin assignments are arranged to be compatible with similar Acromag models. This model is directly loopback compatible with the Acromag Model IP440 32-Channel Digital Input Board. Likewise, pin assignments are identical to those of Acromag Model IP405 40-Channel Digital Output Boards for channels 0-31, except for the user supply connections. This model (remove socketed pull-up resistors) may also interface with industry accepted I/O panels, termination panels, and relay racks when used with the Acromag Model 5025-655 I/O Adapter Card. However, relay racks are usually isolated in which case it would probably be more efficient to use the non-isolated IP405 module. Consult the factory for information on these and other compatible products.

Refer to Drawing 4051-604 for example field output connections. See Drawing 4501-603 for loopback connections to Acromag Model IP440 Input Modules.

Note that the outputs of this module are bipolar, and may be connected in any direction with respect to the port common. Further, do not confuse port commons with signal ground. For the IP445, port common only infers that this lead is connected common to the 8 outputs of the port (a separate common for each port). The port commons of the IP445 output module and IP440 input module are normally not connected together for loopback interconnection (see Drawing 4501-603).
Grounding and Noise Considerations

Output lines of the IP445 are optically isolated between the logic and field output connections. Likewise, separate port commons ensure port-to-port isolation. Consequently, the field I/O connections are isolated from the carrier board and backplane, thus minimizing the negative effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations to avoid inadvertently compromising isolation, or creating ground loops which can cause noise pickup and reduce overall system reliability.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2). The IP Logic Interface connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly.

Table 2.2: Standard Logic Interface Connections (P1)

<table>
<thead>
<tr>
<th>Pin Description</th>
<th>Number</th>
<th>Pin Description</th>
<th>Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>1</td>
<td>GND</td>
<td>26</td>
</tr>
<tr>
<td>CLK</td>
<td>2</td>
<td>+5V</td>
<td>27</td>
</tr>
<tr>
<td>Reset*</td>
<td>3</td>
<td>R/W*</td>
<td>28</td>
</tr>
<tr>
<td>D00</td>
<td>4</td>
<td>IDSEL*</td>
<td>29</td>
</tr>
<tr>
<td>D01</td>
<td>5</td>
<td>DMAReq0*</td>
<td>30</td>
</tr>
<tr>
<td>D02</td>
<td>6</td>
<td>MEMSEL*</td>
<td>31</td>
</tr>
<tr>
<td>D03</td>
<td>7</td>
<td>DMAReq1*</td>
<td>32</td>
</tr>
<tr>
<td>D04</td>
<td>8</td>
<td>IntSel*</td>
<td>33</td>
</tr>
<tr>
<td>D05</td>
<td>9</td>
<td>DMAck0*</td>
<td>34</td>
</tr>
<tr>
<td>D06</td>
<td>10</td>
<td>IOSEL*</td>
<td>35</td>
</tr>
<tr>
<td>D07</td>
<td>11</td>
<td>RESERVED</td>
<td>36</td>
</tr>
<tr>
<td>D08</td>
<td>12</td>
<td>A1</td>
<td>37</td>
</tr>
<tr>
<td>D09</td>
<td>13</td>
<td>DMAEnd*</td>
<td>38</td>
</tr>
<tr>
<td>D10</td>
<td>14</td>
<td>A2</td>
<td>39</td>
</tr>
<tr>
<td>D11</td>
<td>15</td>
<td>ERROR*</td>
<td>40</td>
</tr>
<tr>
<td>D12</td>
<td>16</td>
<td>A3</td>
<td>41</td>
</tr>
<tr>
<td>D13</td>
<td>17</td>
<td>INTReq0*</td>
<td>42</td>
</tr>
<tr>
<td>D14</td>
<td>18</td>
<td>A4</td>
<td>43</td>
</tr>
<tr>
<td>D15</td>
<td>19</td>
<td>INTReq1*</td>
<td>44</td>
</tr>
<tr>
<td>BS0*</td>
<td>20</td>
<td>A5</td>
<td>45</td>
</tr>
<tr>
<td>BS1*</td>
<td>21</td>
<td>STROBE*</td>
<td>46</td>
</tr>
<tr>
<td>-12V</td>
<td>22</td>
<td>A6</td>
<td>47</td>
</tr>
<tr>
<td>+12V</td>
<td>23</td>
<td>ACK*</td>
<td>48</td>
</tr>
<tr>
<td>+5V</td>
<td>24</td>
<td>RESERVED</td>
<td>49</td>
</tr>
<tr>
<td>GND</td>
<td>25</td>
<td>GND</td>
<td>50</td>
</tr>
</tbody>
</table>

An Asterisk (*) is used to indicate an active-low signal.

**BOLD ITALIC** Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

IP IDENTIFICATION SPACE - (Read Only, 32 Odd-Byte Addresses)

Each IP module contains identification (ID) information that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID space. Fixed information includes the “IPAC” identifier, model number, and manufacturer’s identification codes. Variable information includes unique information required for the module. The IP445 ID information does not contain any variable (e.g. unique calibration) information. ID space bytes are addressed using only the odd addresses in a 64 byte block (on the “Big Endian” VMEbus). Even addresses are used on the “Little Endian” PC ISA bus. The IP445 ID space contents are shown in Table 3.1. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID space. Execution of an ID space read requires 0 wait states.

Table 3.1: IP445 ID Space Identification (ID) ROM

<table>
<thead>
<tr>
<th>Hex Offset</th>
<th>From ID ROM Base Address</th>
<th>ASCII Character Equivalent</th>
<th>Numeric Value (Hex)</th>
<th>Field Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>I</td>
<td>49</td>
<td>All IP’s have ‘IPAC’</td>
<td></td>
</tr>
<tr>
<td>03</td>
<td>P</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>05</td>
<td>A</td>
<td>41</td>
<td></td>
<td></td>
</tr>
<tr>
<td>07</td>
<td>C</td>
<td>43</td>
<td></td>
<td></td>
</tr>
<tr>
<td>09</td>
<td>A3</td>
<td>Acromag ID Code</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0B</td>
<td>09</td>
<td>IP Model Code</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0D</td>
<td>00</td>
<td>Not Used (Revision)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F</td>
<td>00</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>00</td>
<td>Not Used (Driver ID Low Byte)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>00</td>
<td>Not Used (Driver ID High Byte)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>0C</td>
<td>Total Number of ID ROM Bytes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>8C</td>
<td>CRC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19 to 3F</td>
<td>yy</td>
<td>Not Used</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes (Table 3.1):
1. The IP model number is represented by a two-digit code within the ID space (the IP445 model is represented by 09 Hex).
2. Execution of an ID space read requires 0 wait states.
I/O SPACE ADDRESS MAP

This board is addressable in the Industrial Pack I/O space to control the 32 channels of digital output to the field.

The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1 to A6, but the IP445 uses only a portion of this space. The I/O space address map for the IP445 is shown in Table 3.2. Note that the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. Accesses may be performed on an 8 or 16-bit basis but only D0-D7 are driven. D08-D15 are not used but will normally read high due to pull-up resistors on the carrier board.

The following table shows the memory map for the IP445. Data is read and written to one of four groups (ports) as designated by the address.

Table 3.2: IP445 I/O Space Address (Hex) Memory Map

<table>
<thead>
<tr>
<th>Base Addr+</th>
<th>D15</th>
<th>MSB</th>
<th>D08</th>
<th>D07</th>
<th>LSB</th>
<th>D00</th>
<th>Base Addr+</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00</td>
</tr>
<tr>
<td>02</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>02</td>
</tr>
<tr>
<td>04</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>04</td>
</tr>
<tr>
<td>06</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>06</td>
</tr>
<tr>
<td>08</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>08</td>
</tr>
<tr>
<td>0A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0A</td>
</tr>
<tr>
<td>7E</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>7E</td>
</tr>
</tbody>
</table>

Notes (Table 3.2):
1. The IP will not respond to addresses that are "Not Used".
2. All Register accesses implement 0 wait state data transfers.

This memory map reflects byte accesses using the “Big Endian” byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. The Intel x86 family of microprocessors uses the opposite convention, or “Little Endian” byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, installation of this module on a PC carrier board will require the use of the even address locations to access the lower 8 data bits while on a VMEbus carrier use of odd address locations are required.

REGISTER DEFINITIONS

Control Register, (Write) - (Base + 00H)

This write only register is used to reset all output ports to 0 (SSR switches OFF).

Table 3.3: Control Register

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1 = Software Reset</td>
</tr>
<tr>
<td>1 to 7</td>
<td>Not Used</td>
</tr>
</tbody>
</table>

Port Output Registers (Read/Write, 03H, 05H, 07H, and 09H)

Four registers are provided to control 32 possible output points. Data can be read from or written to one of four groups of eight output lines (Ports 0-3), as designated by the address and read/write signals. Each port assigns the least significant data line (D0) to the least significant output line of the port grouping (e.g. OD0 for port 0 to D0).

Table 3.3: Control Register

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1 = Software Reset</td>
</tr>
<tr>
<td>1 to 7</td>
<td>Not Used</td>
</tr>
</tbody>
</table>
4.0 THEORY OF OPERATION

This section contains information regarding the basic functionality of the circuitry used on the IP445. Refer to the Block Diagram shown in Drawing 4501-605 as you review this material.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). The P1 interface also provides +5V power to the module. Note that data lines D08..D15, BS1*, the DMA control, interrupt requests (INTREQ0+ and INTREQ1+), ERROR+, STROBE+ and +/-12V power signals are not used.

A Field Programmable Gate-Array (FPGA) installed on the IP Module provides an interface to the carrier board per IP Module specification revision 0.7.1. The interface to the carrier board allows complete control of all IP445 functions. This logic includes: address decoding, I/O and ID read/write control circuitry, and ID space implementation. With regard to throughput, 0 wait states are required for read and write operations.

Address decoding of the six IP address signals A(1:6) is implemented in the FPGA, in conjunction with the IP select signals, to identify access to the IP module’s ID or I/O space. In addition, the byte strobe BS0+ is decoded to identify a low byte data transfer.

OUTPUT PORTS

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.1). Individual Solid State Relays (SSR’s) for each channel isolate the field from the control logic for the IP445. Channels are isolated from each other in groups of eight. There are eight channels to a group or port. Because the output lines of a single port share a common connection, individual outputs are not isolated from each other within the same port. However, separate port commons are provided to facilitate port-to-port isolation.

32 Single Pole Single Throw - Normally Open (SPST-NO, “1 Form A”) SSR outputs are controlled by this module. Each group of eight channels can be connected directly to positive or negative supplies for high (hot) side switching. Alternatively, each group of eight channels can be connected to common for low side switching. Socketed pull-up resistors are provided for low side switching applications. These resistors should be removed if high side switching is needed. In low side switching applications the resistor values can be changed (e.g. lower values will provide a faster pull-up while a higher values will keep power dissipation from becoming a problem at higher voltages) - see Specifications in Chapter 6 for details.

The SSR’s are controlled by output registers within the FPGA. Writing a ‘1’ to the output register will turn the switch ON (closed-circuit) while writing a ‘0’ will turn it OFF (open-circuit). Readback of the output state is accomplished by reading the output registers. However, for complete confidence in output control, loopback should be performed. This may be accomplished using the IP440 isolated digital input module (refer to drawing 4501-603).

The SSR’s employed are rated for a much higher voltage than specified. However, the field connector and printed circuit board foil spacings limit applied voltages to +/-60VDC or AC peak. Each port (group of eight channels) has a single common. Since the connectors and cables are rated to 1A maximum per pin, then each port is limited to that total current. Thus, the sum of currents conducted by the 8 channels must stay below that total (see specifications in Chapter 6 for details). The low on resistance of the SSR’s helps reduce their power dissipation when they conduct high currents; however, given the large number of channels on the board adequate air circulation must be maintained. The SSR’s used in the IP445 are very rugged and contain built-in current limiting for their protection. They provide clean, bounce free switching and can replace electromechanical relays in many applications. SSR switching speeds are comparable to electromechanical relays (1mS typical) but are slow compared to high speed optocouplers.

Output operation is “Fail-safe”. That is, the outputs are always OFF upon power-up reset, and are automatically cleared following a software (control register) or system software reset. This is done for safety reasons to ensure reliable control of the output state under all conditions.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag’s Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag’s Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.
6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

Operating Temperature.................0 to +70°C.
-40 to +85°C (E Version)
Relative Humidity..........................5-95% non-condensing.
Storage Temperature....................-40 to +125°C.

Physical Configuration.............Single Industrial I/O Pack Module.
Length....................................3.880 inches (98.5 mm).
Width.....................................1.780 inches (45.2 mm).
Board Thickness....................0.062 inches (1.59 mm).
Max Component Height..........0.314 inches (7.97 mm).

Connectors:
P1 (IP Logic Interface)............50-pin female receptacle header
(AMP 173279-3 or equivalent).
P2 (Field I/O)..........................50-pin female receptacle header
(AMP 173279-3 or equivalent).

Power Requirements:
+5 Volts (±5%) All On.............300mA, Typical
400mA, Maximum.
+5 Volts (±5%) All Off.............8.5mA, Typical
12mA, Maximum.
±12 Volts (±5%) from P1......0mA (Not Used).

Isolation..............................Logic and field connections are
optically isolated by SSR’s.  Individual ports are also iso-
lated from each other.  However, output lines of individual ports
share a common connection and are not isolated from each other.  Separate port commons are
provided to facilitate port-to-port isolation.  IP Logic and field lines are isolated from each other for
voltages up to 250VAC, or 354V DC on a continuous basis (unit will withstand a 1250V AC
dielectric strength test for one second without breakdown).  This complies with test requirements
outlined in ANSI/ISA-S82.01-1988 for the voltage rating specified.  Port to port isolation is
less critical and is specified as 100V DC.

Isolation Spacing......................Printed circuit board minimum
isolation spacings are as follows:
Port-to-Logic:
0.024" Minimum (inner layer),
0.071" Minimum (external layer).
Port-to-Port:
0.012" Minimum (inner layer),
0.040" Minimum (external layer).

DIGITAL (SSR) OUTPUTS

Output Channel Configuration.......32 isolated Solid State Relay
(SSR) outputs supporting AC
or DC (high or low side
switching) operation.
SPST-NO, “1 Form A” contacts.

“OFF” Voltage Range.............0 to +/-60V DC or peak AC.
Output “OFF” Leakage Current.......1uA Maximum (over temp.).
Output “ON” Current Range...........140mA Maximum continuous
(up to 1A total per port)
No deration required at elevated
ambient conditions.

Output ON Resistance..............15Ω. Maximum (25°C).
Output Current Limiting.............480mA Maximum.
Turn-ON Time..........................1mS. Typical, 2mS. Maximum.
Turn-OFF Time..........................1mS. Typical, 2mS. Maximum.
Reset Condition.....................All output SSR’s OFF.
Output Pull-up Resistors.........Socketed 4.7KΩ (used in low
side switching applications).
See 4501-606: Res. Loc. Dwg,
Calculate resistor power for user
supplied voltage (Power = V²/R).
Limit power to 0.1 Watt per
resistor (21.7V max. @ 4.7KΩ).
Remove or insert higher value
(consult factory) for higher
voltages.  Install lower value
(check power) to obtain faster,
stronger pull-up.  Remove for
high side switching applications.

TTL Compatibility......................Yes, used as low side switch can
sink 27mA. @ 0.4V Maximum;
source 500uA @ 2.4V Min. with
4.7KΩ pull-up to 5V supply.

Resistance to RFI..............No digital upsets occur for field
strengths up to 10V per meter at
27MHz, 151MHz, & 460MHz per
SAMA PMC 33.1 test procedures.

Resistance to EMI...............Unit has been tested with no
digital upsets under the influence
of EMI from switching solenoids,
commutator motors, and drill
motors.

ESD Protection......................Output lines are protected from
ESD voltages to ±4KV, typical.
May degrade 4.7K pullups by
approximately 5%.

INDUSTRIAL I/O PACK COMPLIANCE

Specification.........................This module meets or exceeds all
written Industrial I/O Pack
specifications per revision 0.7.1.

Electrical/Mechanical Interface.....Single-Size IP Module.
IP Data Transfer Cycle Types Supported:
Input/Output (IOSel*).............D16 or D08 least significant
read/write of port data.
ID Read (IDSel*).............32 x 8 ID ROM read on D0..D7.
Access Times (8MHz Clock):
ID ROM Read......................0 wait states (250ns cycle).
Port Registers (R/W)..............0 wait states (250ns cycle).
APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The `-x` suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors).

Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.

Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).

Headers (Both Ends): 50-pin female header with strain relief. Strain Relief - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).

Keying: Headers at both ends have polarizing key to prevent improper installation.

Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.

Shipping Weight: 1.0 pound (0.5Kg) packaged.

CABLE: MODEL 5029-900

Type: Model 5029-900 APC8600 High-Density Cable: A 36-inch long interface cable that mates the high-density (25mil pitch) 50-pin I/O connectors of the APC8600 PC/AT ISA bus carrier board, to the high density connectors on the APC8600 Termination Panels (described below).

Application: Used with the APC8600 PC carrier and termination panel. It mates the high-density (25mil pitch) 50-pin I/O connectors of the APC8600 PC/AT ISA bus carrier board, to the high density connectors on the APC8600 Termination Panel (described below).

Length: 36-inches

Cable: 50-wire flat ribbon cable, 28 gage, Non-Shielded, T&B Ansley Part 135-051 or equivalent.


Keying: Headers at both ends have polarizing key to prevent improper installation.

Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660 Boards

Application: To connect field I/O signals to the Industrial I/O Pack (IP). Termination Panel: Acromag Part 4001-040 (Phoenix Contact Type FLM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP).

Connections to AVME9630/9660: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.

Mounting: Termination panel is snapped on the DIN mounting rail.

Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +100°C.

Storage Temperature: -40°C to +100°C.

Shipping Weight: 1.25 pounds (0.6kg) packaged.

TERMINATION PANEL: MODEL 5029-910

Type: Screw-Terminal Termination Panel For Acromag APC8600 PC/AT ISA bus Carrier Boards.

Application: This panel converts the high-density ribbon-cable connectors coming from the APC8600 carrier board (Acromag cable Model 5029-900) to screw terminals, for direct-wired interfaces. This panel facilitates the connection of up to 50 field I/O signals and connects to the APC8600 PC/AT ISA bus carrier board via high-density (25-mil pitch) flat ribbon cable and connectors (see cable Model 5029-900). The A & B connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.

Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.

Connections to APC8600: P1, 50-pin, high-density male header with strain relief.

Mounting: Termination panel includes mounting holes.

Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +85°C.

Storage Temperature: -55°C to +125°C.

Shipping Weight: 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.

Application: To repeat field I/O signals of IP modules for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-551X).

Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).

Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-551-X).

Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.

Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +85°C.

Storage Temperature: -55°C to +105°C.

Shipping Weight: 1.25 pounds (0.6Kg) packaged.
ASSEMBLY PROCEDURE:

1. Threaded spacers are provided in two different lengths. The shorter length is for use with A&W 9850/9650 carrier boards (shown). Check your carrier board to determine its requirements. Mounting hardware provided may not be compatible with all types of carrier boards.

2. Insert flat head screws (item A) through solder side of IP module and into hex spacers (item B) and tighten (4 places) until hex spacer is completely seated.

3. Carefully align IP module to carrier board and press together until connectors and spacers are seated.

4. Insert pan head screws (item C) through solder side of carrier boards and into hex spacers (item B) and tighten (4 places).

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY
IP445 PULLUP RESISTOR LOCATION DRAWING
FOR REMOVAL AND REPLACEMENT WHERE REQUIRED

NOTES CONCERNING SOCKETED PULLUP RESISTORS R5–R8:

1. ALL OUTPUT PORTS INCLUDE 4.7K OHM PULLUP RESISTORS
   TO THE USER SUPPLY FOR EACH PORT IN THE FORM
   OF SIP RESISTORS AS SHOWN. THESE SIP RESISTORS
   ARE INSTALLED IN SOCKETS AND MAY BE MODIFIED AS REQUIRED.

2. R5–R8 ARE USED IN LOW SIDE SWITCHING APPLICATIONS
   ONLY (REMOVE WHEN SSR’s ARE USED IN HIGH
   (HOT) SIDE SWITCHING APPLICATIONS).

3. SEE CHAPTER 6 “SPECIFICATIONS” FOR MORE INFORMATION
   ON PULL-UP RESISTOR VALUE CHANGES.

PULL-UP RESISTOR SIPS ARE
MOUNTED IN SOCKETS AND
CAN BE REMOVED IF REQUIRED.
RESISTOR SIPS ARE
DIVIDED AS SHOWN

<table>
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<th>SIP</th>
<th>VALUE</th>
<th>FUNCTION</th>
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<td>GD07..0000 PULLUP</td>
<td>PORT 0</td>
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<td>4.7K OHM</td>
<td>GD08..0015 PULLUP</td>
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<tr>
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<td>GD23..0016 PULLUP</td>
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<tr>
<td>R8A..R8.H</td>
<td>4.7K OHM</td>
<td>GD24..0031 PULLUP</td>
<td>PORT 3</td>
</tr>
</tbody>
</table>
IP445 OUTPUT TO IP440 INPUT LOOPBACK CONNECTIONS

NOTE THAT FOR LOOPBACK PURPOSES, THE COMMON LINE OF AN IP440 PORT AND THE COMMON LINE OF AN IP445 PORT DO NOT NECESSARILY CONNECT TOGETHER.

THE IP440 & IP445 INCLUDE 4 PORTS OF 8 CHANNELS EACH. EACH PORT SHARES A PORT COMMON. SEPARATE PORT COMMONS FACILITATE PORT TO PORT ISOLATION. THE IP445 ALSO INCLUDES SEPARATE PORT SUPPLY PINS FOR CONNECTING TO THE ON-BOARD PULLUPS.

IP440 SIMPLIFIED INPUT CHANNEL

- CARRIER BOARD
- DIGITAL ASIC
- ISOLATED INPUT
- INPUTS ARE BIPOLAR
- IN31
- EARTH GROUND CONNECTION IS USUALLY MADE AT CAGE POWER SUPPLY.
- INPUT VOLTAGE RANGE:
  - IP440-1: +/- (4-18V) DC OR AC PEAK
  - IP440-2: +/- (16-48V) DC OR AC PEAK
  - IP440-3: +/- (38-60V) DC OR AC PEAK

IP445 SIMPLIFIED OUTPUT CHANNEL

- SUPPLY
- OUTPUT VOLTAGE: 60V MAXIMUM
- FPGA
- CARRIER BOARD
- DIGITAL COMMON (TYP)
- OUTPUTS ARE BIPOLAR
- IN31
- EARTH GROUND CONNECTION IS USUALLY MADE AT CAGE POWER SUPPLY
- NOTE: FOUR PORTS OF 8 CHANNELS ARE PROVIDED. SEPARATE PORT COMMONS AND PULLUP SUPPLY PINS ENSURE PORT-TO-PORT ISOLATION.
MODEL 5025–552 TERMINATION PANEL SCHEMATIC

TOP VIEW

SIDE VIEW

Screwdriver slot for removal from "T" rail.

NOTES:
Dimensions are in inches (millimeters).
Tolerance: ±0.625 ±0.5.

MODEL 5025–552 TERMINATION PANEL

Acromag®

WIXOM, MICH.

DATE
REV.
ECN.
DR.
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CLIP.

No.

SERIES

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