Interface board testing

Xuedong Chai
U. of Iowa

Final Design Review
Interface Testing: Overview

Upgrade system

TIOM → TSF → BLT → GLT

Neighbor Data

GLINK

LVDS

ZPD → IFT → EMT
Interface Testing: Overview

- The testing involves assorted parts of overall system tests, not only the interface boards themselves (PCB assembly, firmware), but also the cables, backplane, and I/O function of each DCT board.

- Test strategy:
  - Visual inspection for component loading and power up
  - Interface firmware pattern test,
  - Diagnostic memory playback test,
  - DCH track pattern calibration test,
  - Cosmic run test in IR2
GLTi: GLT->GLTi->GLT self-looping test

GLTi

- IFR
- BLT
- EMT
- PTD
- ZPD
- Xilinx switch

3 bits
2x16
10x9
8x2
8x6

GLT

- Output memory
- Input memory

24 bits

Test Box

Oscilloscope

April 11, 2003 for FDR
Xuedong Chai
**GLTi:** GLT->GLTi->GLT self-looping test (2)

- **Reason:** The Glti receives data from all subsystems, it is almost impossible to validate each input with a real system component input.
- **Test Pattern:** Single patterns toggling every single bit.
- **Result:** Up to $10^3$-$10^4$ signal bits per trace, no error.
GLT{i: Cosmic Run Test in IR2

Since New GLTi board is compatible with old DCT system, we can install it at ir2, and use one cosmic run to test our New Glti board:

• All the signal looks OK, signal distribution is like the other run with old GLTi board
• Input DAQ data puzzling, under investigation.
• Identify one problem with the IFT signals, already fixed.
TSFi: TSFi->ZPDi->ZPD with Tsfi firmware pattern test

Test Pattern is created by TSFi Firmware; Frame bit checking logic added into ZPDi firmware.

Preliminary conclusion:

• No problem with pin connection
• LVDS works
• Having a clean ZPD clock is quite important
**TSFi: DCH->TSFi->TSF**

- The independent DCH and DCT Teststands are first combined together outside IR2, more test flexibility than before.
- Now, DCH-DCT Track Pattern Calibration is prepared, and test setup shown in the left figure.
ZPDi Test

- ZPDi pattern test has been done by Eunil, no problem on backplane and input memory, for detail, see his talk
- ZPD->GLT test is in preparation
Summary

- Most of GLTi test has been done
- TSF->ZPD test is in progress
- DCH->DCT track pattern calibration is in progress
- TSF neighbor data test hasn’t begun.
- TSF->BLT test hasn’t begun
- Slow monitoring testing is in progress