ZPD Prototype Tests and DAQ Implementation

BABAR L1 DCT Upgrade FDR

Eunil Won
For Harvard ZPD crews

- Introduction
- Prototype Tests
  - Electrical Signals
  - FPGA Configuration
- DAQ Memory
Printed Circuit Board

- **Two prototypes** were assembled (May 2002)
- Power connection vias **unconnected** in PCB (Layout software bug)
  - Extra wires jumped for prototypes
- Clock Signals on Decoder Driver **routed incorrectly** to normal I/O
  - To be fixed in the production version
- One arrived at SLAC (July 2002)

**power on: no smoke and it booted successfully!**
Flow of Signals in ZPD

Six Algorithm Engines

Algorithm Engine

Algorithm Engine

Decision Module

“Megabus” (74:0)

Decoder Driver

Segments (152:0) 60 MHz

Frame (8:0)

Segments (152:0)

J1

J2

J3

C/D link

C/D clock

“Minibus” (15:0)

Decision (11:0) \( \times 6 \)

: memory access

30 MHz

30 MHz

Fit Results (11:0) \( \times 6 \):

to Decision Module

30 MHz

Decision (7:0)

30 MHz 8 MHz

60 MHz

120 MHz

Not shown: signals to LEDs, Logic Analyzer ports...
Prototype Testing

Testing prototype boards involve

• **PCB level tests**
  - Does it boot?
  - All signals are connected?
  - Crosstalk (in segments/Megabus)?

• Firmware level tests
  - Fast Control commands functional?
  - Memory read/write OK?
  - **Algorithm works/ fits?** (Stephen’s talk)

Two crucial steps toward production
Testing Signals

From ZPDi to ZPD (Decoder Driver)

Test Patterns from ZPDi

Record segment patterns into memory and check contents...
(Automatically involves partial test of fast control and memories)

Tested up to $10^{10}$ bits/trace and no errors found (limited by software speed)

Frame bit

Segment #

Decoder Driver

Diagnostic Memory

Segment (152:0)

J1 / J2

60 MHz
Testing Signals

From **Decoder Driver** to **Algorithm Engines** ("The Megabus Test")

- Six Algorithm Engines
- Megabus (74:0)

- This test is **one of most important** (runs at **120 MHz**) **pieces to confirm**
- A dedicated firmware was written for this particular test (N. Felt @ Harvard)

Up to $10^{13}$ bits/trace with no errors

Out of 75, 5 bits are reserved for future usage
Testing Signals

From **Algorithm Engines** to **Decision Module** (six buses (11:0)) and **Decision bits** to **ZPDi**

All bits were tested with no errors
Miscellaneous

• Memory access bus ("minibus") tested with $10^8$ read/writes

• Also Tested (partially):
  ✓ 47 LEDs (front panel)
  ✓ C/D clock, C/D link
  ✓ L1Accept, L1Accept Buffer (1:0)
  ✓ Read_Event, Read_Event Buffer (1:0)
  ✓ JTAG to SystemACE, SystemACE to FPGAs
  ✓ Logic Analyzer ports
  ✓ Extra bus with 8 bits (reserved) connected to all FPGAs ("xbus")

All tested with no errors
# Summary of PCB level Tests

<table>
<thead>
<tr>
<th>Component</th>
<th>Total Width</th>
<th>Speed (MHz)</th>
<th>Bits/ trace Tested</th>
</tr>
</thead>
<tbody>
<tr>
<td>Segments</td>
<td>153</td>
<td>60</td>
<td>$10^{10}$</td>
</tr>
<tr>
<td>Megabus</td>
<td>75</td>
<td>120</td>
<td>$10^{13}$</td>
</tr>
<tr>
<td>Fit Results</td>
<td>6x12</td>
<td>30</td>
<td>$10^{6}$</td>
</tr>
<tr>
<td>Minibus</td>
<td>16+5</td>
<td>30</td>
<td>$10^{8}$</td>
</tr>
<tr>
<td>Decisions</td>
<td>8</td>
<td>8</td>
<td>$10^{1}$</td>
</tr>
<tr>
<td>DAQ</td>
<td>6</td>
<td>30</td>
<td>$10^{1}$</td>
</tr>
<tr>
<td>Control</td>
<td>~10</td>
<td>30</td>
<td>$10^{3}$</td>
</tr>
</tbody>
</table>

Two most critical items:
- Tested "by hand"
FPGA Configuration

• Prototype originally used Xilinx System ACE MPM
  - One-piece solution for multi-FPGA configuration
    - Suffered from mysterious bugs – Immature technology?
    - ~1 hour to reprogram ZPD → 1 shift for 8 boards

• Switched to System ACE CF (Compact Flash)
  - Flexible, inexpensive and fast to reprogram: < 20 seconds
  - Tested on prototype with an add-on card → Great success
FPGA Configuration

For prototypes, the add-on goes in JTAG socket on front panel

Production: we will have all the patch on board

(Necessary artworks etc all done)
**DAQ Memory**

16 bit wide

<table>
<thead>
<tr>
<th>2 words</th>
<th>Header (tag, counter, CSR)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 words x 8 ticks</td>
<td>TSF input mask bits (0:152) of eight CLK4 ticks</td>
</tr>
<tr>
<td>25 words x 8 ticks</td>
<td>Fit results ($z_0, \delta z_0, \rho, \tan \lambda$) and trigger decisions (0:7) of eight CLK4 ticks</td>
</tr>
</tbody>
</table>

- In total, it amounts to **566 bytes/event/board**
  (cf GLT: 583 bytes/event)

- **Firmware written and under testing**
  - Bug fixes are in progress
  - Tests with high rate L1 triggers need to be done
Summary

• All the **PCB** level tests demonstrated
  - **No showstoppers** for the production

• **We do have modifications** to make
  - Fix power vias
  - Correct clock routings to Decoder Driver
  - Replace FPGA configuration method

• **DAQ Memory**
  - Firmware written and under testing
  - Tests with high rate L1 triggers are planned

• **Next big hurdle: Algorithm**
  → Stephen’s Talk