ZPD Project Overview

* **BABAR L1 DCT Upgrade FDR**

  Masahiro Morii  
  Harvard University

- Design Overview
- Progress and Changes since CDR
- Current Status
- Plans for Production and Testing
Z \ p_T \ Discriminator = ZPD

- ZPD is a 3-D enhanced version of the PTD
  - Finds tracks and fit them to helix
  - Measures p_T, dip angle (\lambda) and z_0
  - Primary usage: Cut on |z_0| to remove background
Block Diagram (Super-Simplified)

ZPDi

153 segments

Receiver /Driver

MegaBus

Algorithm Engine 0
hm 1
hm 2
hm 3
hm 4
hm 5

Fit Results

Decision Module

4 to GLT

8-bit decisions

Memory access, DAQ control, etc.

FPGA Config

C-link

D-link

FCC Decoder
Inputs

- Each ZPD receives data from 9 TSFs
  - 3/8 in $\phi$
  - Seed segments in the middle 1/8 of SL7 and SL10
- 14 bits $\times$ 153 segments/CLK4

- Challenge 1: Moving around 8 Gbit/s
  - Backplane: 153 pins @ 60 MHz
  - Megabus: 75 LVDS pairs @ 120 MHz

1: mask
4: cell location
6: $\phi$ in the cell
3: error in $\phi$

144 used

Up to 12 seeds

Eunil’s talk
Algorithm Engines

- Algorithm largely unchanged since CDR
  - Finder selects combination of segments \( \rightarrow \) Seed tracks
  - Fitter does 3-D helix fitting \( \rightarrow \) \( z_0, p_T, \tan \lambda \)
- Algorithm Engines = Xilinx Virtex II 4000
  - Each AE handles 2 seeds/CLK4 \( \rightarrow \) 12 seeds/CLK4 total
- Challenge 2: Implementing the Algorithm
  - Does it fit in the chip?
  - Does it run fast enough?
  - Clock margin?
  - Latency < 8 CLK4s

Stephen’s talk
Outputs and Interface

- Output to GLT: 4 bit decisions/CLK4
  - Decision Module FPGA makes 8 decisions
  - Programmable cuts on $z_0$, error on $z_0$, $p_T$ and $\tan\lambda$
- DAQ data: 566 bytes/event
  - Mask bits (exist or not) for 153 TSF segments/CLK4
  - $z_0$, error on $z_0$, $p_T$ and $\tan\lambda$ for 12 tracks/CLK4
  - 8-bit decisions/CLK4
- Diagnostic memories help debugging
- Fast Control interface talks to BABAR online system

Eunil’s talk
Progress Since CDR

- Prototype has been built (May 2002) and tested
  - 2 working modules – 1 at SLAC, 1 at Harvard
  - I/O and buses have been fully validated
  - Algorithm Engines *almost* do what they’re supposed to do

- Problems & inconveniences found and fixed
  - Unconnected vias due to layout software bug
  - Choice of clock input pins on FPGA
    - Move them to special pins that guarantee timing
  - FPGA configuration method
    - Switch to use Compact Flash memory

Eunil’s talk
Are the FPGAs Right?

- Algorithm fits comfortably

<table>
<thead>
<tr>
<th></th>
<th>Decoder/Driver</th>
<th>Algorithm Engine</th>
<th>Decision Module</th>
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</thead>
<tbody>
<tr>
<td>CLBs</td>
<td>27%</td>
<td>44%</td>
<td>70%</td>
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<tr>
<td>RAMs</td>
<td>15%</td>
<td>74%</td>
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<td>Multipliers</td>
<td>0%</td>
<td>20%</td>
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</table>

- Speed is sufficient
  - Firmware meets 60.5 MHz constraint
  - Tested to work up to 67 MHz
  - Latency 2 µs → Meets the specification

Stephen’s talk
Current Status

- Firmware coding continues
  - Algorithm bugs at lower-and-lower levels
    - Goal: bit-wise match with the C++ simulation
  - DAQ memory implementation
    - Mostly done; tests in progress
- PCB is ready for production
  - Design is solid
  - All issues have been fixed in the layout
- All parts are on order or in hand
Production Plan

- After the “green light”
  - Final “paranoid” layout check – 1-2 days
  - PCB production – 2-3 weeks
  - PCB assembly – 2-3 weeks

- Cost for 11 ZPD modules

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<tr>
<th>Function</th>
<th>Part</th>
<th>Qty</th>
<th>$/ea</th>
<th>$/ea*Qty</th>
<th>Fixed</th>
<th>Total</th>
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<td>PCB fab. + tooling</td>
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<td>65.00</td>
<td>715.00</td>
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<td><strong>Total</strong></td>
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<td></td>
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<td></td>
<td></td>
<td>112,222.77</td>
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</table>
Test Plan – Harvard

- Production modules will be tested first at Harvard
  - PC-based test stand has been developed
  - Signal connectivity test to ensure PCB is good
    - Boundary scan
      - Tool in hand, but has not been used
  - Megabus test with special firmware
    - Done on prototype. High statistics ($\sim 10^{13}$ bits/trace)
  - Bus tests using diagnostic memories
    - Done on prototype. Tests memory access & buses
  - Small-scale ($\sim 1000$ simulated events) algorithm test
    - Done on prototype for a few events
Test Plan – SLAC

- More tests follow at SLAC test stand
  - Interface test with ZPDi
    - Done on prototype at $10^{10}$ bits/trace level
  - Algorithm test with higher statistics
    - Can do $10^6$ events easily – Is it useful?
  - System test: integrate with the BABAR DAQ system
    - Work in progress → Gerald’s talk
- Finally, integrate in IR-2…
Following Presentations

- Eunil Won
  - Prototype PCB test results
  - DAQ memories and interface
- Stephen Bailey
  - Algorithm implementation
  - Current issues and problems

We concentrate on what is new since the CDR. Please interrupt for more information.

Checklist before production:

- Is the PCB design correct?
- Is the firmware mature enough to confirm design choices?
- Are there any bugs that require a PCB modification to fix?