ZPD-Engineering issues

- Engineering personnel (Harvard)
- Technical issues
  - High speed bus design
  - Global timing (slide added 9-11-01)
  - PCB issues
  - Ball grid arrays; assembly, rework, reliability
  - Testability; Boundary scan
• Engineering personnel (Harvard)
  • John Oliver Engineer (1/3 FTE)
  • Nathan Felt Engineer (1 FTE)
  • Sarah Harder PC design, tech
  • Jack O’Kane Tech
  • Tom Fries Manufacturing
High speed bus: “MegaBus”

~ 160 bits @ 60 MHz $\Rightarrow$ ~ 10 Gbits/s

Implementation: Virtex II
SSTL2-Stub Series Terminated Logic @ 2.5 V

- Xcite technology - internal terminations, programmable slew rate
- No on board discretes
- Load and source terminations → “clean” edges, high speed
- For 50 Ω trace, ~ 50 mW/signal (20% driver, 80% final Tracker)
- For 160 bits wide @ 60 MHz → 8 Watts
- For 80 bits @ 120 MHz → 4 Watts
- Source termination (~PCI) version is possible, much lower power but expect significantly more ringing → lower speed operation
LVDS_25 – 80 bits @ 120 MHz (or higher)

Slew rate limiting
Back termination

⇒ 80 trace pairs
⇒ 240 external discretes (It fits with 603/402, or TF hybrids)
⇒ Pd = 3.5ma * 2.5 V = 8.5mW/signal
⇒ Pd(total) = 680 mW (mostly in driver)
⇒ Low emi operation

Conclusion: Baseline design is LVDS @ 120 MHz
**Global Timing**

- **Input Data**
- **MegaBus Data, clk**
- **Output Data**

- **Driver Decoder**
- **Tracker Z fitter 1**
- **Tracker Z fitter 2**
- **Tracker Z fitter 3**
- **Tracker Z fitter 4**
- **Tracker Z fitter 5**
- **Tracker Z fitter 6**

- Clk60

- VirtexII DLL allows high resolution clock phasing at Decoder/Driver
  - quadrature clocks @ 120 MHz
  - clk/256 fine phase control
  - Multiple clock domains
  - DLLs not simulatable
- To zeroth order, clk/data phase relationship is correct at Decision Module
- Decision module *could* implement fine phase control for fitters individually.
- We don’t expect that implementing this will be necessary.
Two buses
- LVDS @ 120 MHz and higher
- SSTL @ 60 MHz, 120 MHz, ….
- other i/o standards may be tested as well
- XC2V40, FG256 BGA
- 8 bit circulating pattern
- Tracker s lock onto pattern, test BER (Better be ~ zero!)
PCB Issues I - BGAs

- Virtex II parts available only in BGA
- Issues → Assembly, rework, reliability
- Several vendors investigated (See report for full details)
  - Colonial Electronic Manufacturers, Nashua NH: SMT, BGA assembly
  - Circuit Technology Center, Haverhill Ma.: SMT, BGA rework

CEM
- BGAs applied in same reflow process along with SMTs
- BGA parts must be profiled to establish optimal Temp vs Time for solder reflow
- Profile is established with mechanical samples supplied by Xilinx
- During reflow, balls collapse under weight of part → ball diameter increases.
- BGAs are 100% x-ray inspected. Voids, solder bridges, and un-collapsed balls are readily identified.
- Balls are relatively far apart (1 mm). Solder bridges are almost non-existent.
- CEM experience → Properly profiled BGA assembly is highly reliable, exceedingly low failure rate.
CTC

- Rework specialists: 12,000 sq ft, 40 employees
- BGA rework done on Air-VAC rework equipment

- Parts are profiled prior to re-assembly
- Large BGA on thick board takes ~ 10 min to assemble
- 100% x-ray inspection
- BGAs sent to third party vendor for “re-balling”
- CTC is not an assembly house but could treat our (small) production run as rework.
- Very reliable rework facility
Conclusions:

• For high density, high pin count packages, BGA assembly is the technology of choice.
• It is much more reliable than equivalent pin count peripheral packages. Vendors claim near-zero failure rate.
• Use CEM for assembly, CTC for rework
PCB Structure and Requirements

- MegaBus prototype → 16x16 (1mm) BGA (FG256)
- ZPD → 34x34 (1mm) BGA (FF1152)
- BGA footprint → land matrix with 45 deg offset via matrix
- BGA packages sit on bus → no stubs (except BGA package strays)
- Single 0.006” track between vias
- LVDS pairs → vertical diff stripline between power/gnd planes
- 80 pairs requires 3 layer pairs (~27 signals per pair)
- 12 layer board, thickness 0.008” per layer
- Estimated 65Ω differential bus impedance
LVDS pairs
Power/Gnd planes
BGA Via array
“Exit” routing
LVDS pairs
Electrical test: JTAG boundary scan

- After 100% bare board test + 100% assembly x-ray, we expect exceedingly low failure rate.
- Nonetheless, faults are difficult to find and we favor boundary scan.
- ~ 5000 scannable pins on ZPD
- Software/hardware vendors being investigated
  - Low end: Teradyne Eclipse ($2k), limited to six packages, limited test only
  - High end I: Teradyne Victory ($$$ we can’t afford it)
  - High end II: JTAG Technologies ($7k with substantial educational discount)

- Conclusion: We favor JTAG Technologies product and will investigate further