Trigger Ideas

Masahiro Morii, Harvard U.
for the Trigger Group

- Level 1 DCT upgrade
- Level 2 idea
Level 1 DCT Upgrade

- Idea has been widely discussed.
- L3 rejects many junk events using track $z_0$'s.
- Can we do it in L1?
  - Work with TSF segments.
    - 10 measurements of ~1mm resolution. (c.f. 40 x 140 $\mu$m)
  - Is the resolution enough?
  - Will it be fast enough?
  - How much will it help?
How will we use it?

- Require 1 track from IP (in xyz) on top of various DCT & EMT triggers.
- Expect ~60% reduction of BG events.

<table>
<thead>
<tr>
<th>Current (A)</th>
<th>Lumi ($10^{33}$)</th>
<th>L1 rate (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>HER/LER</td>
<td>Lumi</td>
</tr>
<tr>
<td>Best 2000</td>
<td>0.8/1.1</td>
<td>2.5</td>
</tr>
<tr>
<td>July 2002</td>
<td>1.1/2.8</td>
<td>8.0</td>
</tr>
<tr>
<td>Dec 2003</td>
<td>1.3/3.7</td>
<td>11.7</td>
</tr>
<tr>
<td>w/DCZ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dec 2005</td>
<td>1.5/4.6</td>
<td>33.3</td>
</tr>
<tr>
<td>w/DCZ</td>
<td></td>
<td></td>
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</tbody>
</table>
What’s our limit?

Bunch of things fail between 4 kHz and 5 kHz

This one can be saved only by reducing L1 rate

A. Perazzo
C. O’Grady
Project

- Find an algorithm that gives useful $z_0$.
  - Starting from TSF segments.
  - Possible to implement in L1 $\rightarrow$ Latency!
- Replace TSF and PTD.
  - New DCZ (est. $300k$) replaces PTD.
  - Rebuild TSF (est. $180k$) send axial + stereo layers to DCZ.
  - Interface boards, cables, etc.
- Don’t forget the software!
Algorithm

- A two-stage algorithm being studied.
  - Find TSF segments that form tracks.
  - Fit them to extract $z_0$ (and $\phi_0$, $p_T$, $\tan\lambda$).
- ROOT-based tools help collaborative studies.
- Trying to optimize per-track efficiency and background in the L1 pass through data.
- Track $\rightarrow$ event-level performance studies started using MC.
Ex: track efficiency

- Good IP tracks $\rightarrow$ matching seed track = (97.3±0.1)%
- Good IP tracks $\rightarrow$ accepted by NI Fitter = (83.6±0.3)\%
Ex: event efficiency

Fraction of events with no DCZ tracks.

L1 pass-thru

MC bb events

$p_T$ cut

U. Schwanke
Algorithm status

- Start to see real progress.
  - All aspects (pattern finder, fitter, GLT) covered.
  - Quantitative evaluation has started.
  - Could use more people & alternative ideas.
- Still dangerously late.
- Credible design for CDR requires realistic simulation → Problems with trgDC.
  - Much work jointly with DCH simulation.

A. Borgland, V. Halyo, M. van Hoek
Hardware – TSF

- New TSF sends full stereo info to DCZ.
  - Also sends more segments (1 → 2/supercell?).
  - Significant increase in output signal count.
  - Otherwise straightforward engineering.
  - 24 boards (16 “X” and 8 “Y”) in the system.

- UK group will do the production.
  - Manchester (design, engineering)
  - Bristol (testing) → Will be done at SLAC.
Hardware – TSF

- Work partly started.
  - Original LBNL design transferred to Manchester.
  - Selection of FPGA and cost estimate.
    - Large cost uncertainty to be sorted out.
- Proposal to UK PPESP delayed Jun → Oct.
  - Must make a head start to stay on schedule.
  - Will be a big mess if not approved.

Ensuring PPESP approval is absolutely crucial.
Hardware – DCZ

- DCZ algorithm is implemented in 8 boards.
  - Receive TSF segments → Find IP tracks → Send a φ map to GLT.
- Engineering will be a joint effort
  - Harvard: J. Oliver, N. Felt + 2 physicists.
  - SLAC: G. Haller, TBD + resident physicists.

Optimum use of available resources necessary to meet the aggressive schedule.
Hardware – DCZ

- Difficulties largely in FPGA programming.
  - Expect 40 weeks of VHDL coding.
  - Hope to use many physicists on this.

- Testing
  - Rudimentary board-level testing at Harvard.
  - Full-blown testing at SLAC test stand.
Hardware – Interface

- Back-of-crate cards (TSFi, DCZi) and cables.
  - Production likely at SLAC
  - x5 more signals between TSF and DCZ.
  - Bottleneck = pin count on DCZ backplane.
    - A few ideas exist that reduce data volume
      → need validation.

On the critical path for the entire engineering.
Spec. needs to be fixed NOW.
Software

- **Simulation**
  - Something realistic needed urgently for CDR.
  - Real C++ version by March ’02.
    - Replace trgDC.
    - In time for validating hardware.

- **DAQ/control/test stand software**
  - Iowa group takes the responsibility.

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G. Grenier
**Schedule**

We are late by ~2 months than the originally desired schedule (S. Dong, April ’01)

<table>
<thead>
<tr>
<th>Date</th>
<th>Event Description</th>
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<tbody>
<tr>
<td>Jul 01</td>
<td>Fix interface spec. Start engineering.</td>
</tr>
<tr>
<td>Aug 01</td>
<td>CDR ⇐ Realistic simulation.</td>
</tr>
<tr>
<td>Oct 01</td>
<td>UK PPESP approval.</td>
</tr>
<tr>
<td>Jan 02</td>
<td>Preliminary design complete. Prototype boards.</td>
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<tr>
<td>Mar 02</td>
<td>Prototype testing.</td>
</tr>
<tr>
<td>May 02</td>
<td>Final design complete. Production.</td>
</tr>
<tr>
<td>Sep 02</td>
<td>Installation and commissioning.</td>
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- 4 months later than the original schedule.
- Same target date – Install during 2002 shutdown.
Schedule

- Still possible, but extremely tight.
  - Must watch the first few milestones closely.
    - I/F spec., CDR, PPESP approval, …
  - We have no room for mistakes!
    - First prototype must work with few fixes.
  - Fully effective use of engineering resources.
    - Smart partition of work between institutions.
Level 2 Idea

- L1Acc holds the event in the FEEs
  - Must be followed by ReadData.

- Idea (T. Liu):
  - Data wait for L2Acc in the ROMs.
  - L2Acc initiates FEX.
What generates L2Acc

- A special ROM reads all TSF data before L2Acc, do tracking and generates L2Acc.
  - All what DCZ will do can be done in a CPU.
    - Access to all the TSF segments.
      - No TSF → DCZ cabling limitation.
    - More time (1/L1 rate > 100 μs) available.
  - Very small hardware needed.
    - Send L2Acc from the ROM to the FCTS.
      - Ugly but possible.
Limitations

- Does not help the FEEs and G-links.
  - DCH G-links will fail at ~4kHz.
- Significant development burden on ODF.
  - Intrusive modifications to the working, delicate, real-time system.
  - Dataflow group has no extra manpower to divert from their on-going development.
Summary

- Level-1 DCT upgrade is making progress.
  - Schedule is very tight but possible.
    - Optimal use of resources is needed.
  - Manpower improved → All aspects covered.

- Critical items for the next few months:
  - Interface specification → Start engineering.
  - CDR with credible prelim. design in August.
  - UK funding: PPESP October.

- Level-2 idea should be pursued in parallel.
  - Not as an alternative to the L1 upgrade.