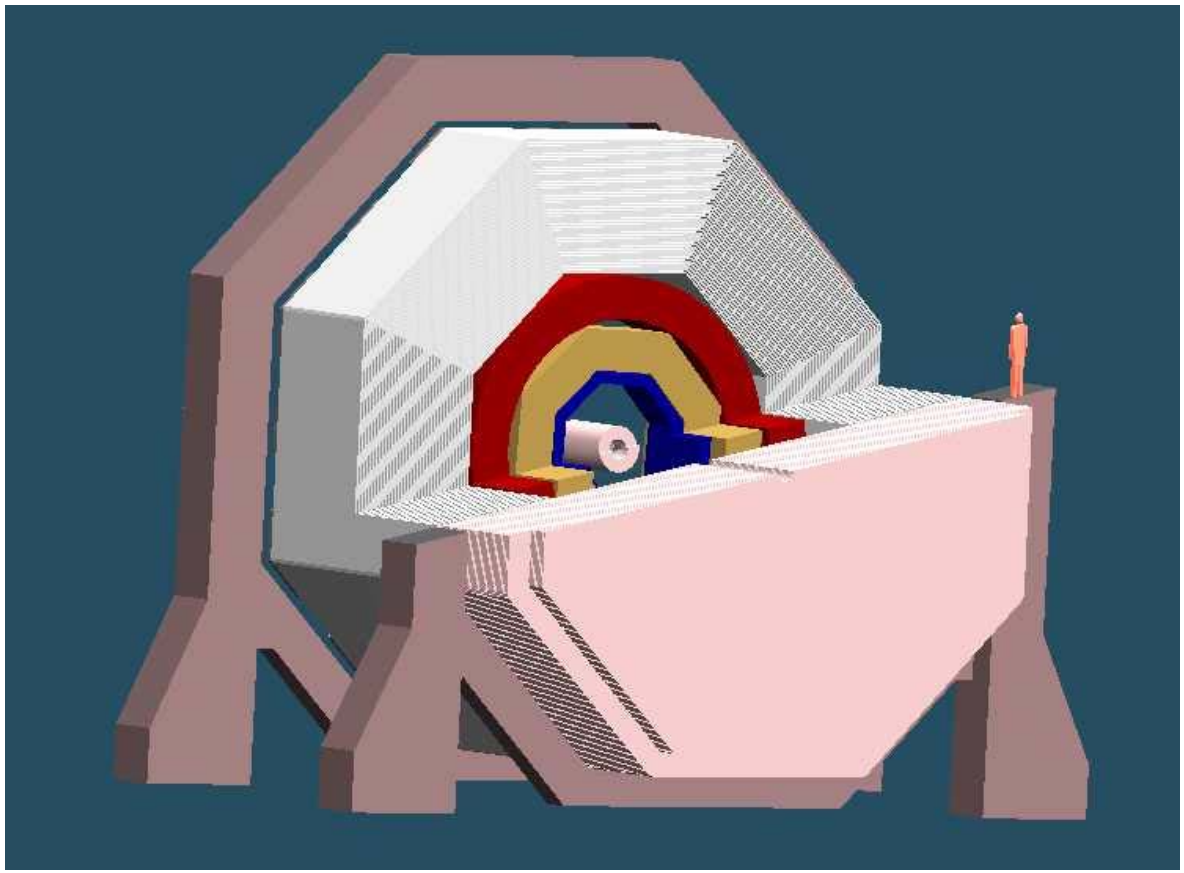
SD – Silicon Detector EM Calorimetry

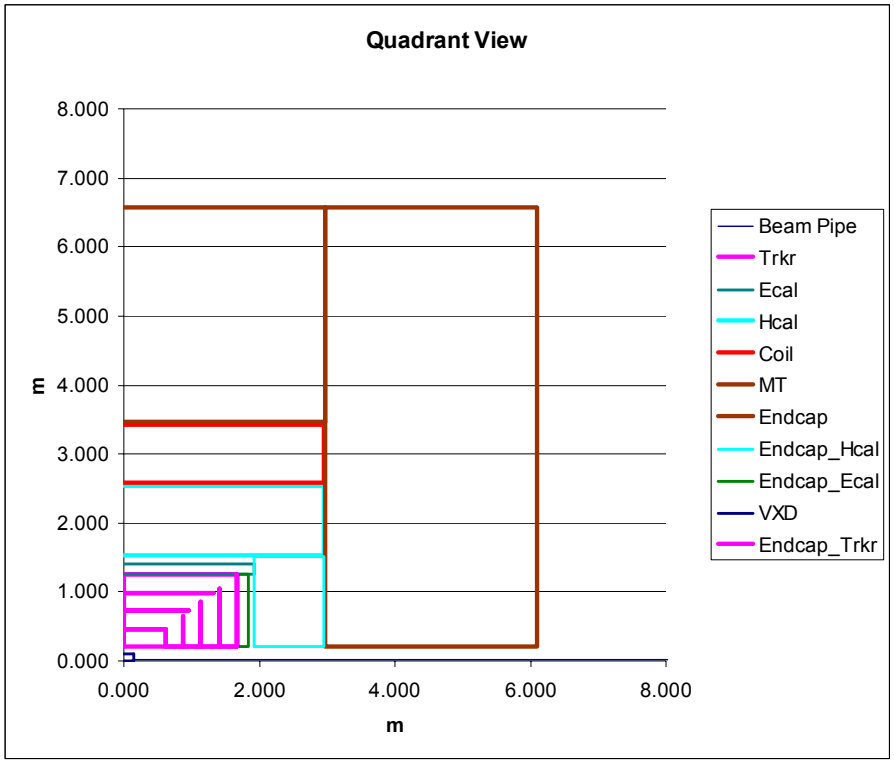


SD (Silicon Detector)

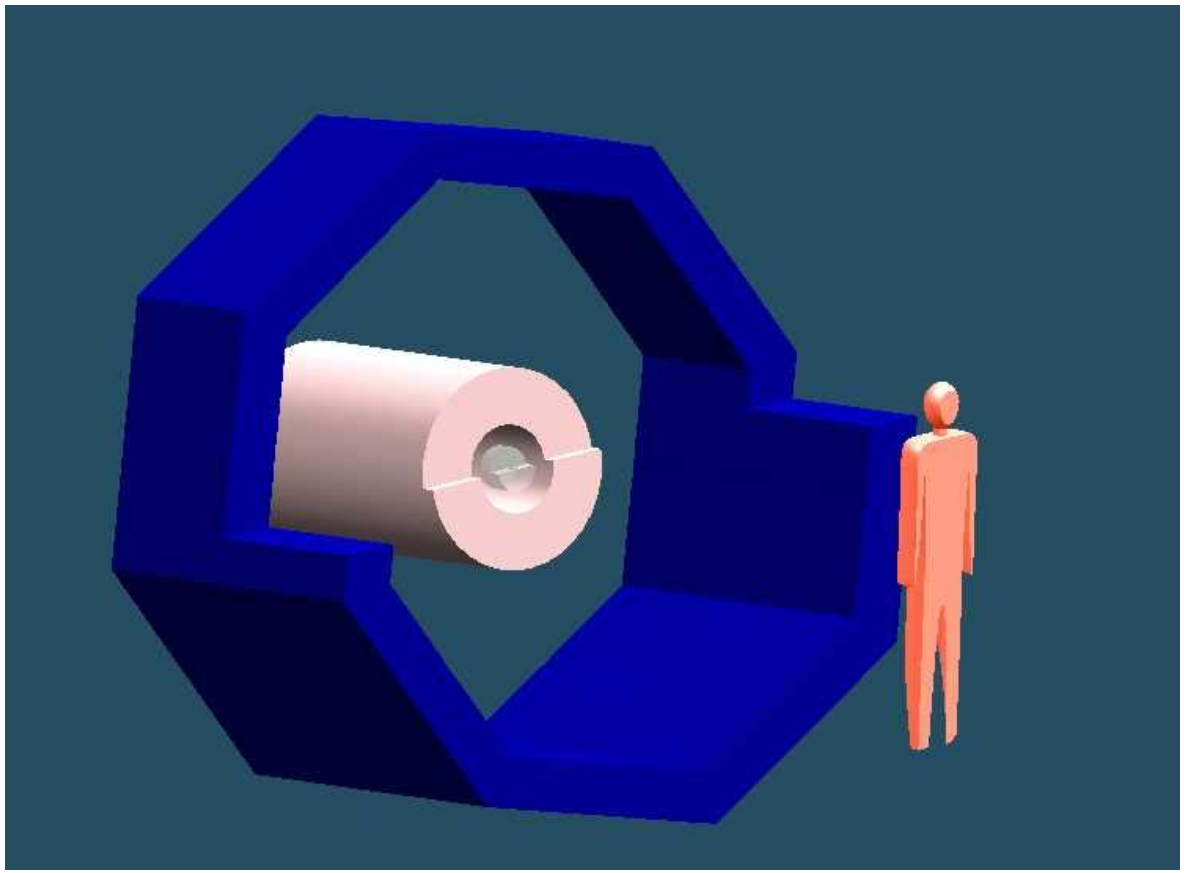
- Conceived as a high performance detector for NLC
- Reasonably uncompromised performance
- But
- Constrained & Rational cost

- We accept the notion that excellent energy flow calorimetry is required, and explore optimization of a Tungsten-Silicon EMCal…

Silicon Detector
EM Calorimetry



Scale of EMCal & Vertex Detector



Silicon Tungsten EMCal

- Figure of merit something like BR^2/σ, where σ is the rms sum of Moliere radius of the calorimeter and the pixel size.
  - Maintain the great Moliere radius of tungsten (9 mm) by minimizing the gaps between ~2.5 mm tungsten plates. Dilution is (1+Rgap/Rw)
  - Could a layer of silicon/support/readout etc fit in a 2.5 mm gap? Even less?? 1.5 mm goal??
- Requires *aggressive* electronic-mechanical integration!

EMCal, continued

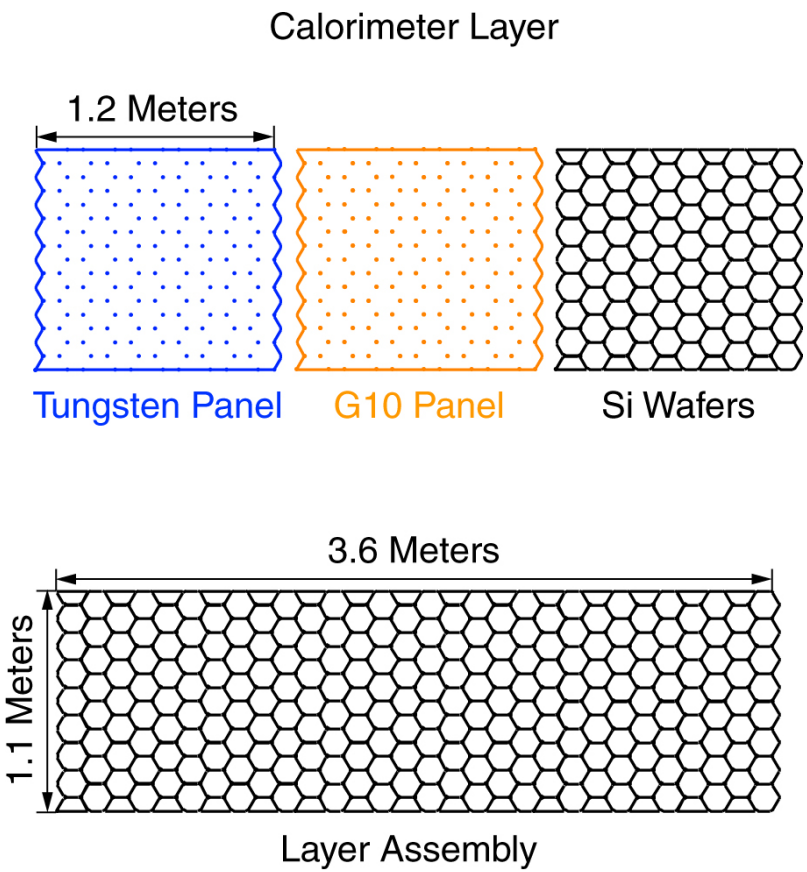
- Diode pixels between 5 – 10 mm square on largest hexagon fitting in largest available wafer. (6" available now – 300 mm when??) Consider μ tracking as well as E flow in picking pixel dimension.
- Develop readout electronics of preamplification through digitization, zero suppression and IO on bump bonded chip. Upgrade would be full integration of readout on detector wafer. (R&D opportunity!)
- Optimize shaping time for small diode capacitance. Probably too long for significant bunch localization within train. But some detector element needs good time resolution!!!

Channel Counts [Forget Them!!]

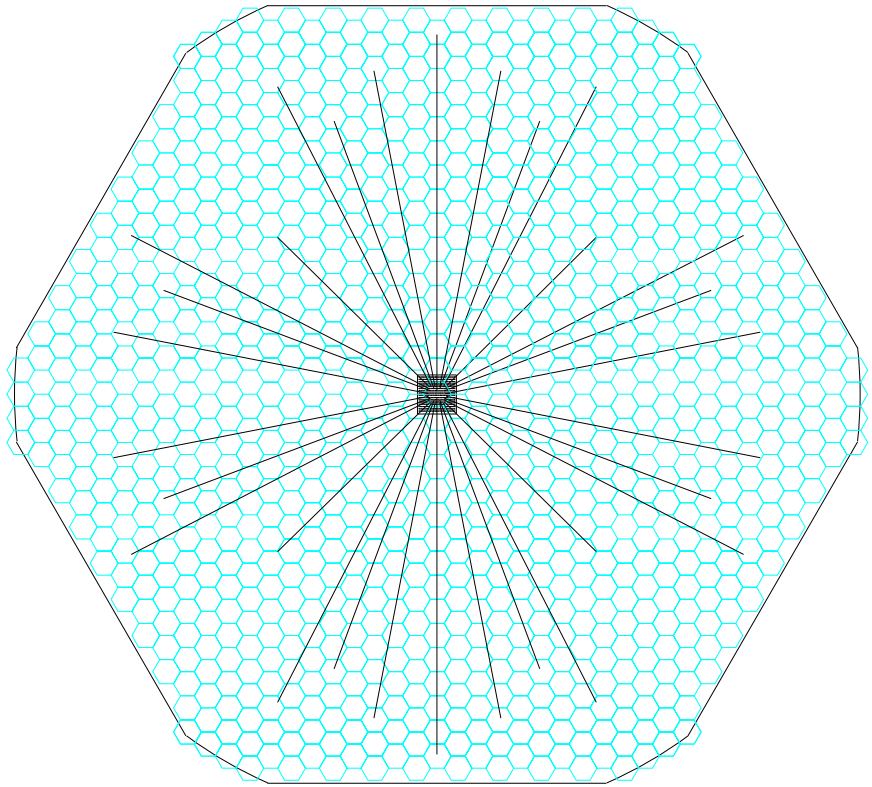
- We are used to pixel counts in CCD's …
  - 3×10^8 last time, 1×10^9 this time, no problem
- Silicon Strip Tracker ~5×10^6 strips (channels??)
- EMCal ~5×10^7 pixels (channels??)
- Don't even think about multiplying channels by O($10)……

- Must solve the cluster technology challenges.

Structure


Calorimeter Layer
1.2 Meters
Tungsten Panel
G10 Panel
Si Wafers
3.6 Meters
1.1 Meters
Layer Assembly

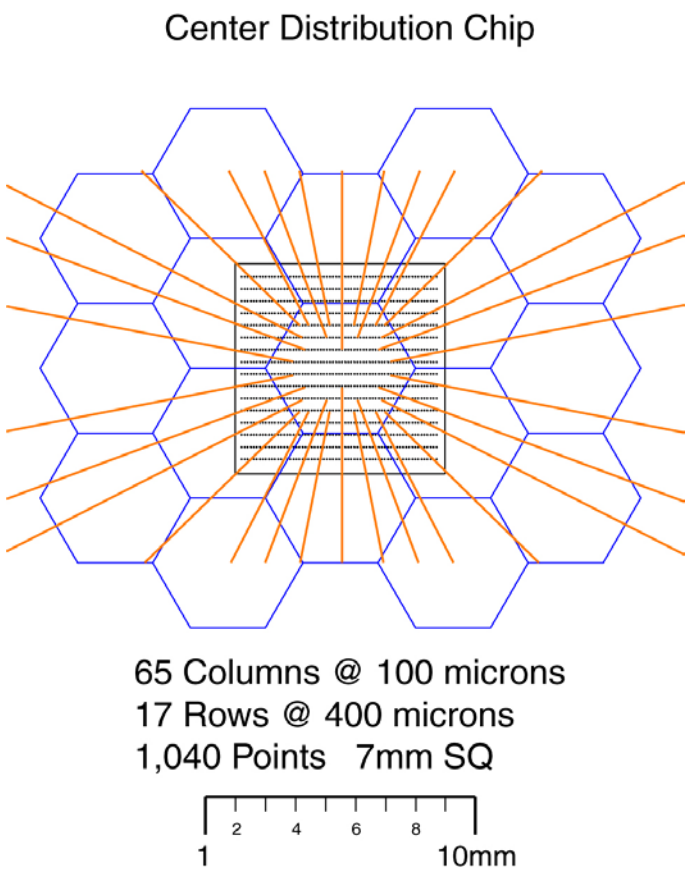
Pixels on 6" Wafer



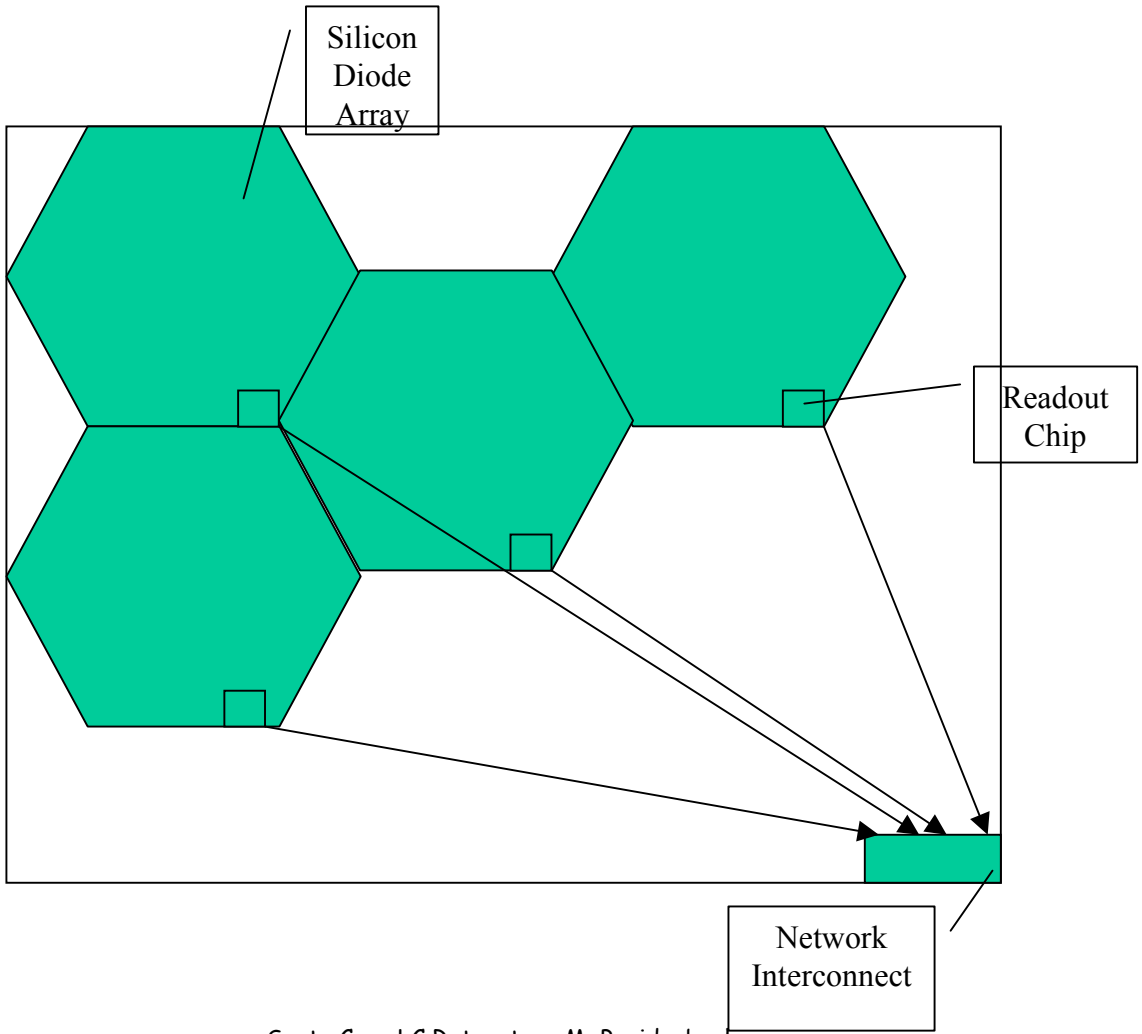
6 inch (152mm) WAFER

1,027 (5mm) CELLS

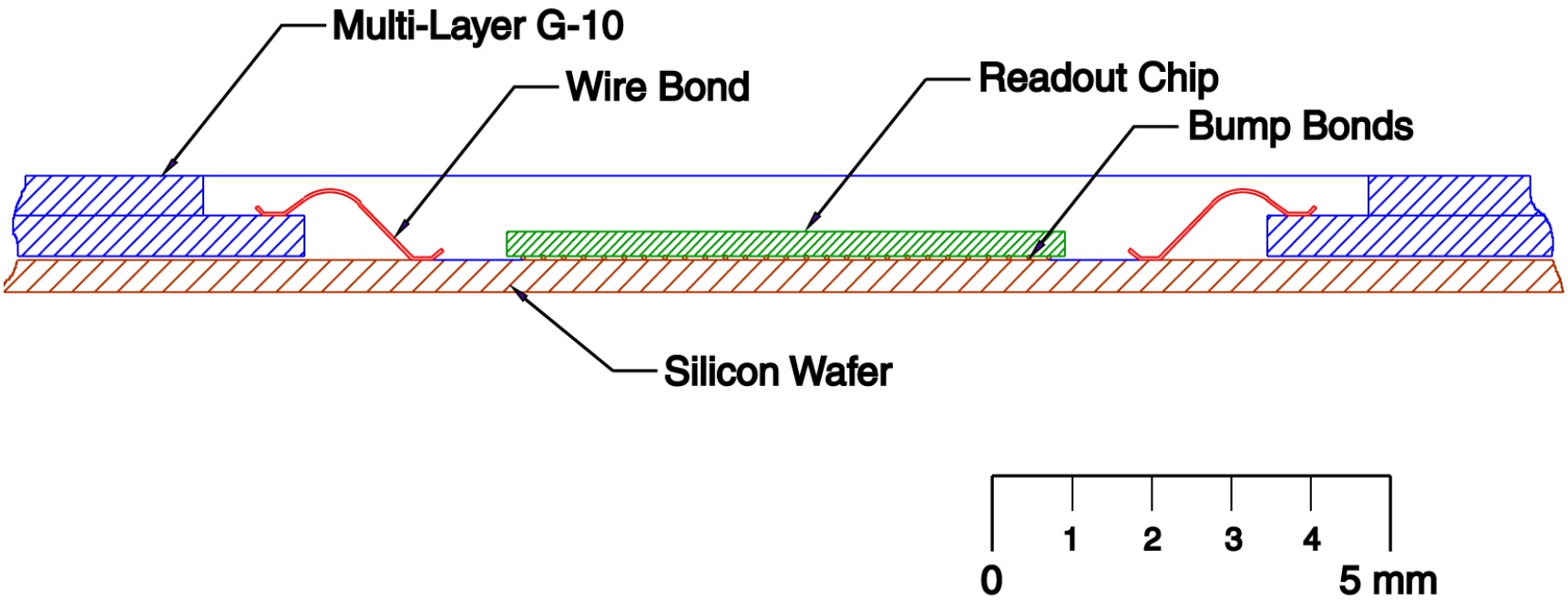
Zoom to Readout Chip



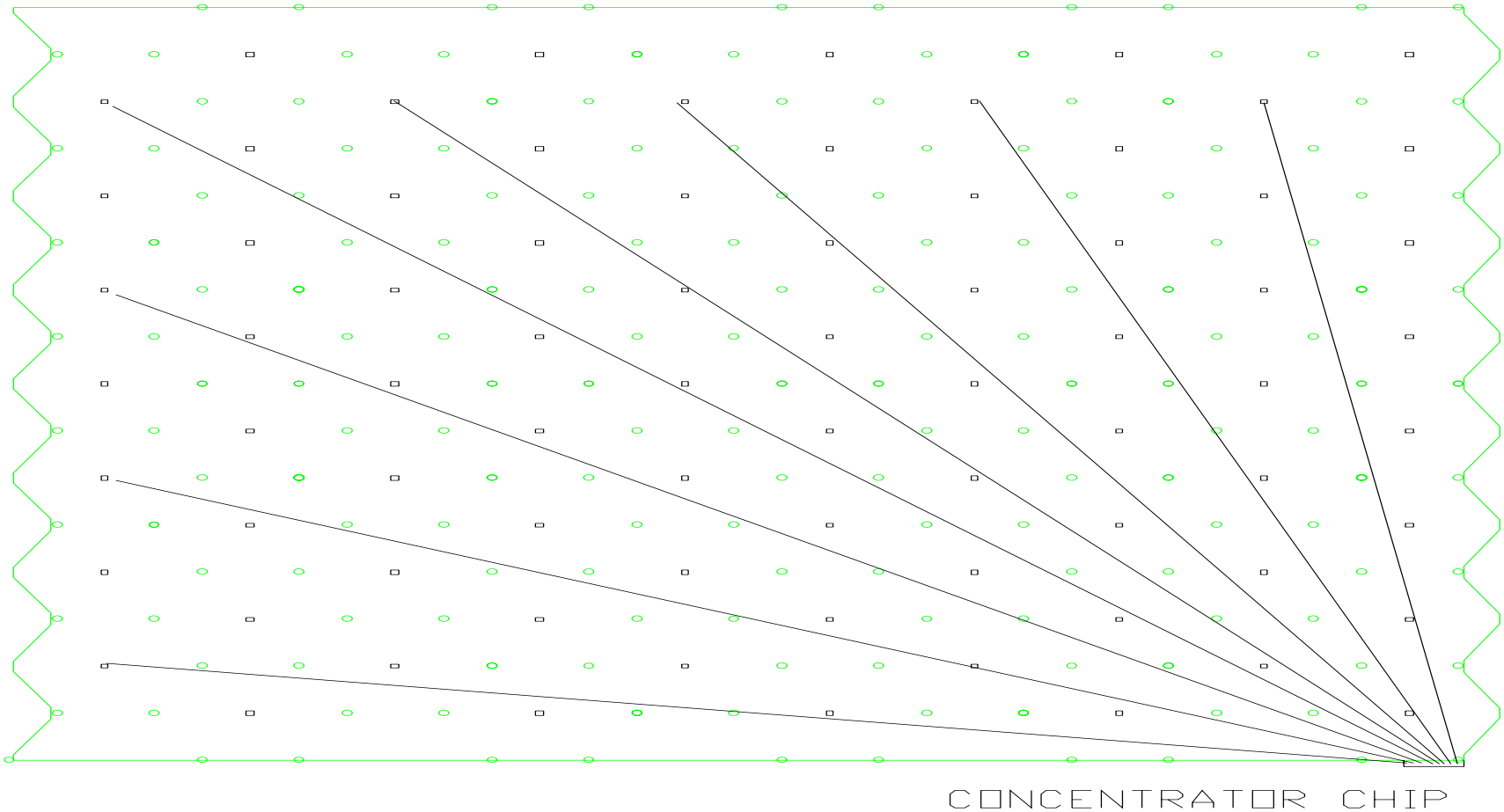
Gross System Architecture



Cross Section

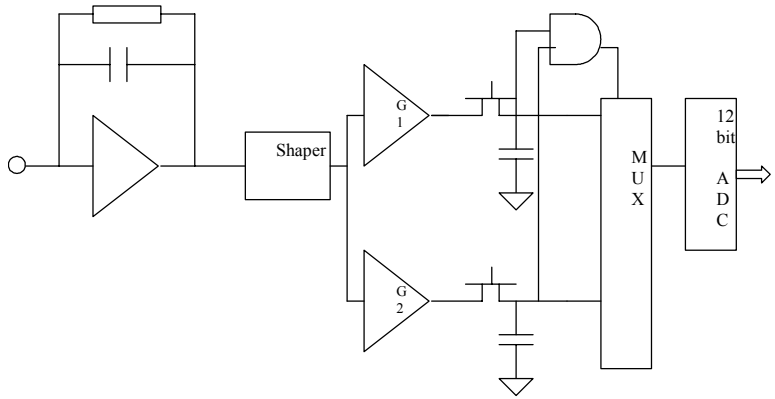


Signal Collection from m² board



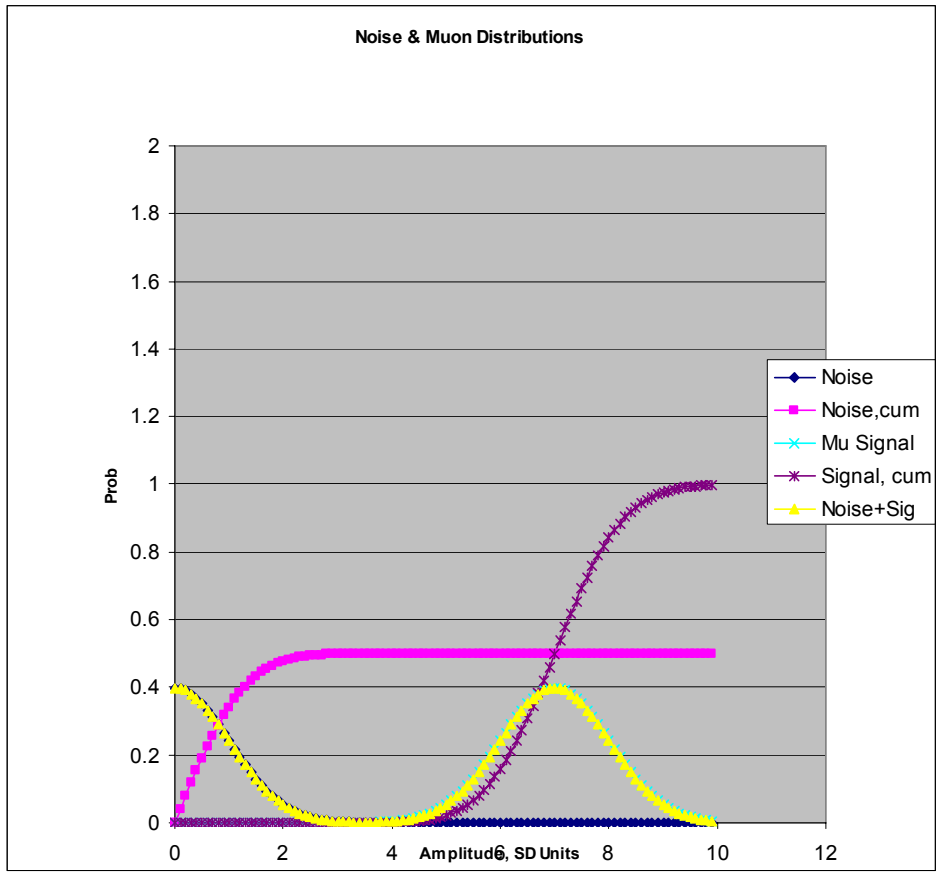
Preamplifier Architecture

- Charge amplifier and shaper followed by two amplifiers with gains G1,G2 and sample & holds.
- Comparator logic to select appropriate range
- Mux and 12 bit ADC



Noise and Muons

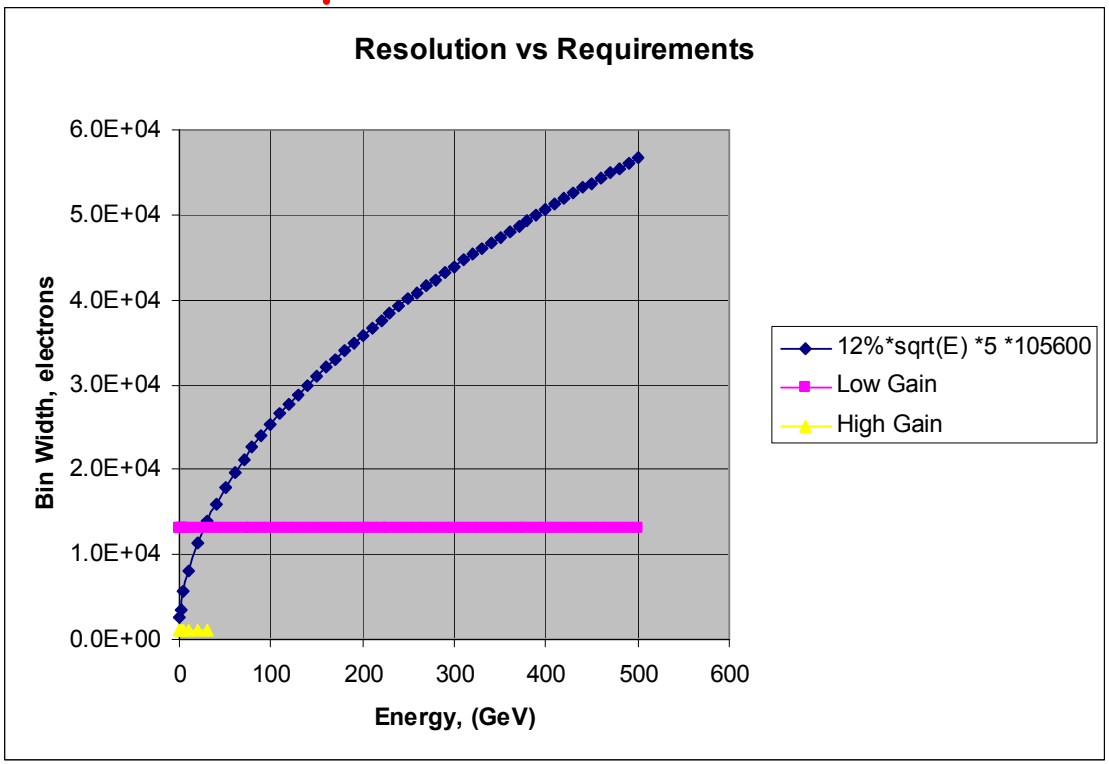
- Assume 300 μ (400-500 μ possible) effective e^- collection at 80 e^-/μ. signal ~ 24000 e^-.
- Assuming diode capacitance of 0.3 pf/mm^2, and amplifier noise of 20e^-/pf+200e^- – noise ~400 e^-. S/N ~60, plenty good!
- Pick S/N of 7 (Figure) for minimum performance.



Plausible Resolution Criteria

- Spread the 0.6% muon σ into several bins, with enough range for MIP counting to a few.
- Preliminary Monte Carlo indicates peak ionizing track density from a high energy shower to be 2200 μ equivalent. (5×10^7 e^- = 8 pC.)
- Do not degrade resolution of calorimeter! Energy resolution of a sampling calorimeter with 2/3 X_0 plates will not exceed $12\%/\sqrt{E}$. Say this peak should be spread over 5 bins, and take no credit for multiple sampling.
- Relaxation of these requirements now being studied with EGS.

Required Resolution



- High Res Bin Width=1000 e^-, Emax=37 GeV,Mips=170
- Low Res Bin Width=13200 e^-,Emax=512 GeV,Mips=2325

Technical Issues

- Assuming integrator full scale voltage of around 1 V, feedback (and calibration) capacitors need to be ~10 pF. This is large for an integrated capacitor, but doable with substantial real estate.
- Plus is that this makes the bump bond pitch easy!

Thermal Management

- Cooling is a fundamental problem: GLAST system is ~2 mW/channel. Assume 1000 pixels/wafer and power pulsing duty factor for NLC of 10^{-3} (10 μsec @120 Hz), for 2 mW average power.
- Assume fixed temperature heat sink (water cooling) at outer edge of an octant, and conduction through a thick (6 oz) copper ground plane in the G10 motherboard.
- $\Delta T \sim 1^0 C$.
- This is fine, but it sure doesn't work without power pulsing!!! Holding the power down while maintaining the noise/resolution is a serious engineering challenge.

Plans

- We (Oregon and SLAC) plan to develop this design in more detail and build prototype wafers and chips.
- Test detectors in 5 Tesla field.
- If successful, develop board level chip.
- Build 1 wafer wide by about 25 X_0 deep calorimeter for test beam.