Silicon/Tungsten ECal for the SD Detector

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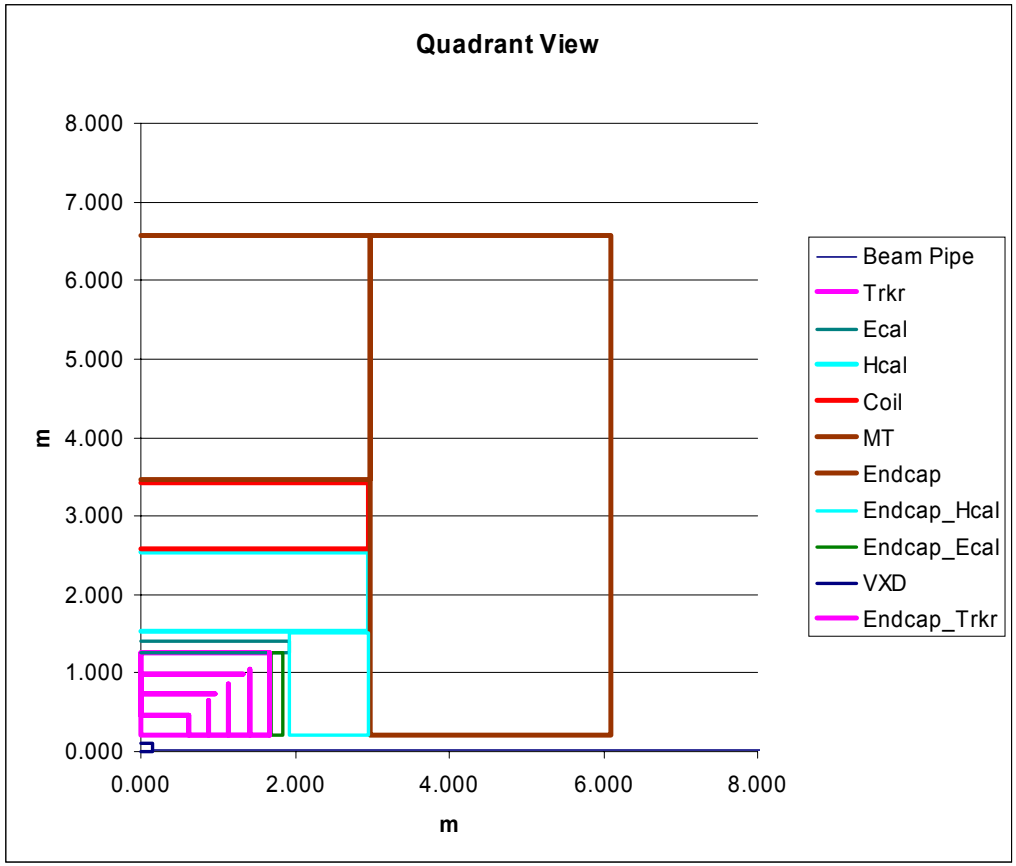
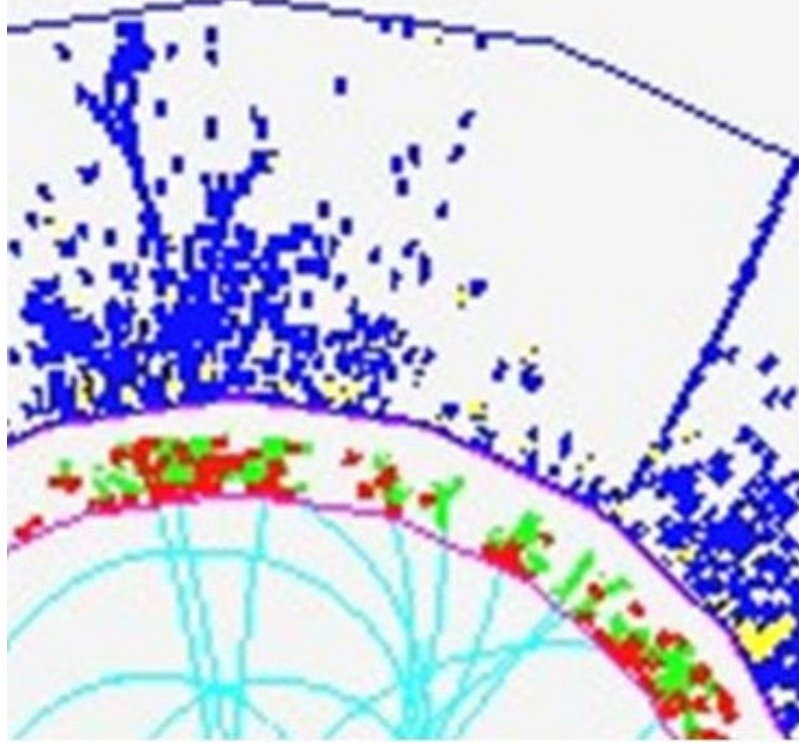


SD Detector

- SD designed for excellent energy flow performance – with well-understood and somewhat constrained costs (see Snowmass Orange Book for details)

- **Si/W ECal**
  - 5 T ; R_{in} = 1.27 m
  - 5mm transverse segmentation
  - [2.5 mm W (0.7 X_0), 0.3 mm Si] x30
    - *Not* optimized !
  - R_m = 9mm (1 + gap(mm)/2.5) → Keep gaps small !



In this talk:
- Detector/Frontend architecture and considerations
  - Current R&D
  - Still working on overall mechanical design
- Plans

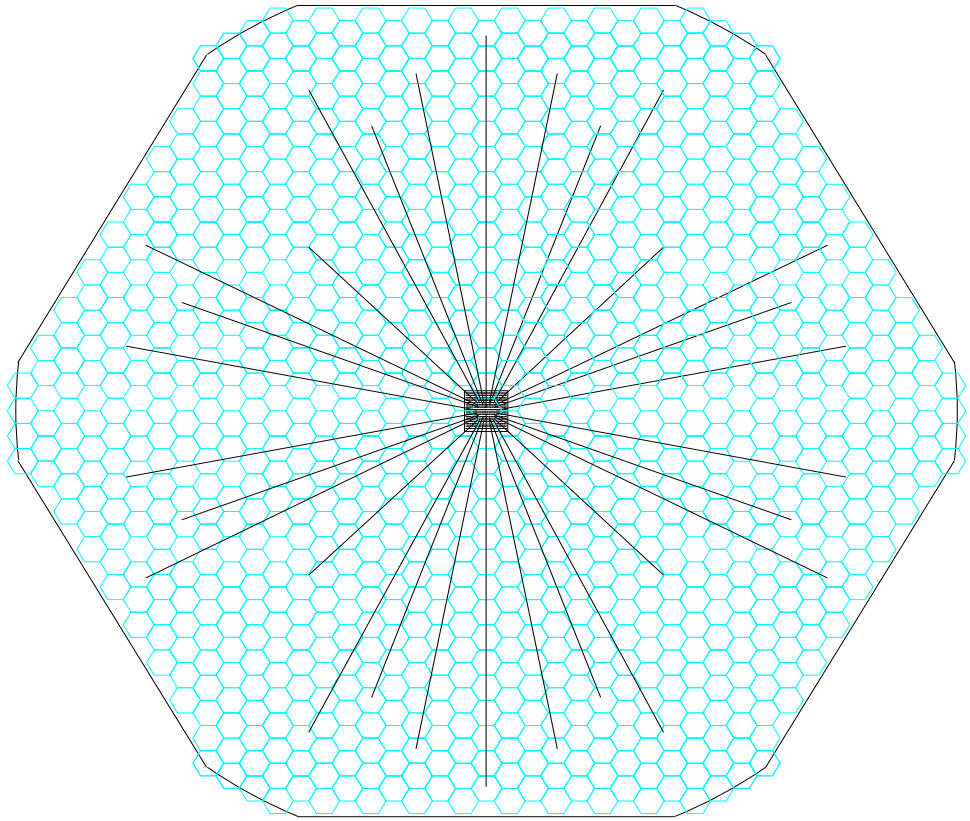
SD Si/W

- 5x5 mm^2 pixel ⇒ 50M pixels
- Do NOT scale electronics by this number
- *For each (6 inch) wafer:*
  - 1000 pixels (approx)
  - One readout chip (ROC)
- *Simple, scalable detector design:*
  - Minimum of fab. steps
  - Use largest available wafers

⇒ Detector cost below \$2/cm^2

⇒ Electronics cost even less

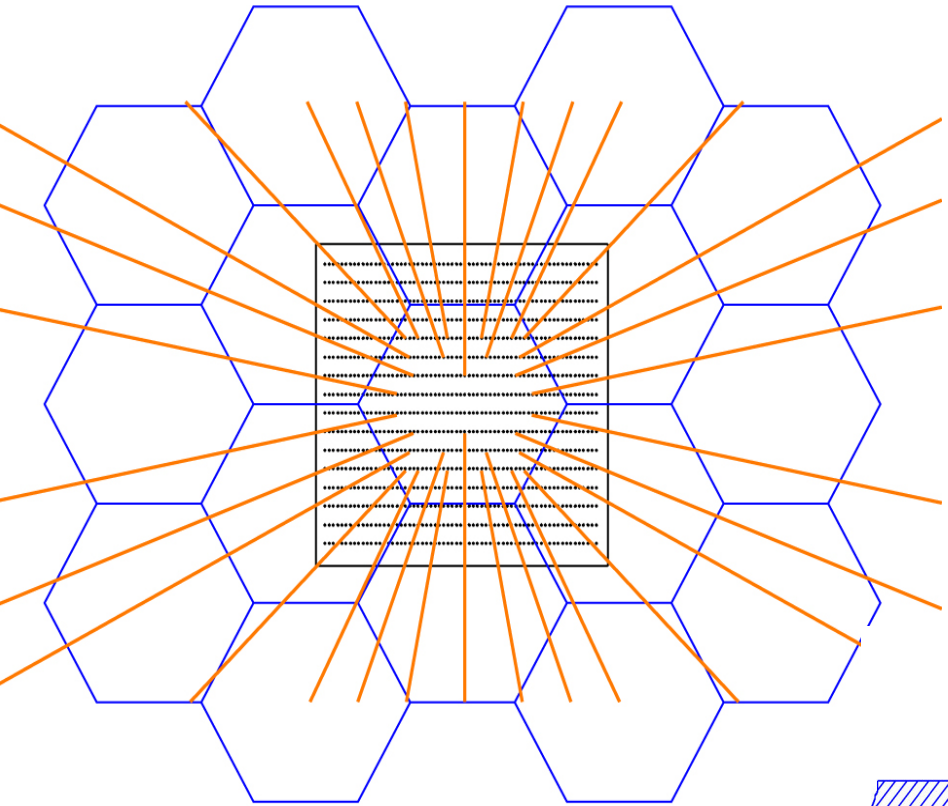
⇒ **A reasonable (cheap?) cost**



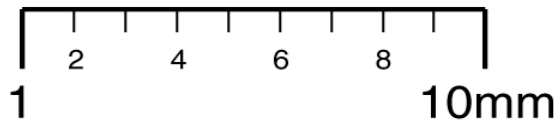
6 inch (152mm) WAFER

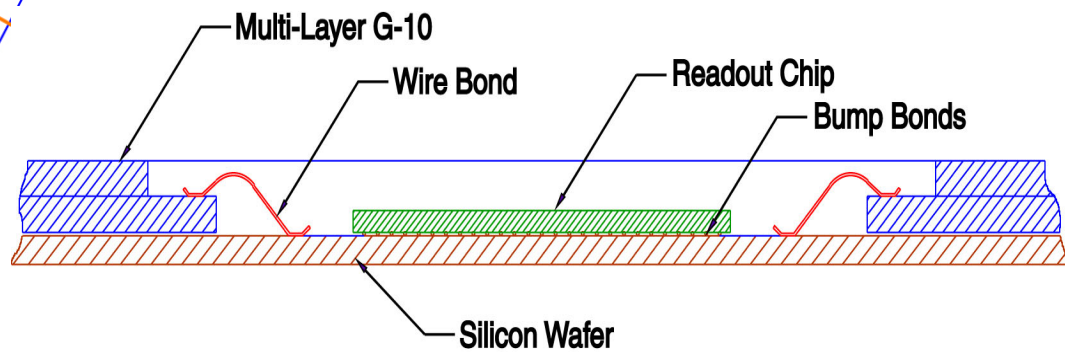
1,027 (5mm) CELLS

Wafer and readout chip



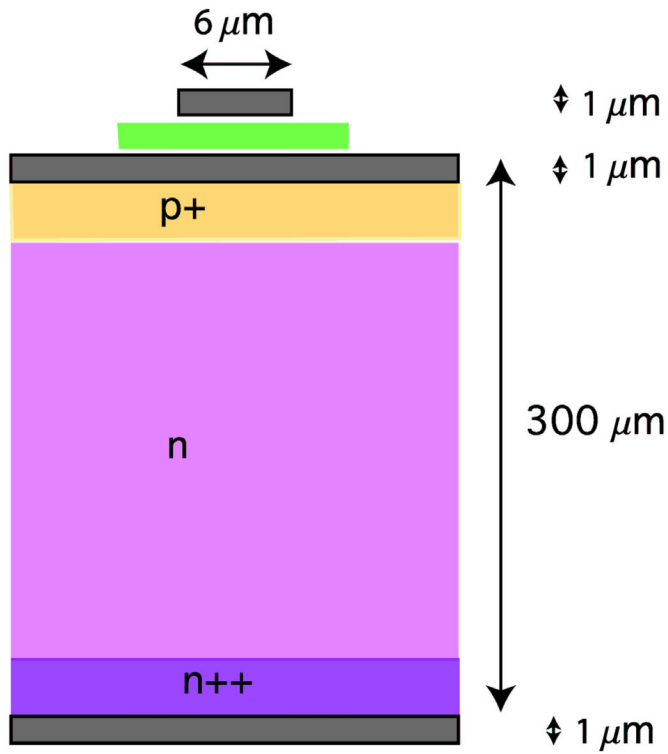
Use bump-bonding technique to mate ROC to array of pads on wafer





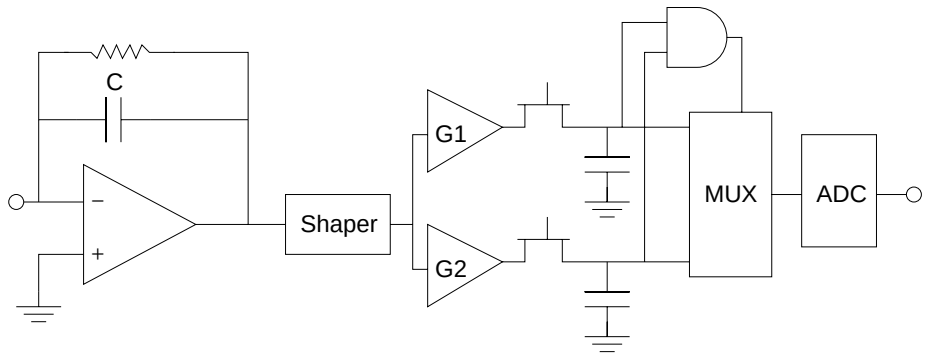
Silicon detector layout considerations

- DC coupled detectors are simple (cheap)
  - Use AMPLEX-type preamp design
  - OK as long as leakage currents small and *stay* small
  - Straightforward layout uses two metallization layers (OK)
    - Possible to try one for R&D ?
  - Get (fast) trigger signal from common back side
  - Pixel-readout trace crosstalk ≈ 1%
- AC coupled also possible
  - Avoid inputting leakage current to preamp
  - More complicated
    - Complete additional network (hard)
    - Additional layer and vias
    - Cap. breakdown
    - Beware hierarchy of capacitances



Readout channel

- Dynamic range: MIPs to Bhabhas
  - About factor 2000 range per pixel
  - Want to maintain resolution at both ends of scale
  - Demand S/N of 7 for MIPs
  - Satisfy with 2 overlapped ranges
    - G1/G2 ≈ 15
    - 12 bit ADC
  - Need C ≈ 10 pF (big)
    - Approx. same as pixel cap.



- Additional 10 pF cap. for calib.
- Shaping time about 100-200 ns
- One additional channel per chip for fast common trigger signal
- Expect noise of 300 e rms (GLAST)

Detailed design in progress

Radiation

- EM radiation dominated by Bhabhas (in forward endcap)
  - $d\sigma/d\theta \approx 10\ pb/\theta^3$ for t-channel
  - Consider 1 ab^{-1}, 500 GeV, shower max., and θ=60 mrad (worst case)
    - Use measured damage constant (Lauber, et al., NIM A 396)

    $\Rightarrow$ ≈6 nA increase in leakage current per pixel
  - Comparable to initial leakage current
  - Completely negligible except at forward edge of endcap

- Currently evaluating potential neutron damage

- A 300 GeV electron shower into a readout chip?
  - "Linear Energy Threshold" (LET) is 70 $MeV/cm^2/mg$

  $\Rightarrow$ Expect no such problems

Heat

- Does integrated design imply fancy cooling system?
- Consider: NLC duty cycle is 5×10^{-5} (5×10^{-3} for TESLA)
  - 270 ns bunch trains at 150 Hz

$\Rightarrow$ Use power pulsing of the electronics

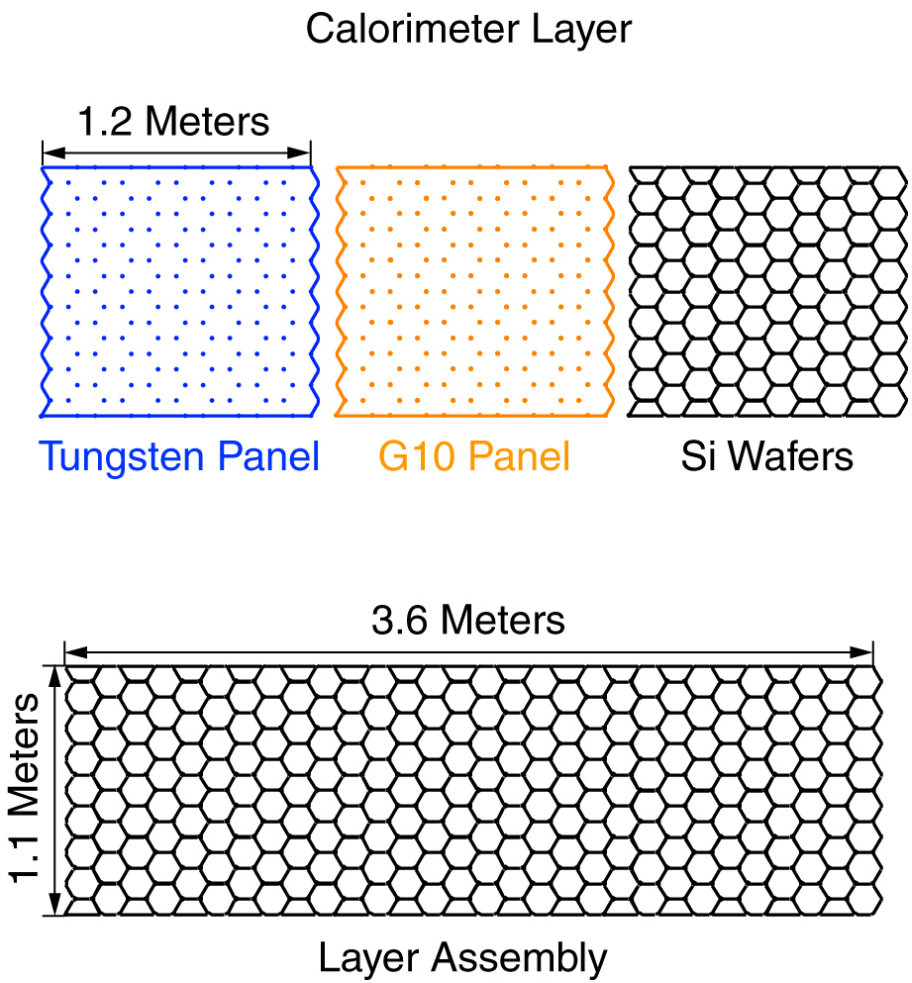
- For example, GLAST-equivalent readout would produce only about 1 mW average power per 1000-channel chip
  - Assumes power duty cycle of 10^{-3}

    … this factor is an important R&D item

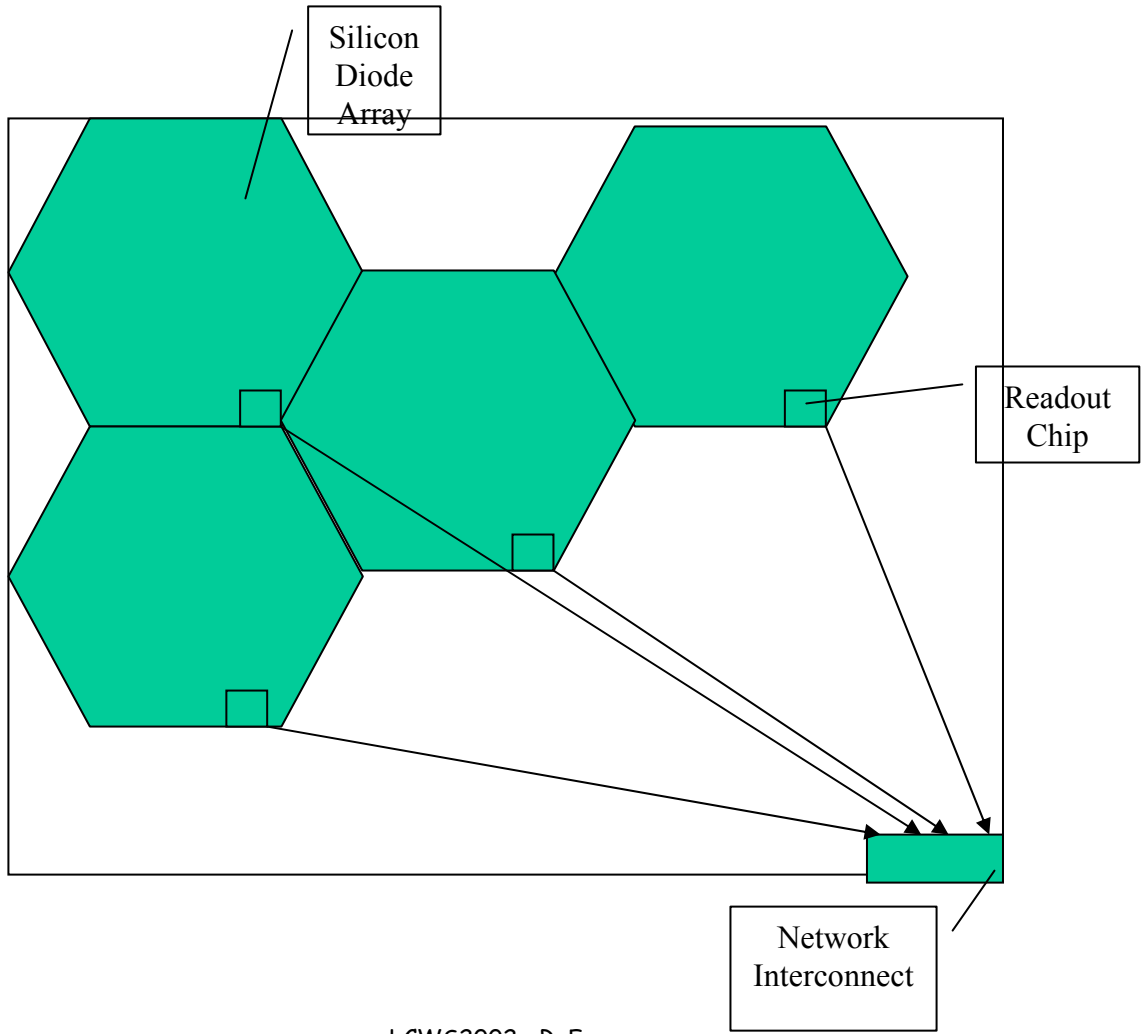
- Current proposed scheme:
  - Heat conduction thru thick (6 oz) Cu layer in G10 m-board to fixed temperature heat sinks at edges of ECal modules

  $\Rightarrow \Delta T \approx 1^{\circ}C$
- Requires R&D to demonstrate

Putting together a layer



Gross System Architecture



Plans

- Procure full-wafer (6” for now) detectors with complete layout
  - QC, verify crosstalk, SNR, etc.
  - Test in 5 T
- Simulations: optimize segmentation and longitudinal sampling
- Design and produce first readout chip
- Bump bonding trials
- Design and build full 1-wafer wide module
  - Power pulsing and thermal management
- Test beam
  - Electrons/photons and hadrons (together?)
  - Check vs simulations
- Mechanical structure
- Cost optimizations
  - Silicon
  - Readout
  - Tungsten

Summary

- A highly granular Si/W ECal would be very nice at the LC !
  - Expect excellent EFlow jet reconstruction
  - Photon reconstruction (non-pointing; flavor id. of jets)
  - “Imaging calorimeter” for MIPs, photons, had. showers
- An integrated design makes this feasible
  - If not cheap, at least not crazy
- Requires answers to key R&D issues over next ≈ 2 years
  - Silicon configuration
  - Readout chip
  - Cooling and mechanics
  - Test beam