Project name

Development of a silicon-tungsten test module for an electromagnetic calorimeter

Classification (accelerator/detector:subsystem)

Detector:calorimetry

Institution(s) and personnel

University of Oregon, Department of Physics and Oregon Center for HEP: <u>Raymond Frey</u> (professor), David Strom (professor)

Stanford Linear Accelerator Center: <u>M. Breidenbach</u> (faculty), D. Freytag, N. Graf, G. Haller, J. Jaros (faculty), M. Huffer, J.J. Russell

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Project Overview

The TESLA and SD detector designs call for a silicon-tungsten electromagnetic calorimeter (ECal) as the best option for providing the necessary segmentation to implement the energy flow method for jet reconstruction at the LC, capable of achieving jet energy resolution of $\approx 0.3/\sqrt{E}$ jet, as recommended by LC physics studies. The number of detector pixels for these ECal designs is on order 50 million. One of the outstanding technical questions is how to integrate a silicon detector wafer with its readout electronics. Along with the cost of the silicon detectors themselves, a solution to the integration issue is likely to determine the overall viability of the silicon-tungsten approach. We have, in fact, proposed^{1,2} a possible solution to the integration problem. We propose to implement this idea in stages, starting with component feasibility assessments (year 1) and engineering prototypes (year 2). If successful, we plan to develop a full ECal module (year 3) for testing in a beam.

Briefly, we hope to integrate detector pixels on a large, commercially feasible silicon wafer. For example, a 6 inch wafer would include on order 1000 pixels for pixel size 5x5 mm². One readout chip for each wafer would be bump bonded to the wafer. The chip would include the analog and digitization elements for the 1000 pixels. In this way, the channel count is effectively reduced by a factor 1000. We take advantage of the low beam duty cycle (5×10^{-5} for NLC) to reduce the heat load using power cycling. Initially, we break up the project into two areas of responsibility:

- 1. Silicon detector design, procurement, and characterization (Oregon)
- 2. Readout chip design, procurement, and testing (SLAC)

The description above is the main thrust of this proposal. However, several of us (Frey and Strom at Oregon, Graf and Jaros at SLAC) also plan to be involved in closely related simulation and software activities, for which we are not requesting funding:

- Technical simulations. Use EGS4 and Geant4 to study dynamic range, longitudinal sampling optimization, segmentation, etc. Graf is developing a general package for test beam configuration simulation to be used by other groups as well as ours. Use SPICE to study issues like crosstalk from pixels to metallization traces on the wafers.
- Detector modeling simulations. Continue to use the LCD software packages to optimize detector configurations as a function, for example, of photon and tau reconstruction performance, pion rejection, etc, as well as performance for benchmark physics processes. The LCD Geant4 packages are to be used for this.
- Algorithm development. The Energy Flow (EF) concept is to be used for jet reconstruction. In large part this is what underlies the detector concept. There are many different ideas for how to implement EF algorithmically. We plan to continue these studies. We are included in a separate proposal, submitted by NIU/NICADD, for this element of research, although no funding is requested by us at this time.
- Physics simulations. Help to develop multi-jet and other benchmark processes to be used for Energy Flow evaluation. Study the contributions to jet resolution from the detector, QCD, 2-photon backgrounds, etc. Studies to date indicate that, unlike for the LHC, the resolution is limited by the detector, not QCD and backgrounds. We would like to explore this further.

Some details on the silicon detector research

Several experts on silicon detector fabrication are projecting that the cost for simple silicon detectors, like those considered here, will be in the range 1 to 2%/cm² when detectors are purchased on a large scale. The current SD design calls for 13×10^6 cm² of silicon. With silicon being the largest cost component, it seems that a reasonable total cost for the silicon-tungsten ECal is achievable. However, to keep the silicon cost at this level requires that the silicon layout be as simple as possible. Therefore, we seek to use DC-coupled detectors if possible. High resistivity silicon (~10 k Ω -cm) should initially have low leakage currents at full depletion (\approx 1 nA or less per pixel), and our initial studies of potential radiation damage indicate that this current will not increase substantially. This allows DC-coupled detectors to be used with standard readout electronics with a front-end similar to the AMPLEX chip used by the silicon-tungsten luminosity calorimeters at LEP.

Since Energy Flow performance is best when individual particles can be separated in the calorimeter, a small Moliere radius in the ECal is highly desirable. Tungsten, with $R_m=9$ mm, provides this. However, the *effective* Moliere radius includes the sampling layers. For example, for tungsten layers of thickness 2.5 mm (as for SD), the effective Moliere

radius becomes (9 mm)(1 + z/2.5), where z is the thickness of the sampling layer (*i.e.* everything not tungsten) in mm. So, one of our design goals is to keep z small.

Thermal issues are important for most calorimeters, especially as in our case with embedded electronics. Since we aim to put all electronics for each $\sim 10^3$ pixels on a single readout chip (ROC) within the detector, this is a concern. Here, we use one of the nice features of LC design — the bunch structure. For NLC the bunch-train duty cycle is just 5×10^{-5} . So one might hope to use power pulsing to keep the electronics off for most of the dead time. If one assumes a power duty cycle of 10^{-3} , then the average power consumption of the ROC will be small (~ 1 mW) and hopefully manageable with simple techniques. Clearly, it is important to demonstrate this.

Current status

We are presently working with potential vendors of the silicon detectors on detector design, layouts, etc. We (Oregon) expect to buy prototype detectors as soon as funds become available. Meanwhile, the SLAC group is working on the readout chip design. We have begun weekly SLAC-Oregon phone meetings. We have discussed our design ideas at regional and international meetings, and it seems that other groups, including those primarily studying TESLA, will be interested in the results of this work.

Description of first year project activities

Design and procure first round of detector prototypes. We do not yet know the prototype costs, but based on past experience we hope to purchase about 5 detector wafers with the indicated budget line. These are to be full 6 inch wafers with pixels, traces, bump bond pads, biasing, etc. These are to be received at Oregon and will undergo initial testing, including basic QA and crosstalk measurements (using an IR laser system). The tests will include leakage current, capacitance, and depletion voltage measurements. In parallel, SLAC will develop the first readout chip. No funds are requested for this part. The goal is to have wafers and readout chip ready to be bonded together for testing by end of year one. Year one is to include a silicon detector test in a 5 T magnetic field. We now also include 2.5 k\$ for travel to cover 1) the Oregon part of the simulation effort, and 2) the planned meetings with European colleagues to discuss our silicon-tungsten work. We expect to include meetings at SLAC as part of our ordinary SLAC travel for BaBar, so do not request funding for this.

Deliverables include the prototype detectors and first bench test results, a first readout chip design, and delivery of the first chips.

Budget

_	Year 1	
Institution	Item	Cost
Oregon	Custom silicon detector prototypes (about 5)	\$25,000
Oregon	Probe and test equipment for detectors	\$10,000
Oregon	Travel	\$ 2,500
Oregon	Oregon total	\$37,500
SLAC	SLAC total	\$0

Notes: Indirect costs for the travel are included in the 2.5 k\$. We have a clean room at Oregon for the detector work, and a probe station, but not all of the required test equipment.

Description of second year project activities (guesstimates)

Note: Year 2 and 3 activities are necessarily vague at this point. Test the first round of prototypes using various particle sources on the bench. Most likely will need a second round of detector (and readout chip) prototypes. Perform the next level of system measurements for the final design, such as heat dissipation, leakage current changes with radiation, signal size, crosstalk, noise, etc. Start to design a mechanical system for a full test beam experiment. Collaborate with others on the beam test, hopefully including a hadron calorimeter prototype.

Institution	Item	Cost
Oregon	Custom silicon detector prototypes – round 2	\$25,000
Oregon	Data acquisition equipment	\$10,000
Oregon	Test equipment	\$ 5,000
Oregon	Travel	\$ 5,000
Oregon	Oregon total	\$45,000
SLAC	SLAC total	\$0

Year 2

Description of third year project activities (guesstimates)

Procure a "final" set of detectors. At this point, the cost/detector will be reduced, based on past experience. Goal is to build a full-depth ECal module of 30 layers (wafers), one wafer wide. The tungsten radiator plates to be procured and fabricated by method to be determined. Test beam to include both EM particles and hadrons. Other detector modules hopefully to be included (i.e. HCal, tracker) if possible, to be determined.

Year	3
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Institution	Item	Cost
Oregon	Custom silicon detector prototypes (25-30)	\$40,000
Oregon	Tungsten, material and machining	\$40,000
Oregon	Oregon total	\$80,000
SLAC	SLAC total	\$0

References

- 1. M. Breidenbach, talk at Chicago LC Workshop, Jan. 2002.
- 2. R. Frey, talk and conference paper presented at Calorimeter 2002, Pasadena, CA, March 2002; talk presented at Linear Collider Workshop, LCWS2002, Korea, August 28, 2002.

(Talks available at <u>http://zebu.uoregon.edu/LC/SiW/</u> and at the web site of the American Linear Collider Calorimeter Group: <u>http://www.slac.stanford.edu/xorg/lcd/calorimeter/</u>)

Relevant experience of proponents

The SLAC group has vast experience in design of e^+e^- detectors, including design and implementation of the readout electronics for most major detector systems for the SLD detector and several BaBar sub-systems. Of specific relevance, recently members of the group led the design of the electronics for the silicon strip detectors for the GLAST experiment. Graf is co-leader of the American Linear Collider Physics Group (ALCPG) simulations group and is the leader of the SLAC group which is developing the LCD simulation software.

Strom and Frey have each worked on silicon-tungsten luminosity calorimeters for OPAL (Strom) and SLD (Frey). Strom in particular was a key person in the OPAL silicon-tungsten development. Frey is co-leader of the ALCPG calorimeter group. Frey and Iwasaki (former postdoc, now at U. Tokyo) have done extensive calorimeter simulation work, which has been reported at many LC meetings.