Silicon detector layout and properties for linear collider calorimeters with MIP sensitivity

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1 Detector layout and properties

The detector layout is based on hexagonal pads which efficiently use the space on the round silicon wafers. A possible layout for six inch wafers is shown in figure 1. A possible cross section for DC coupled sensors is shown in figure 2.

1.1 Pixel capacitance

The pad capacitance is set by the thickness of the silicon wafer (300 μm) and the longest dimension of the pads (5mm) giving an area of 0.1624 cm^2. Taking the dielectric constant of Si into account ($\kappa = 11.8$), the capacitance for a fully depleted pixel should be approximately 5.7pF. Stray capacitances due to the traces used to connect the pads to the readout chips are discussed below.

1.2 Detector Leakage Current

Typical initial values of leakage current for past detectors are given in table 1.

In the case of OPAL and SLD the specification for leakage current given to Hamamatsu was much looser than the typical values. In order to get a good price, we ought to allow for $\sim$1% of the detectors to have leakage currents much larger than typical. In the past the depletion voltages for most detectors based on 4 in wafers have been below 80 V. It may be difficult for detector manufactures to obtain high resistivity 6 in (or larger) wafers with such low depletion values. If necessary, we could tolerate depletion voltages 2 or 3 times larger.

Leakage current due to radiation damage is discussed below.

1.3 Trace capacitance and cross talk.

The readout will be located at the center of each wafer and the signals will be transported from the pads to the readout on Al traces. These traces will be

isolated from the pads with a layer of SiO_2 ($\kappa = 3.98$) or a similar dielectric.

Previous uses of double metal Si strip detectors are summarized in table 2. As a baseline, we assume a trace width of 6 μm and an oxide thickness between metal layers of 1 μm.

This gives a coupling capacitance between the trace and a given pixel it crosses of 0.8 pF. The total capacitance for the longest trace is approximately 15pF and larger than the pixel capacitance itself. There will be additional coupling for the pads directly below the bounding area.

For 6 μm (wide) x 1.0 μ (thick) traces, the resistance for the longest traces ($\sim$70mm) will be approximately 300 Ω.

We have investigated the expected cross talk due to the capacitive coupling between the traces and the hexagon pads using Spice. Our simple model assumes an amplifier with an input FET with a transconductance in the range 0.1 to 5.0 mS and a feedback capacitor in the input stage of 10 pF. The charge amplifier is followed by an integration stage with time constant $\tau \simeq 200ns$ which is much longer than time needed to collect the charge from the silicon (approximately 40ns). In the absence of noise, the output signal will be of the form

$$1 - e^{-t/\tau}.$$

The output of the integration stage will be sampled at time $a\tau$ with a in the range 5-10, so almost the full charge will appear at the output.

In our baseline design the nominal thickness of the oxide between the traces and the pads is 1 μm. As a worst case we suppose that the oxide thickness is only 0.5 μm thick giving a coupling capacitance of $\sim$ 2pF. In figure 3 we give the cross talk (in %) as a function of transconductance and sampling time for $\tau = 200ns$. The cross talk predicted by Spice appears to be independent of most of the charge amplifier properties except for the transconductance of the input FET and the ratio of the sampling time to τ, a. Larger input transistor transconductances reduce the input impedance of the amplifier leading to reduced cross talk. These simulations should eventually be repeated with a more realistic model of the charge amplifier since bandwidth limiting elements inside the amplifier could lead to increased cross talk. However, given these results, it would appear that cross talk in other parts of the readout chain are likely to dominate in the final system.

Operating Voltage	Leakage current	Group	Si Manufacturer
80 V	2.5nA/cm^2	SLD	Hamamatsu
80 V	1nA /cm^2	OPAL	Hamamatsu
35 V	5nA/cm^2	ALEPH	Canberra

Table 1: Operating voltage and *typical* leakage currents.

Oxide	Oxide thickness	Trace width	Group	Si Manufacturer	References
SiO_2	3-5 μm	6-8 μm	CLEO III	Hamamatsu	[1],[2],[3],[4]
SiO_2	4-5 μm	6 μm	DELPHI	Hamamatsu	[5]
SiO_2	4μm	xxx	H1	CSEM	[6]
SiO_2	5 μm	8 μm	Belle	Hamamatsu	[7]
ONO	1.2 μm	12μm	Phobos	ERSO(Taiwan)	[8] , [9],[10]

Table 2: Oxide thickness, trace width for double metal detectors.

1.4 AC coupling

Using an amplifier with AC coupling would require a more complicated sensor design than that shown in figure 2. If a coupling capacitor is added between the first metal layer and p implant with an SiO_2 layer of 1 μm, it would have value $\sim$ 575 pF. This capacitance is sufficiently large compared to the pixel capacitance to cause a negligible loss of signal. If it were reduced to 100pF (for example by reducing the metalization on the pixel) it would start to reduce the total charge collected by the amplifier.

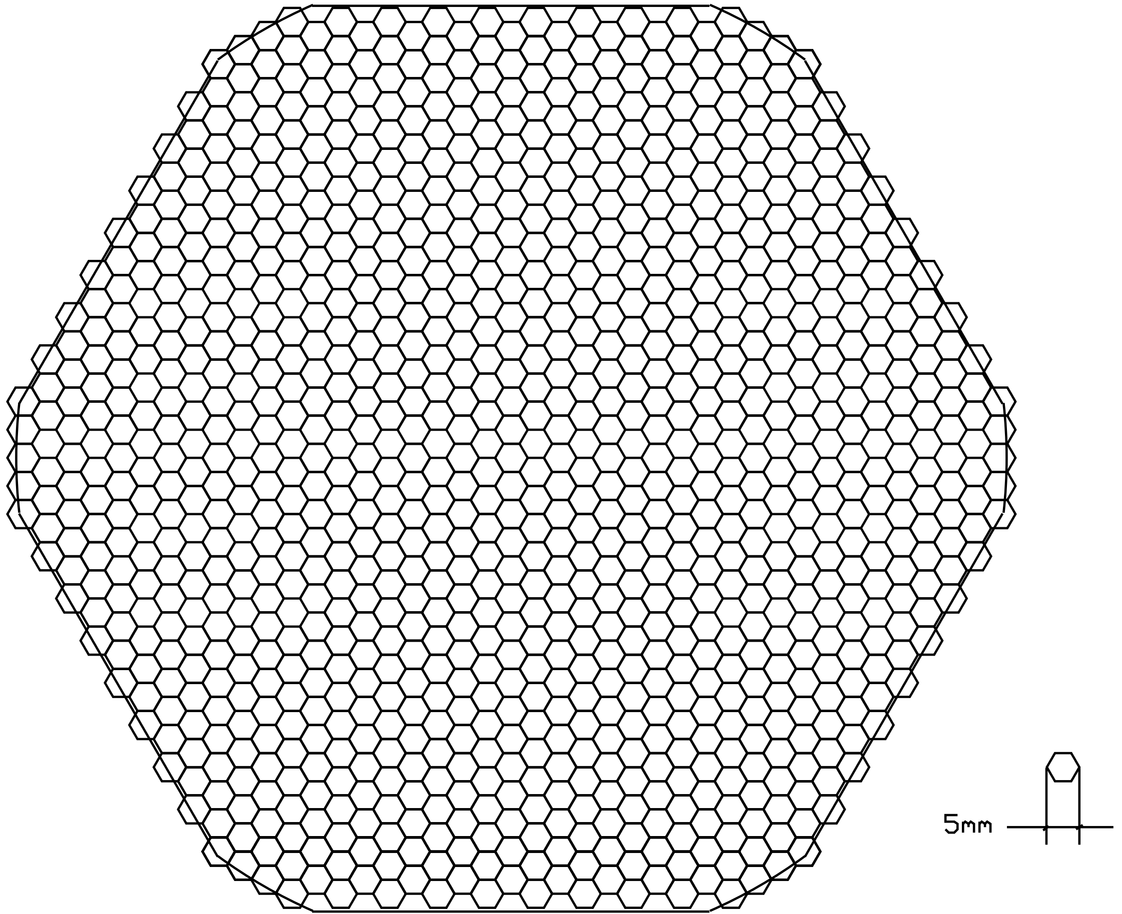

Figure 1: Detector layout with 5mm hexagon pads.

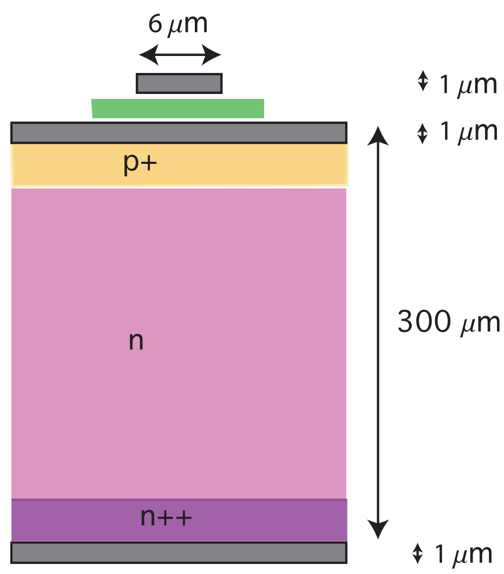

Figure 2: Cross section of Si detector, not to scale. The gray shows Al metalization. The green is insulator.

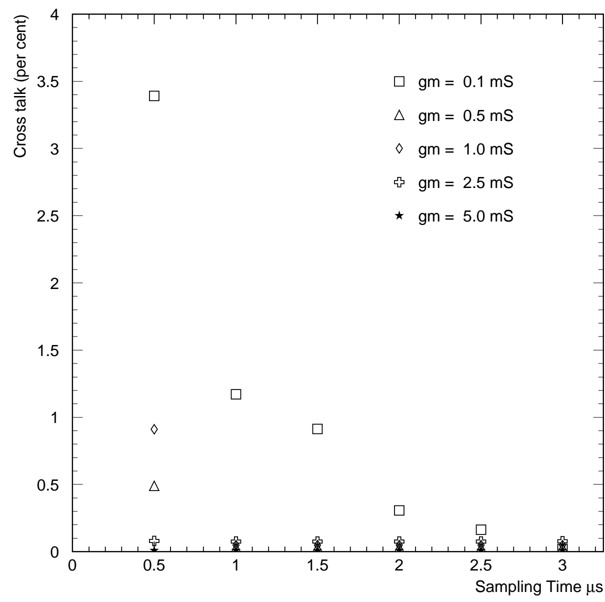

Figure 3: Cross talk versus sampling time for various values of the transconductance of the input FET in the charge amplifier.

2 Lorentz angle of holes and electrons

The Lorentz angle for charge carries in silicon is given by

$$\tan\alpha = \mu B \tag{1}$$

where μ is the electron or hole mobility and B is the magnetic field, in this case 5 T. Taking the hole mobility to be $\mu_h = 370\text{cm}^2/\text{Vs}$ we get a Lorentz angle of 10.5°. For the electrons the mobility is larger, $\mu_e = 1670\text{cm}^2/\text{Vs}$ giving a larger angle of 40°.

3 Radiation Damage

We can get some idea of the likely rate of radiation damage by looking at the rate from Bhabha scattering at small angles. This process has the largest cross section of any physics process in our detector and any machine background is likely to be limited to a similar rate.

The Born level cross section for Bhabha scattering (photon exchange only) is given by

$$\frac{d\sigma}{d\Omega} = \frac{\alpha^2}{2s}\left[\frac{1+\cos^4\frac{\theta}{2}}{\sin^4\frac{\theta}{2}} - 2\frac{\cos^4\frac{\theta}{2}}{\sin^2\frac{\theta}{2}} + \frac{1+\cos^2\theta}{2}\right]. \tag{2}$$

where s is the center-of-mass energy squared and θ is the polar angle with respect to the incoming beam. At small angles equation 2 reduces to

$$\frac{d\sigma}{d\theta} \sim \frac{32\pi\alpha^2}{s\theta^3} \tag{3}$$

which at 500 GeV evaluates to roughly

$$\frac{d\sigma}{d\theta} \sim \frac{10}{\theta^3}(pb) \tag{4}$$

assuming that acceptance of the detector begins at 60mrad, this gives a total cross section of roughly 1.5nb. For an instantaneous luminosity $\mathcal{L} = 10^{34}$ cm^{-2} s^{-1}, this would give a rate of 15 Hz.

Assuming an endcap calorimeter is located 1.7m from IP, the cross section of a single pad with area 0.1624 cm^2 at small angles is

$$\sigma_{pad} \simeq \frac{0.57}{(\theta/0.060)^4} pb. \tag{5}$$

when running at center-of-mass energy 500 GeV.

To calculate the flux in a given layer, we uses EGS which gives 315 MeV/layer at shower max. Which is corresponds to about 8 MIPs/GeV, giving a multiplicity for 250 GeV electrons of 2000 MIPs at shower max. We note that this is not all concentrated in a single pad, but for the purpose of calculating the average radiation dose we will treat it as if it were. (Note that at 250 GeV the showers are longer than at 45 GeV so the estimation of the dose at shower max is smaller than our previous result based on the OPAL luminosity monitor.) For a future linear collider at 500 GeV and a total integrated luminosity of 1000fb^{-1} the flux for pads near shower max at the inner edge of the detector would be 1.1×10^9/pad. This corresponds to a flux of $7.0 \times 10^9/\text{cm}^2$.

The radition dose at shower max in the more familiar unit of krad can be obtained by noting that the Si absorbs an energy dose of 0.315 GeV/ 250 GeV at shower max. At 60 mrad, this corresponds to an energy deposition of 3.7×10^7 GeV/cm^3. Converting to Joules/kg we obtain 2.5 Grays or 0.25 krad.

Using the damage constant from Lauber of

$$\alpha = 1.5 \times 10^{-8}\text{nA/cm}$$

and a detector thickness of $t = 0.03$cm, we obtain a worst case leakage current at 500 GeV center-of-mass energy of

$$\alpha \ t \ 1.1 \times 10^9 = 0.51\text{nA}$$

The expected upper limit on the neutron flux is $10 \times 10^{10}/\text{cm}^2$ which is somewhat more than the expectation from the Bhabhas. The damage coefficient is expected to be similar for the neutrons, giving a contribution to the leakage current from neutrons of roughly

$$7.3\text{nA/pixel.}$$

In most areas of the detector this will be the dominant effect.

The contribution from off-momentum beam electrons or positrons is much harder to estimate. At OPAL the rate of single electrons with energy more than 0.5 E_{beam} in the luminosity monitor was typically 50-500 times higher than the Bhabha cross section. In terms of bunch crossing, this corresponded to off-momentum particles in 1-5% of bunch crossings. At SLD the luminosity

monitor had trigger rates as high as 3Hz of coincidences of energy deposits of 10 GeV or more. Rather than being due to single off-momentum electrons as at LEP, this energy tended to be the sum of a diffuse background which was correlated between the two ends of the luminosity monitor.

One way to estimate the number of off-momentum particles at a future linear collider would be to assume that the machine would primarily operate with optics such that no more than 1% of all bunchlets had an off-momentum particle that was focused into the detector at an angle of greater than 60mrad. This would give a rate of $120 \times 192 \times 0.01 = 230$Hz which is much larger than the Bhabha rate. Assuming that these particles have an angular distribution like Bhabhas, but only half the energy (which was true at LEP), we could expect leakage currents as large as

$$\frac{1}{2} 0.51\text{nA} \times \frac{230\text{Hz}}{15\text{Hz}} = 4\text{nA}.$$

However, at 120mrad this rate would be a factor of 2^4 (see equation 5) smaller, giving a contribution similar to the neutrons.

4 Dependence of electronic noise on detector design

In X-band linear colliders the electronics will be configured to integrate over the entire bunch train. A conceptual diagram of the charge amplifier is shown in figure 4. First charge from the diode flows on to capacitor C_f. Note that inputs to both amplifiers are to first order "virtual grounds". Next, the bandwidth of the circuit is limited by a single stage RC low-pass filter. During the interval when the switch is open, the same currents flows through capacitors C and C_1 thus the signal on C and C_1 are related by gain factor $\frac{C}{C_1}$.

The transfer function for a voltage which is present at the input of the RC low-pass stage to voltage across the capacitor C is given by

$$T_{RC}(\omega) = \frac{1}{1 + j\omega\tau}$$

where $\tau = RC$. In operation at a linear collider the switch across capacitor C_1 will be opened just before the bunch trains arrive for a time interval $a\tau$ As

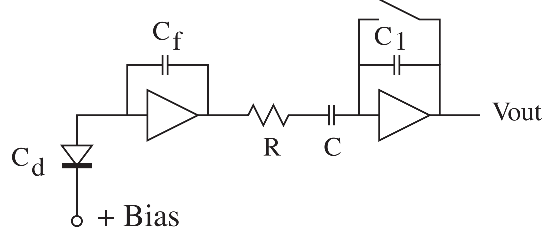

Figure 4: Conceptual amplifier design. The value of C_f is required to be 10pF or larger to accommodate the charge from the largest showers. The time constant RC is 200ns.

the current which flows through the capacitor C also flows through C_1, the feedback capacitor in the second amplifier, the output of the circuit (V_{out}) at time $t = a\tau$ is effectively the difference in the voltage across C at time $t = a\tau$ and time 0, giving a transfer function

$$T_{shape}(\omega) = \frac{e^{j\omega a\tau} - 1}{1 + j\omega\tau} \tag{6}$$

The absolute value is then

$$|T_{shape}(\omega)|^2 = \frac{2(1 - \cos\omega a\tau)}{1 + \omega^2 R^2 C^2} \tag{7}$$

The amount of "voltage" noise will be governed by the bandwidth product B which is this case is given by:

$$B = \int_0^\infty |T_{shape}(2\pi f)|^2 df = \frac{1}{2\tau}(1 - e^{-a})$$

In our case we will typically have a in the range 5 to 10 and the value of B will be $\frac{1}{2\tau}$. It is worth noting that this is just twice the value of a simple RC low pass filter. Since our sampling method amounts to taking the difference between two voltages, we would expect the noise to increase by $\sqrt{2}$ corresponding to an increase in B of a factor of 2.

4.1 Amplifier noise

The lower limit on the amplifier noise can be obtained by finding the noise from the input FET. The variance in the current flowing between source and

drain of an FET is given by

$$\delta^2_{i,FET} = 4KT(\frac{2}{3}g_m)df \tag{8}$$

where K is the Botzmann constant, T is the absolute temperature, g_m the transconductance and df is some small interval of frequency. This equivalent to a variance in the input voltage of

$$\delta^2_{v_in,FET} = 4KT\frac{2}{3g_m}\mathrm{d}f \tag{9}$$

which is in turn equivalent to a variance of the output voltage of

$$\delta^2_{v,out} = \frac{C_d}{C_f}4KT\frac{2}{3g_m}\frac{C}{C_1}\mathrm{d}f \tag{10}$$

In our case it is a good assumption that all of the charge from the input is collected onto the feedback capacitor C_f. Thus the voltage signal at the output from a single electron is

$$\frac{q_e}{C_f}(1-e^{-a})\frac{C}{C_1} \tag{11}$$

where q_e is the charge of a single electron and a is the ratio of the sampling time to the time constant of the integration stage τ. This gives a variance, in electrons, at the output of

$$\delta^2_{e,FET} = C_d^2 4\frac{KT}{q_e^2}\frac{2}{3g_m}\frac{|T_{shape}(2\pi f)|^2}{(1-e^{-a})^2}\mathrm{d}f \tag{12}$$

Integrating over all frequency we obtain an rms of

$$e_{rms,FET} = C_d\sqrt{4\frac{KT}{q_e^2}\frac{2}{3g_m}\frac{1}{2\tau}\frac{1}{(1-e^{-a})}} \tag{13}$$

Under our usual conditions ($T = 300$ K, $a > 5$) and g_m in mS and τ in μs, we obtain

$$e_{rms} = 14.4\sqrt{\frac{1}{\tau g_m}}C_d \tag{14}$$

where C_d is understood to include the detector capacitance as well as any stray capacitance and the capacitance of the input FET. Equation 14 only

includes the noise from the input transistor of the charge amplifier. We can expect that actual noise to be approximately twice as large.

In the present design we have $\tau = 0.2\mu$s and $g_m = 2$mS. For 1μm thick oxide between traces and pads and for channels located on the outer edge of the detector the stray capacitance is $\sim$ 15pF, and the capacitance of the input FET wil be $\sim$ 10pF giving a total capacitance of $\sim$ 30pF and a total amplifier noise of approximately 700 electrons. Assuming an equal amount of "excess" noise which adds in quadrature, the amplifier noise would then be approximately 1000 electrons. If the oxide can be only 0.5 μm thick, then the stray capacitance will double to $\sim$ 30pF and equation 14 predicts approximately 1000 electrons noise. If this is matched by an equal amount of excess noise we will have an amplifier noise of 1400 electrons which is still gives better than 10:1 signal to noise for MIPs.

Somewhat more problematic are the pads near the center of the detector. As the traces from all of the pads must be brought into the bump bound array, there will be consider stray capacitances due to all of the traces passing over the inner pads. In the present design the pitch of the bump bound array is 200 x 484. This gives pitch of traces coming into the array of 484/16 about 30μ. For 6 μm traces this gives a coverage of 20% corresponding to a stray capacitive load of $\sim 115pF$. Note that as we move out from the center of the detector the fractional area covered with traces we fall like $1/r$.

For the pads located directly under the chip, the pad may be covered with up to 50% bonding and probing pads. This would give a total capacitance of 290pF and a noise of 7000 electrons or 1/3 of a MIP.

4.2 Shot noise related to the leakage current

The noise (in electrons) due to the leakage current can be easily calculated in the case of our electronics if we assume that all of the charge is collected in time $a\tau$. Then the rms fluctuations in units of electrons are just

$$e_{rms,leak} = \sqrt{\frac{i_{leak} a\tau}{q_e}} \tag{15}$$

For 1 μs sampling time ($a = 5$) and 10nA leakage current this gives 250 electrons. The advantage of having a relatively long sample time is that the bunch-to-bunch variations in the signal amplitude for the 270ns trains are minimized; for 1 μs sampling time it is $\sim$ 0.7%. However, if the sampling

time is reduced to 500ns the shot noise will be reduced but the bunch-to-bunch fluctuations will grow to$\sim$ 25%. This may still be tolerable as the bunch times will be measured with a precision of a few ns. The electronics will be designed so that a can be dynamically changed on each readout chip. Thus if the leakage current dramatically increases a smaller value of a could be used.

For small values of a, equation 15 will no longer hold. The variance on a current in a diode in frequency interval df is given by

$$\delta^2_{i,shot} = 2q_e i_{leak} \mathrm{d}f \tag{16}$$

where i_{leak} is the leakage current. The transfer function which relates current at the input to voltage at the output is given by

$$T_i(\omega) = \frac{1}{j\omega C_f}\frac{e^{j\omega a\tau}-1}{1+j\omega\tau}\frac{C}{C_1} \tag{17}$$

The variance at the output in some frequency interval df in units of electrons referred to the input is then given by

$$\begin{aligned} \delta^2_{e,shot} &= 2q_e i_{leak} \frac{|T_i(2\pi f)|^2}{(\frac{q_e}{C_f}(1-e^{-a})\frac{C}{C_1}}\,)^2 \mathrm{d}f \\ &= 2i_{leak}\frac{1}{(2\pi f)^2}\frac{2(1-\cos 2\pi f a\tau)}{1+(2\pi f)^2\tau^2}\frac{1}{q_e(1-e^{-a})^2}\mathrm{d}f \end{aligned} \tag{18}$$

Integrating over all frequency and taking the square root, we then

$$e_{rms,leak} = \sqrt{\frac{I}{e}\tau\frac{a-1+e^{-a}}{1-e^{-a}}} \tag{19}$$

which reduces to equation 15 in the limit of large a.

In a DC coupling design the leakage current would be supplied by an FET in the charge amplifier. The leakage current flowing through this FET will increase the total shot noise from the leakage current by $\sqrt{2}$ over that predicted by equation 15 giving a total of contribution to the noise of 350 electrons from leakage current for 10nA leakage current.

In an AC coupled design we would have an additional contribution to the noise from the current through the bias resistor $i^2 = 4KT/R_{bias}$ for 200ns shaping in the large a limit this gives approximately

$$e_{bias} \sim 660\sqrt{\frac{a\tau}{R_{bias}}}$$

for R_{bias} in MΩ and τ μs.

4.3 Noise from series resistance of traces

The variance in current in some frequency interval of frequency df due to the series resistance R_s of the trace is given by

$$\delta^2_{i,R_s} = \frac{4KT}{R_s} \frac{1}{1 + \frac{1}{(2\pi f)^2 R_s^2 C_{tot}^2}} \mathrm{d}f \tag{20}$$

where K is the Botzmann constant, e is the electric charge, T is the temperature. Here C_d includes any stray capacitance in parallel with the detector capacitance and the capacitance of the FET. For the worst case $C_d = 45$pF with $R_s = 300\Omega$ giving a time constant of roughly 15 ns which is much shorter than amplifier shaping time of 200 ns. We can then approximate equation 20 as

$$\delta^2_{i,R_s} = 4KTC_d^2 R_s (2\pi f)^2 \mathrm{d}f \tag{21}$$

Using the transfer function relating a current at the input to charge in units of electrons at the output we obtain

$$\delta^2_{e,R_s} = 4KTC_d^2 R_s (2\pi f)^2 \frac{|T_i(2\pi f)|^2}{(\frac{q_e}{C_f}(1 - e^{-a})}) ^2 \mathrm{d}f \tag{22}$$

where T_i is given by equation 17. Integrating over all frequency we obtain

$$e_{rms,R_s} = C_d \sqrt{4 \frac{KT}{q_e^2} R_s \frac{1}{2\tau} \frac{1}{(1 - e^{-a})}} \tag{23}$$

Under our usual conditions ($T = 300$ K, $a > 5$) and R_s in Ω and τ in μs, we obtain

$$e_{rms,R_s} = 0.56 C_d \sqrt{\frac{R_s}{\tau}} \tag{24}$$

for noise in electrons and C_d in pF. For an oxide thickness of 1μm $C_d = 30$ pF and the worst case value of $R_s = 300\ \Omega$ this is gives 600 electrons noise. If the oxide is only 0.5μm thick, $C_d = 45$ pF and the noise is 975 electrons.

Note that stray capacitances between the traces and the other pads C_{stray} scales with the strip width, w while R_s scales inversely. In principle we could optimize the noise by decreasing strip width until the noise from the amplifier and the series resistance are equal. For the assumed value of the FET input capacitance of 10pF, the detector capacitances of 5.7pF , the oxide thickness 0.5 μm and assuming the amplifier noise is given by equation 14, the optimized strip width would be 3 μm, which may be too small to be reliably fabricated.

4.4 Charge noise summary

The expected contributions to the noise are summarized in table 3 for the baseline configuration of the detector and electronics. For the outer pads the totals are comfortably below the required signal noise of 1:7 corresponding to 3400 electrons. For the pads near the center the expected noise is slightly over the spec. This noise could be reduced by decreasing the thickness of the metalization near the bump bound porotion of the detectors. It should be noted that relatively few channels are near the detector center.

5 Timing measurement

The output of the charge amplifier may be used to produce timing a signal which can aid in the identification of the bunches and may be useful in rejecting background clusters. We have studied the performance of such a circuit using a toy Monte Carlo.

In the toy Monte Carlo we have assumed that the output of charge amplifier is used to trigger a discriminator when the output cross some threshold. The RC time of the timing circuit can be different than the charge amplifier. In general better timing resolution is obtained as the RC time is reduced. However, this implies a faster charge amplifier which may require too much power. As a baseline, we consider the case of a timing circuit which has the same RC time as the charge measurement, $RC_{timing} = \tau_{timing} = 200$ns.

Note that the transfer function needed to calculate the noise has only an upper frequency cut-off given by RC_{timing} and gives a noise from the

source	outer channels	channels near center
input FET	700	2980
excess noise	700	2980
leakage current	250	250
series resistance	600	-
quadrature total	1180	4220

Table 3: Noise values at end of life for the baseline detector and electronics. Baseline values are $\tau = 0.2\mu$s, $g_m = 2$mS, 1.0 μm oxide thickness, and $i_{leak} =$ 10 nA.

input FET and the series resistance which are $\frac{1}{\sqrt{2}}$ smaller than that given by equations 14 and 24. As before, we assume "excess" amplifier noise equal to the input FET noise. We ignore noise from leakage current. This gives a total of 820 electrons noise for the outer pads. Note that this noise corresponds to the worst case pads at the outer edge of the wafer. Our simulation has simple model of the capacitance of the traces as a function of there distance from the center of the detector and of the number of traces which pass over each pad. The threshold used for the time determination is set to 8000 electrons and assumed to have a common mode shift of 1%.

To evaluate the timing resolution we consider a calorimeter with 30 layers and assume a Landau distribution of the number of electrons with a mean value of 24,000 (see PDG). The radial position of each hit is randomly chosen and noise calculated accordingly. As can be seen in figure 5 there is a large variation in time with measured charge. Note that measured charge includes an independent source of noise and is quantized due to the finite granularity of the ADC. For the baseline simulation we assume that the noise in the timing measurement and the charge measurement are uncorrelated. To the extent that the noise from the first FET dominates and the charge and timing measurement have the same bandwidth this the two measurements will have correlated noise. Below we explore both options.

We then correct the measured times assuming that the parameters used to characterize the rise time of the pulses in the timing circuit are known to 5%. We then take the average of up to 30 measurements per track, requiring the measured charge was at least 12,000 electrons. The expected noise for each channel is taken into account when getting the average time. The resulting time resolution is shown in figure 6. Various other algorthims to minimize the timing resolution by using pulse heights and predicted errors for individual times have been tried and they give results similar to the simple average shown in figure 6. We obtain an rms of approximately 2.3ns whith almost all measurements contained in a 15ns interval. If the noise in the timing and charge measurement are assumed to be 100% correlated the rms drops to 1.9ns.

In practice it may be possible to have a faster shaping time, τ_{timing}, for the timing circuit which could improve the timing precision by a factor of 2 or more. On the other hand, it may be more difficult to characterize the charge-time relationship for each channel than we have assumed here. For example, if the parameters used in the charge-time relation are only known to 15% and there is a common mode threshold shift of 5%, the rms time resolutions

degrades by a factor of 3 to 6.5 ns for $\tau_{timing} = 200$ns. This degradation is smaller for faster shaping times; for $\tau_{timing} = 100$ns the rms degrades to 3.5ns when the parameters in the charge-time relation are poorly known. This implies a faster shaping time should be used for the timing circuit.

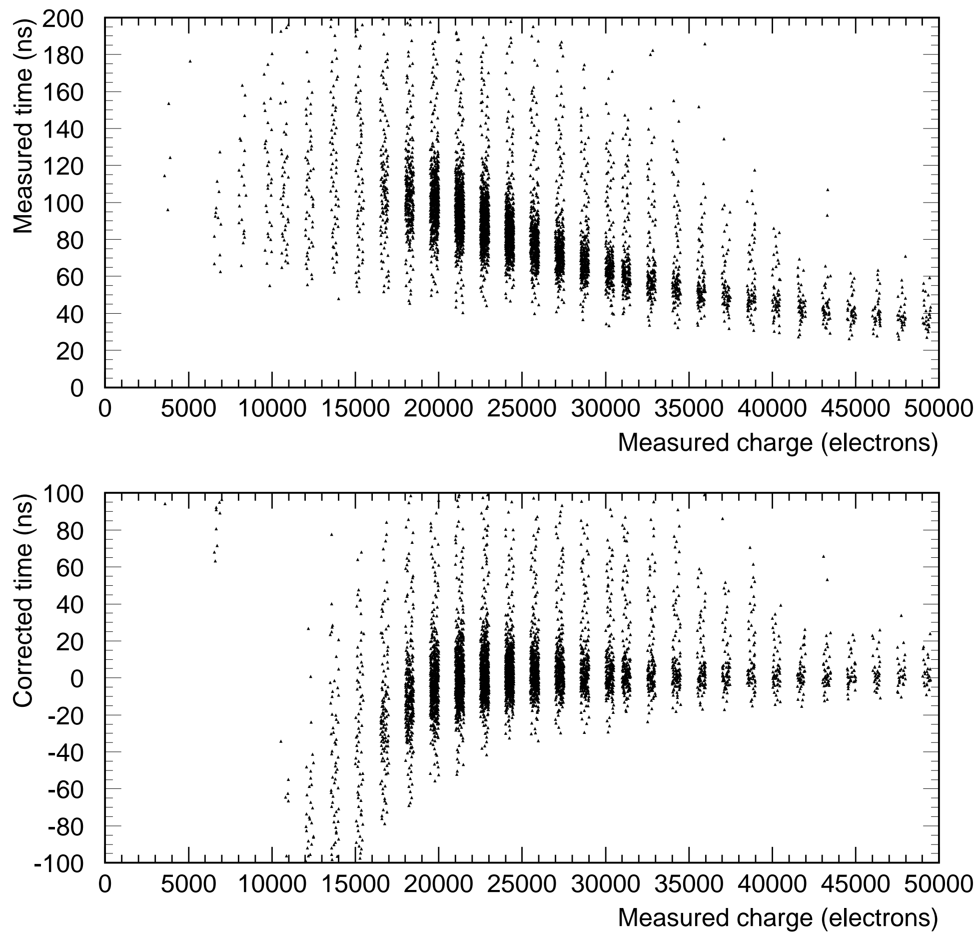

Figure 5: Top: measured time versus measured charged. The bands are due to granularity of the ADC. (In principle, the the charge values would appear as lines and not bands. They are shown as bands here to allow the scatter of the data to be seen.) Bottom: amplitude corrected time versus measured charged.

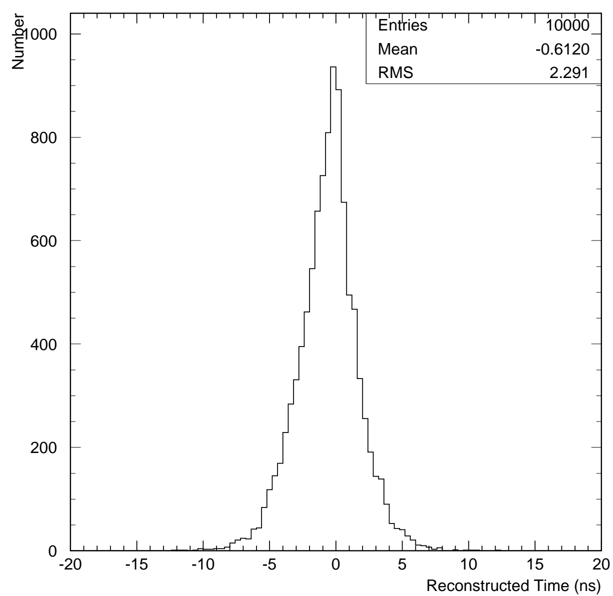

Figure 6: Mean time for reconstructed tracks assuming up to 30 mip samples in the calorimeter.

6 Conclusion

The performance of a silicon detector with integrated electronics has been evaluated for a prototype design. The electronics noise should be allow to allow for good sensitivity to MIPs. The cross talk from the detector is expected to be small compared to other parts of the detector. The timing resolution should be adequate to assign tracks to within a few bunchlets.

Possible areas for future research on the silicon detectors include exploring the reduction of the stray capacitive load of the pads near the detector center by using thinner traces and/or increasing the oxide thickness. In the present design the noise performance of the detector is dominated by the amplifier noise which is proportional to stray capacitance and not noise from leakage current.

Since the amplifier noise scales as $\sqrt{1/\tau}$ and noise from leakage current scale as $\sqrt{\tau}$ it is possible that the overall noise could be reduced by considering longer shaping times for the charge measurement. In addition every effort should also be made to keep the "excess" noise in the amplifier from being large.

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