Second Prototype Silicon Sensor Specifications for LC R&D

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1 Overview

Please see recent conference papers[1] or talks [2] for further background on the application of these detectors to elementary particle physics and the Linear Collider (LC) project. We plan to build a detector system for the LC which will use on order of 10 million cm^2 of silicon sensors. Each individual sensor will be of a size approximately given by the largest readily available silicon wafer, subject to economic considerations. For the second prototype sensors we plan to base our design on 6 inch wafers. These sensors will be subdivided into individual detector elements which we call *pixels*. We are developing a readout chip called "KPiX" with 1024 readout channels and we propose to divide the useable area of the silicon sensors into 1024 pixels. The KPiX chip is to be mounted directly to the silicon sensor using the bump-bonding technique. The KPiX chip will amplify, shape, buffer and digitize the input signals. Besides the inputs, the external connections to the KPiXs are only the few required for power, control, and for the serialized digital output. By integrating the detector readout in this way, we hope to control the cost and complexity of the project.

2 Sensor Layout

Figure 1 shows the suggested layout of pixels on a 6 inch (150 mm) wafer. The wafer has been cut into a hexagon with the vertices removed. We plan to assemble a detector module by placing such sensors side-by-side, as shown in Figure 2. It is necessary to remove the vertices of the hexagons so that circular spacers can be placed at the vertex of each sensor as shown in Figure 1.

To obtain 1024 pixels on the sensor, the individual pixels should be $\frac{1}{31}$ the size of the active area of the sensor. Scaling the pixel size by $\frac{1}{31}$ rather than $\frac{1}{32}$ leaves enough extra pixels to completely tile the active area of the sensor and to allow the pixels near the center of the sensor to be split as shown in Figure 1. The reason for splitting the pixels in the center of the wafer is to reduce stray capacitance from the traces on the second layer of metalization (see Section 4 below).

The detector readout is to be performed by a single readout chip (KPiX) which will provide complete analog and digital readout of all pixels. A schematic showing the KPiXs placement is given in Figure 3. A few representative traces between the pixels and KPiX are indicated. The traces should be spread out to limit the stray capacitance between the top of any one pixel and traces on the second layer of metalization.

Figure 4 shows a cross-sectional view in the vicinity of the KPiX. The few power, control, and output lines are shown as bump bond connections to traces on the kapton cable.

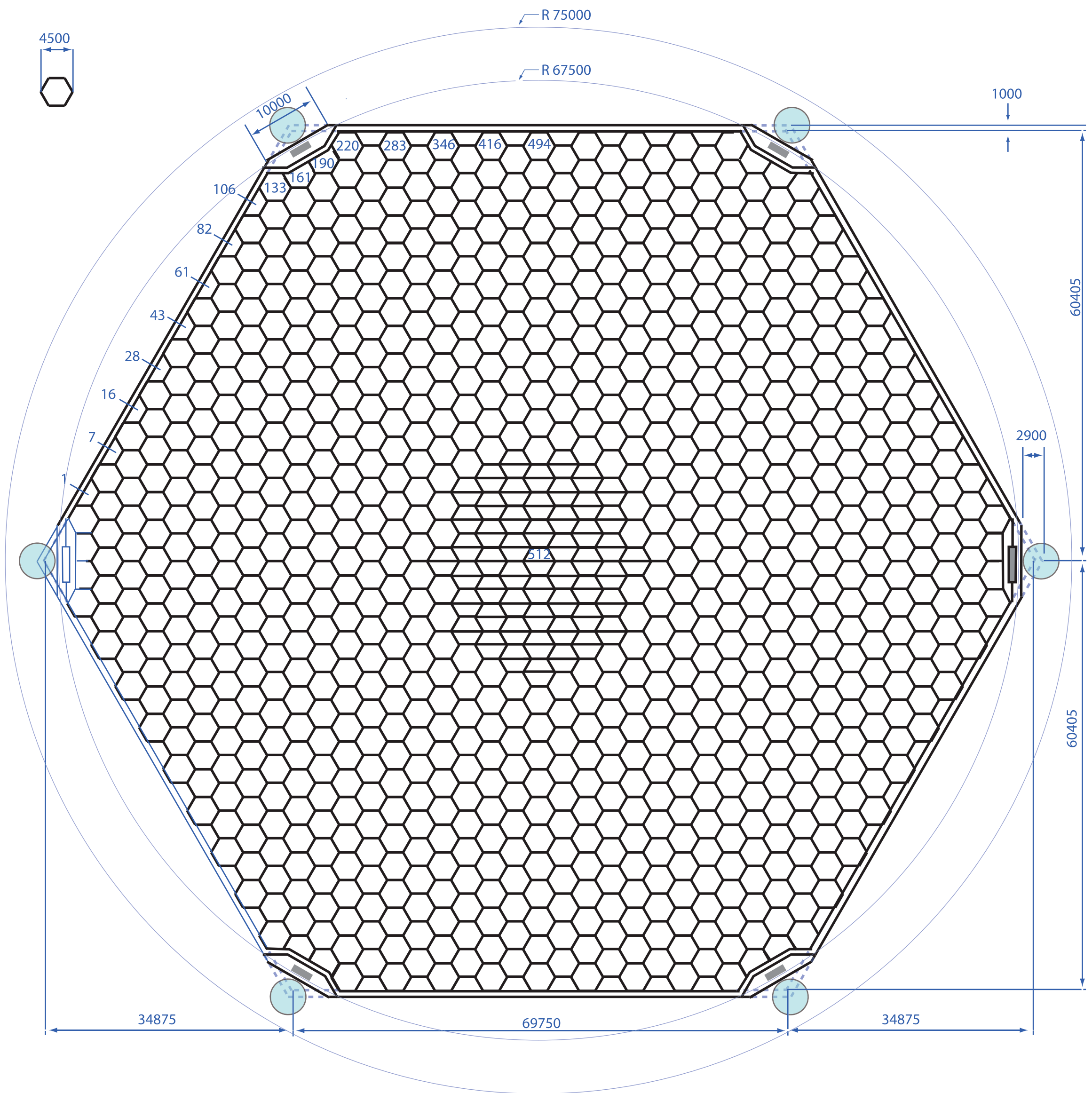

Figure 1: Suggested layout of pixels on the sensor wafer. All dimensions are given in microns. The dimensions generally correspond to edge of the active area of the sensor. Exceptions are 1000 μm showing the expected distance between the physical sensor edge and the active area of the sensor, 2900 μm showing the distance between the center of the spacers and physical edge of the sensor and 10,000 μm showing the length of the short sides of the detector. The shaded blue circles at the vertices of the hexagon correspond to the area needed by the spacers that hold the layers of the calorimeter apart. The outer blue circle with a radius of 75,000 μm shows the approximate wafer size. The inner blue circle with a radius of 67,500 μm shows the maximum extent of the active area of the first prototype sensors.

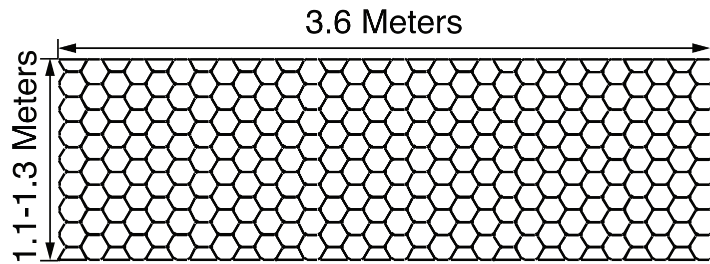

Figure 2: Assembling a layer from individual sensors.

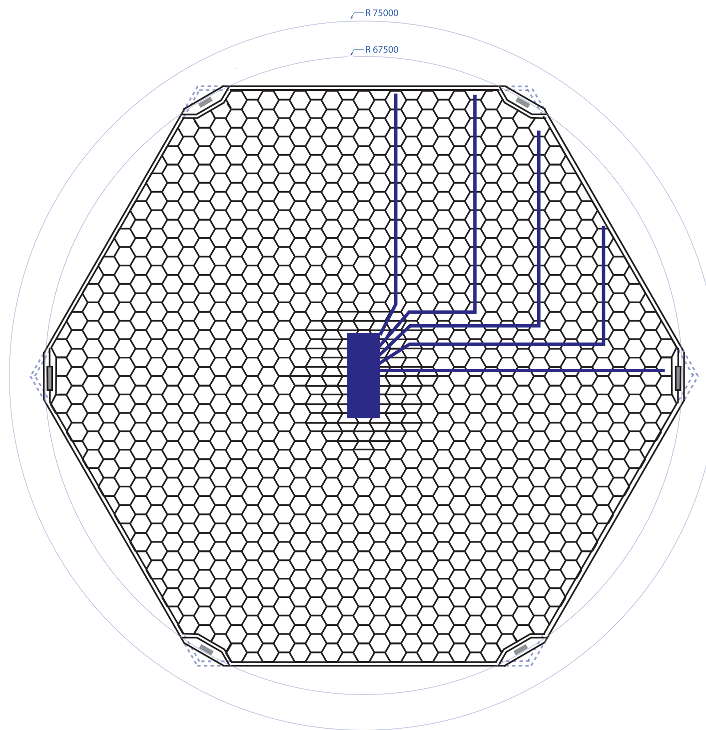

Figure 3: Schematic of KPiX placement on the wafer. A few representative traces (not to scale) between pixels and KPiXs are indicated in dark blue.

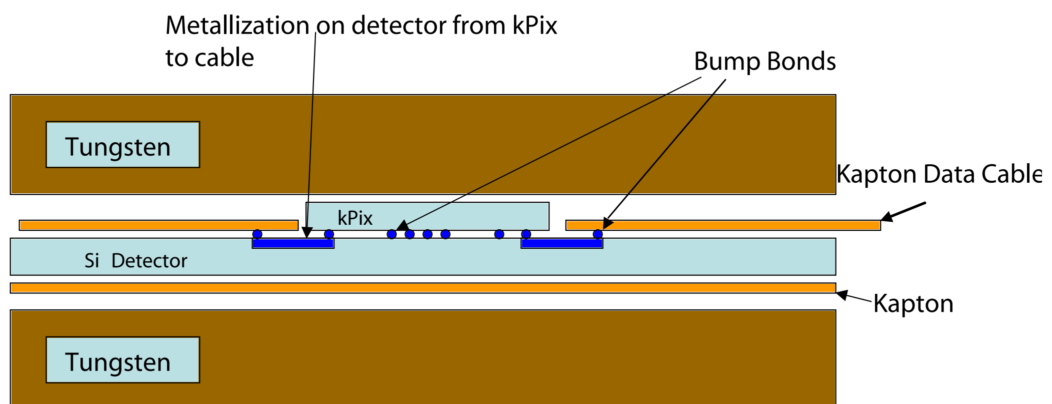

Figure 4: Cross section in the vicinity of the KPiX.

3 Sensor Structure

We wish to keep the sensor structure as simple as possible in order to minimize cost. In any case, we feel that our application does not require a complicated structure. We show a proposed structure for one pixel in Figure 5. The sensors are to have DC-coupled readout. The positive bias voltage is to be either applied to the backside of the sensor or to four topside bias pads located at four of the six vertices of the hexagon.

In addition to the usual metallization to provide the pixel electric field, we require a second metallization layer above for the traces which carry the pixel signals to the KPiX. The stray capacitances introduced by these traces will be manageable provided that the layer of dielectric is equivalent to at least 0.9 μm SiO_2. If possible, the traces should be narrower ($\sim 3\mu$m) in the vicinity of KPiX chip where there is a high number of traces crossing a given pixel. Farther from the KPiX where 16 or fewer traces cross a given pixel, the traces can be wider, ($\sim 6\mu$m).

During normal operation, there will be only a small voltage across the dielectric. However, during testing, it is possible that the bias voltage will occasionally be applied across the oxide layer. Therefore, the dielectric strength of the oxide layer should be at least as large as the depletion voltage of the detector.

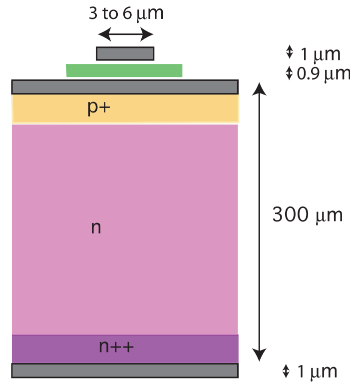

Figure 5: Schematic of detector cross section for one pixel.

- Detectors derived from maximum use of 6-inch (150 mm) wafers.
- DC-coupled readout.
- Detector thickness $\approx$ 300 to 350 μm.
- Two metallization layers.
- Insulator thickness should be at least 0.9 μm.
- The maker of the silicon detectors is not responsible for the electronics chip (KPiX), kapton cable, or connections to these.

- Detector bias voltage (positive) will be either to the sensor back side or the four top-side bias pads.

4 Metallization Layout

The upper metallization layer has the function of connecting the output signal from each pixel to the KPiX. These signal traces terminate in an array of bump bond pads, and the KPiX is to be bump-bonded to this array. Therefore, the KPiX will have one input connection per detector pixel for a total of 1024 signal connections. In addition the KPiX has 2×32 connections that are used for power, ground, control and I/O signals. Figure 6 shows the area near the bump-bond array, including the outline of the pixels on the first layer of metalization. In the KPiX chip, each channel has an area of 200μm $\times$ 500μm giving a pitch of 200μm in one direction and 500μm in the other.

Figure 7 shows a sketch of the bump-bond array plus signal trace metallization. The bump-bond array for the KPiX has $32 \times 34 = 1088$ pads of pixel inputs, consisting of $32 \times 32 = 1024$ pixel inputs plus two rows ($2 \times 32 = 64$ pads) that are connected with traces (see below) to the bump-bond array for the kapton cable. The centers of the two additional rows of bump bond pads are spaced 1 mm from the 32×32 of KPiX inputs and have a pitch of $200\,\mu$m. The center of bump-bond array should be centered on the horizontal and vertical axes of the detector as shown in Figure 6. Thus the 16th row of pixel input connections should be $250\,\mu$m above the horizontal detector axis as shown in Figure 6. Similarly the 16th column of KPiX pads should be $100\,\mu$m to right of the detector's vertical axis. Figure 8 shows some details of the proposed bump pads and the pitch of signal traces within the array.

Also shown in Figure 7 are two rows of 16 300μm $\times$ 300μm with a pitch of 500μm. These pads are connected to traces that supply power and carry control signals and I/O signals. The traces that supply power should be wide ($\sim 1\,mm$ or more) to keep their resistance low. The traces that supply control signals that are active during the data acquisition phase should be narrow and symmetrical to avoid any pickup to the pixels under the traces. The traces that are especially crucial are the pairs labeled CLKP,CLKPM and TRIGP,TRIGM. These traces carry differential signals during the data acquisition phase and each pair should be constructed so that the capacitive coupling to the pixels that they cross is as identical as possible.

Please note that the indicated layout of traces connecting the bump-bond array to individual pixels is meant to be conceptual only. The parts of the layout which are fixed by us are that of the bump-bond pads: their number, size, and spacing. These are determined by the KPiX geometry and the geometry of the kapton cable. With the layout concept we show, the number of traces and their pitch and width is within our specificiations and, we believe, within the range of what is possible for the fabricator. We do not, however, attempt to show any detailed configuration for the signal traces outside of the bump-bond array, as we assume the vendor will provide this.

In Figure 8 we see that for every bump bond pad there is an adjacent connected pad for probing and testing. This is required so that probes do not damage the surface of the bump bond pads.

To summarize a few points concerning the metallization layout:

- We assume aluminum metallization.

- We assume oxide thickness between the two metallization layers to be at least 0.9 μm of SiO_2.

- The KPiX bump-bond pad array layout (1088 $50\mu m \times 50\mu m$ pads) is fixed by the KPiX, and is to be as shown.

- The KPiX bump bonding array should be placed at the center of the sensor.

- The cable bump-bond pad array layout has 2×16 $300\mu m \times 300\mu m$ pads with $500\mu m$ pitch. The centers of the two rows of cable bump-bond pads are offset by 2.5 mm from the first and last row of KPiX pads.

- The signal trace dimensions and pitch are determined by signal to noise and crosstalk considerations. Our optimized dimensions (as shown in the drawings) are:

  - 3 μm wide near the KPiX;
  - 6 μm wide far from the KPiX;
  - 1 μm thick;
  - typical pitch of 20 μm within the bump pad array;

- The layout of the signal traces outside of the bump-bond array can be optimized by the detector manufacturer as appropriate, but to avoid excessive capacitive coupling to any one pixel, the traces should be fanned out in the area near the KPiXs that contain split pixels.

- Four fiducial marks should be provided to aid in positioning the KPiX chip and the kapton cable in the bonding process. These marks should be aligned with the centers of the first and last rows of the KPiX bump-bond array and with the centers of the first and last columns of the $300\mu m \times 300\mu m$ pads. These marks are shown in Figures 6, 7 and 8.

- We would like openings to be provided in a small number (~ 10) of pixels to allow testing with an IR laser.

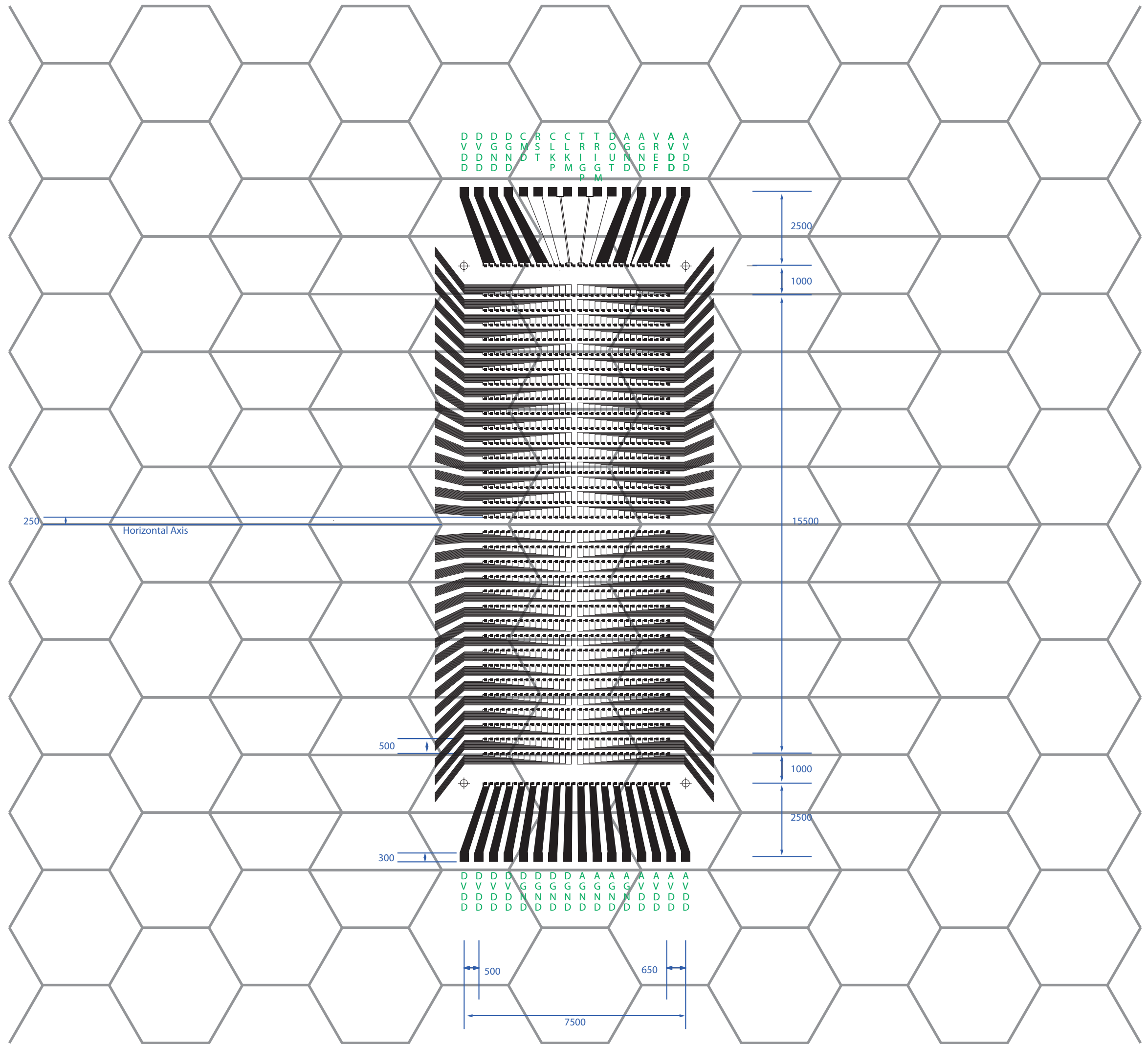

Figure 6: Central portion of the sensor showing the bonding array (approximately 4 × actual size). The dimensions shown in blue are microns. Labels for the signal names are shown in green.

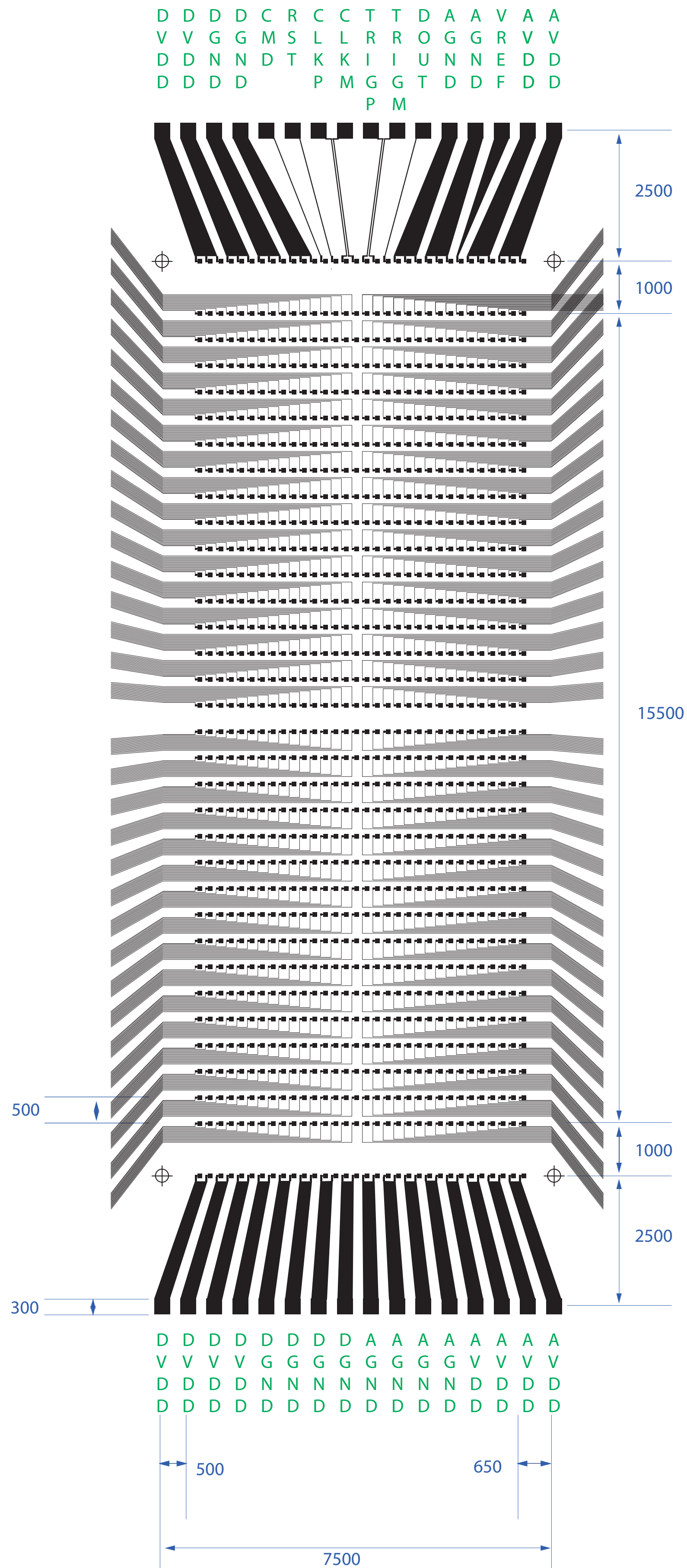

Figure 7: Bump-bond array (approximately 8 × actual size). The dimensions shown in blue are microns. Labels for the signal names are shown in green.

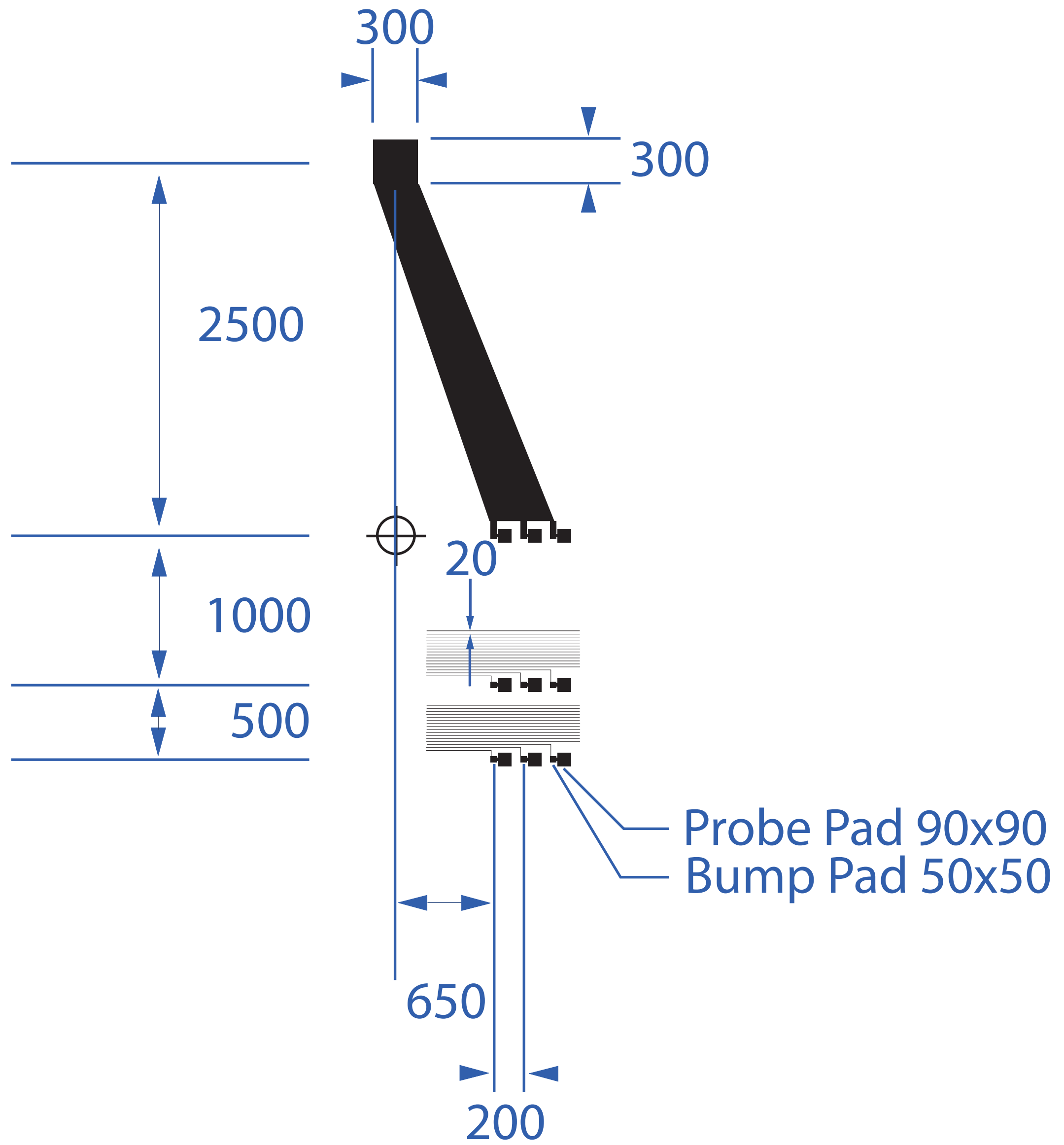

Figure 8: Bump-bond array detail. Metalization is shown in black. The dimensions shown in blue are microns.

5 Top Side Bias and Guard Ring

For the second round of prototypes we are interested in testing a top side bias scheme. In this configuration the bias will be connected to four bias pads at four of the six vertices of the sensor. The connection between the top side and the back-side of the detector can be of relatively high resistance ($< 500\mathrm{k}\Omega$). We plan to explore configurations of the sensor where the back side is capacitively coupled to the signal ground of the KPiX chip. If these schemes prove unworkable, we will connect the bias directly to the back detector. A detail of the suggested layout for the top side bias is shown in Figure 9. The dimensions are suggested ones; the bonding pad should be at least $300\mu\mathrm{m} \times 300\mu\mathrm{m}$, in addition, the bonding pad should be at least $300\mu\mathrm{m}$ from the guard ring.

Access to the guard ring is provided by bonding pads at two locations. A detail of one of the suggested dimensions of one of these pads is shown in Figure 10. We assume that the distance between the active edge of the detector and the physical edge of the detector will be 1 mm.

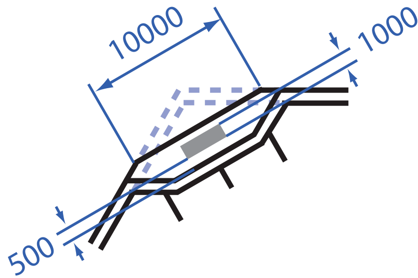

Figure 9: Suggested top side bias bonding pad. Metalization is shown in black and gray. The dimensions shown in blue are microns.

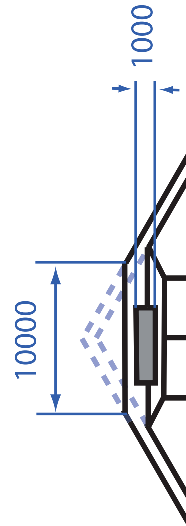

Figure 10: Suggested guard ring pad. Metalization is shown in black and gray. The dimensions shown in blue are microns.

6 Silicon Performance Requirements

We assume detectors are pure, high-resistivity silicon with full depletion voltage in the usual range 50 to 200 V, as is typical for detectors of this thickness. Hence, we expect leakage current for most pixels at full depletion will normally be at the level of a few nA. At high leakage current levels, the signal/noise will effectively make a pixel inoperable (dead) or unacceptably noisy. With our current readout electronics model, this will occur at about 40 nA. Note that we expect that these detectors

will operate in the temperature range 20°C to 40°C. We do not expect an appreciable increase in leakage current due to radiation damage during the detector lifetime. For the final detectors, we would like to negotiate with the vendor what fraction of dead pixels are considered acceptable for a detector, especially as it might impact cost. For the second prototypes we require that an acceptable detector have fewer than 1% of its pixels which are dead or exceed 40 nA leakge current at full depletion.

7 Other Requirements

For the initial prototypes, we expect an order of about 40 detectors. It is possible that we will structure the project in two phases. Phase I consists of the production of the masks and some other nonrecurrent engineering costs. Phase II consists of the actual production of the detectors. The schedule for completion of Phase I and Phase II will be negotiated with the vendor.

References

[1] D. Strom *et al.*, "First results with the prototype detectors of the Si/W ECAL," SLAC-PUB-11335, SPIRES entry *Presented at 2005 International Linear Collider Workshop (LCWS 2005), Stanford, California, 18-22 Mar 2005*
D. Strom *et al.*, "Fine Grained Silicon-Tungsten Calorimetry for a Linear Collider Detector," IEEE Trans. Nucl. Sci. **52**, 868 (2005).

[2] M. Breidenbach, Silicon-tungsten ECal - Recent Results and Plans, Presented at VLCW06, 19-23 July 2006, Vancouver, B.C. Canada.