

# Initial Prototype Silicon Detector Specifications for LC R&D

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## 1 Overview

Please see the conference paper[1] or talk[2] for further background on the application of these detectors to elementary particle physics and the Linear Collider (LC) project. We plan to build a detector system for the LC which will use on order of 10 million  $\text{cm}^2$  of silicon detectors. Each individual detector will be of size approximately given by the largest readily available silicon wafer, subject to economic considerations. These detectors will be subdivided into individual detector elements which we will call *pixels*. The pixel size is approximately 5 mm across, or about  $0.25 \text{ cm}^2$ . Hence, for a 6 inch wafer, there would be somewhat less than 1000 pixels per detector. We plan to readout the signal information using one electronic chip per wafer. This readout chip (ROC) is to be mounted directly to the silicon detector using the bump-bonding technique. The ROC will amplify, shape, multiplex, and digitize the input signals. Besides the inputs, the external connections to the ROC are only the few required for power, control, and for the serialized digital output. By integrating the detector readout in this way, we hope to control the cost and complexity of the project.

## 2 Detector Layout

Figure 1 shows one possible layout of pixels on a 6 inch wafer. The wafer has been cut into a hexagon with rounded corners. A guard ring will presumably be required on the perimeter of the wafer, but is not shown in the drawing. We plan to assemble a detector module by placing such detectors side-by-side, as shown in Figure 2.

- The detector pixels are  $5 \text{ mm} \times 5 \text{ mm}$  in area, as shown.
- The number of pixels for a 6-inch wafer will be  $\approx 750$  to 800, depending on pixel shape and the width of the guard ring and any unuseable area on the perimeter of the wafer.

The detector readout is to be performed by a single readout chip (ROC) which will provide complete analog and digital readout of all pixels. A schematic showing a possible ROC placement is given in Figure 3. A few representative traces between pixels and ROC are indicated.

Figure 4 shows a cross-sectional view in the vicinity of the ROC. The silicon detector is supported by a G10 (or similar) board. The few power, control, and output lines are shown

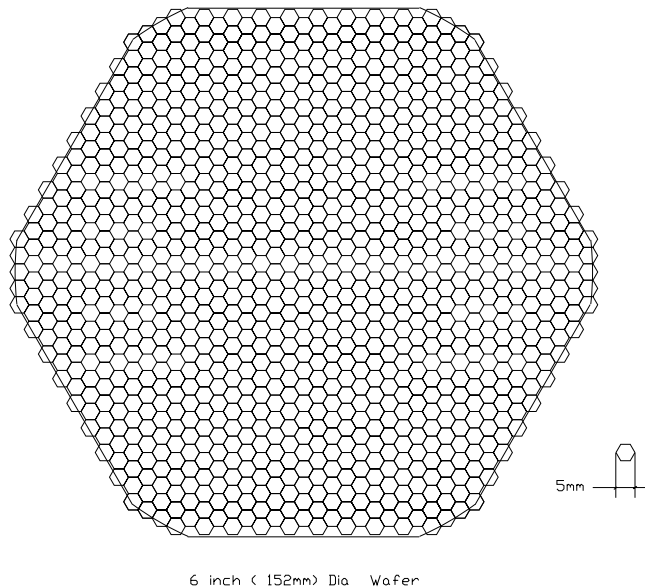


Figure 1: Possible layout of pixels on detector wafer.

as wire bond connections to traces on the G10 board. We are presently considering other options besides wire bonds, for example by through-plated holes in the G10, to provide these connections.

### 3 Detector Structure

We wish to keep the detector structure as simple as possible in order to minimize cost. In any case, we feel that our application does not require a complicated structure. We show a proposed structure for one pixel in Figure 5. The detectors are to have DC-coupled readout. The positive bias voltage is to be applied to the detector backside (bottom of the figure). We do not have a favorite idea for how to apply the bias voltage. In addition to the usual metallization to provide the pixel electric field, we require a second metallization layer above for the traces which carry the pixel signals to the ROC. We have studied the capacitance necessary for the upper insulating (oxide) layer, as shown in the figure. We believe these are within the usual fabrication range.

- Detectors derived from maximum use of 6-inch (150 mm) wafers.
- DC-coupled readout.
- Detector thickness  $\approx$  300 to 350  $\mu\text{m}$ .
- Two metallization layers.
- $\text{SiO}_2$  insulator thickness should be 1  $\mu\text{m}$ .

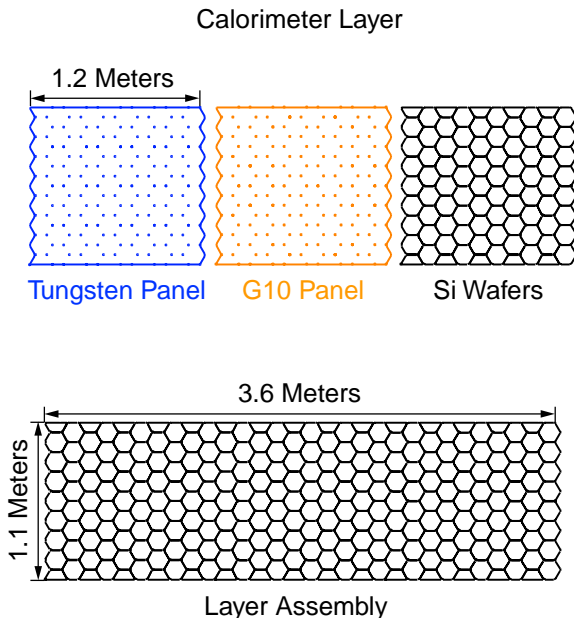


Figure 2: Assembling a layer from individual detectors.

- The maker of the silicon detectors is not responsible for the electronics chip (ROC), PCB board, or connections to these.
- Detector bias voltage (positive) will be connected to the detector back side.

## 4 Metallization Layout

The upper metallization layer has the function of connecting the output signal from each pixel to the ROC. These signal traces terminate in an array of bump bond pads, and the ROC is to be bump-bonded to this array. So the ROC will have one input connection per detector pixel. Figure 6 shows our current idea for a bump-bond array. The pitch of the array corresponds to a ROC of size  $6.2 \times 17.5 \text{ mm}^2$ . (Each electronics channel uses an area  $0.200 \times 0.500 \text{ mm}^2$ . Figure 7 shows some details of the proposed bump pads and the dimensions and pitch of signal traces within the array. Figure 8 shows a sketch of the bump-bond array plus signal trace metallization.

Please note that the indicated layout of traces is meant to be conceptual only. The only part of the layout which is fixed by us is that of the bump-bond pads: their number, size, and spacing. These are determined by the ROC geometry. With the layout concept we show, the number of traces and their pitch and width is within our specifications and, we believe, within the range of what is possible for the fabricator. We do not, however, attempt to show any detailed configuration for the signal traces outside of the bump-bond array, as we assume the vendor will provide this.

For our conceptual layout, shown in the figures, the bump-bond array has  $32 \times 34 = 1088$  pads of pixel inputs, consisting of  $32 \times 32 = 1064$  pixel inputs plus two rows ( $2 \times 32 = 64$  pads) for connections to the PCB (see Figure 11). The input pads will be connected to

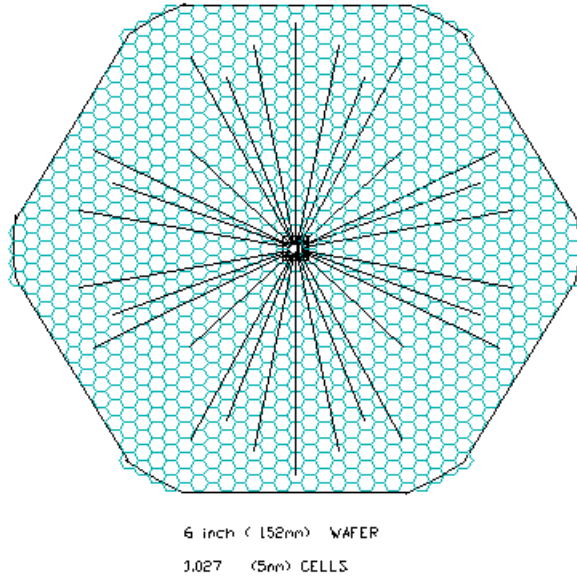


Figure 3: Schematic of ROC placement of the wafer. A few representative traces between pixels and ROC are indicated.

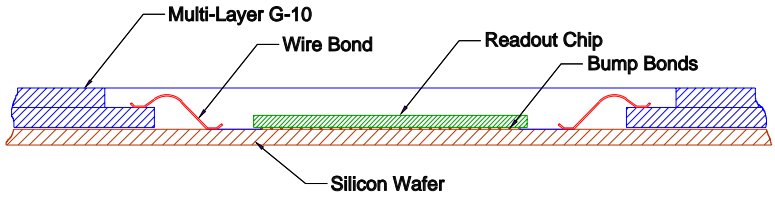


Figure 4: Cross section in the vicinity of the ROC.

$\approx 750$  to  $800$  pixels for a 6-inch wafer, thus leaving about 25% unconnected. This is OK, as we may wish to connect to more pixels in a later version.

In Figure 7 we see that for every bump bond pad there is an adjacent connected pad for probing and testing. This is required so that probes do not damage the surface of the bump bond pads.

To summarize a few points concerning the metallization layout:

- We assume aluminum metallization.
- We assume oxide thickness between the two metallization layers to be  $1 \mu\text{m}$  of  $\text{SiO}_2$ .
- The bump-bond pad array layout is fixed by the ROC, and is to be as shown.
- The signal trace dimensions and pitch are determined by signal to noise and crosstalk considerations. Our optimized dimensions (as shown in the drawings) are:

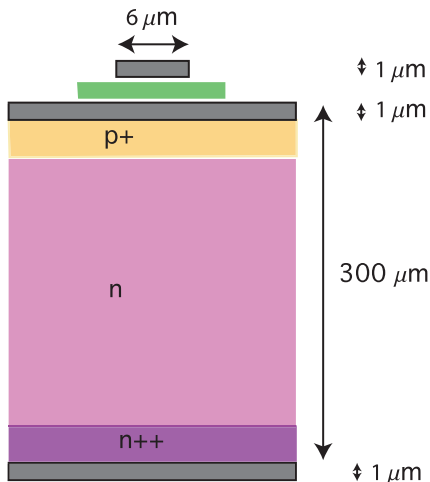


Figure 5: Schematic of detector cross section for one pixel.

- 6  $\mu\text{m}$  wide;
- 1  $\mu\text{m}$  thick;
- typical pitch of 25  $\mu\text{m}$  within the bump pad array;
- The layout of the signal traces outside of the bump-bond array can be optimized by the detector manufacturer as appropriate.
- We would like openings to be provided in a small number ( $\sim 10$ ) pixels to allow testing with an IR laser.

## 5 Silicon Performance Requirements

We assume detectors are pure, high-resistivity silicon with full depletion voltage in the usual range 50 to 200 V, as is typical for detectors of this thickness. Hence, we expect leakage current for most pixels at full depletion will normally be at the level of a few nA. At high leakage current levels, the signal/noise will effectively make a pixel inoperable (dead) or unacceptably noisy. With our current readout electronics model, this will occur at about 40 nA. Note that we expect that these detectors will operate in the temperature range 20°C to 40°C. We do not expect an appreciable increase in leakage current due to radiation damage during the detector lifetime. For the final detectors, we would like negotiate with the vendor what fraction of dead pixels are considered acceptable for a detector, especially as it might impact cost. For the initial prototypes we require that an acceptable detector have fewer than 1% of its pixels which are dead or exceed 40 nA leakage current at full depletion.

## 6 Other Requirements

For the initial prototypes, we expect an order of about 10 detectors. Delivery of the full order should be completed by January 30, 2004.

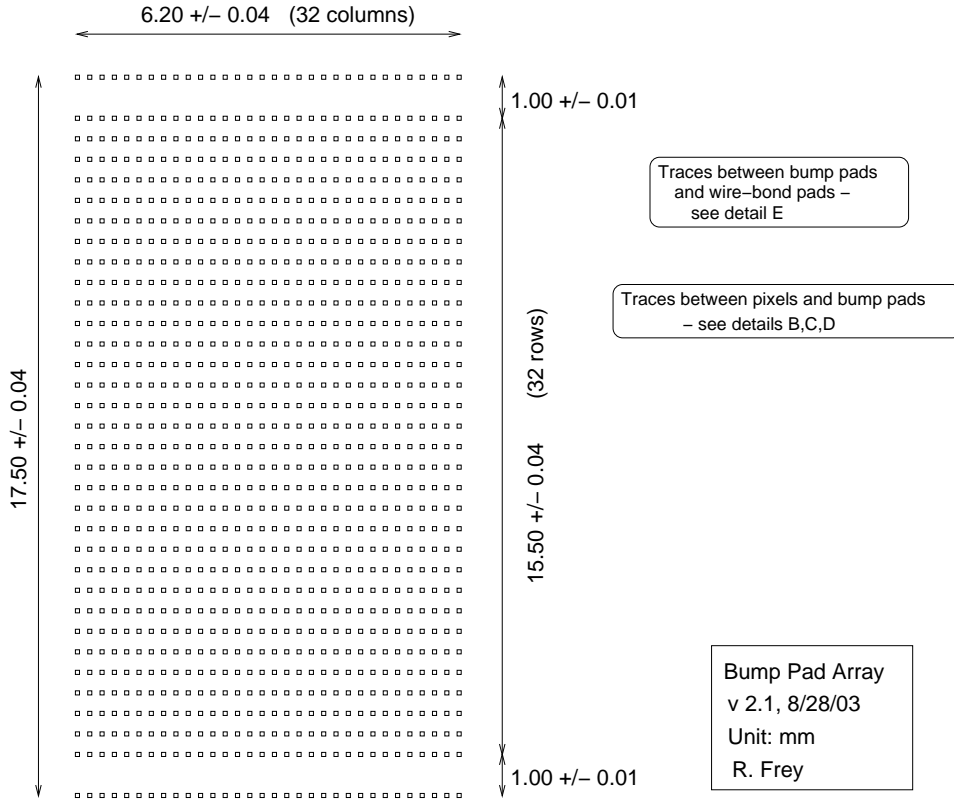


Figure 6: Bump-bond array.

## References

- [1] R. Frey, Proceedings of Calor2002, Pasadena, CA, March 2002,  
[http://zebu.uoregon.edu/~rayfrey/LC/SiW/frey\\_calor02\\_silicon\\_proc.pdf](http://zebu.uoregon.edu/~rayfrey/LC/SiW/frey_calor02_silicon_proc.pdf)
- [2] R. Frey, Talk slides from LCWS2002, Korea, August 2002,  
[http://zebu.uoregon.edu/~rayfrey/LC/SiW/frey\\_lcws02\\_silicon\\_talk.pdf](http://zebu.uoregon.edu/~rayfrey/LC/SiW/frey_lcws02_silicon_talk.pdf)

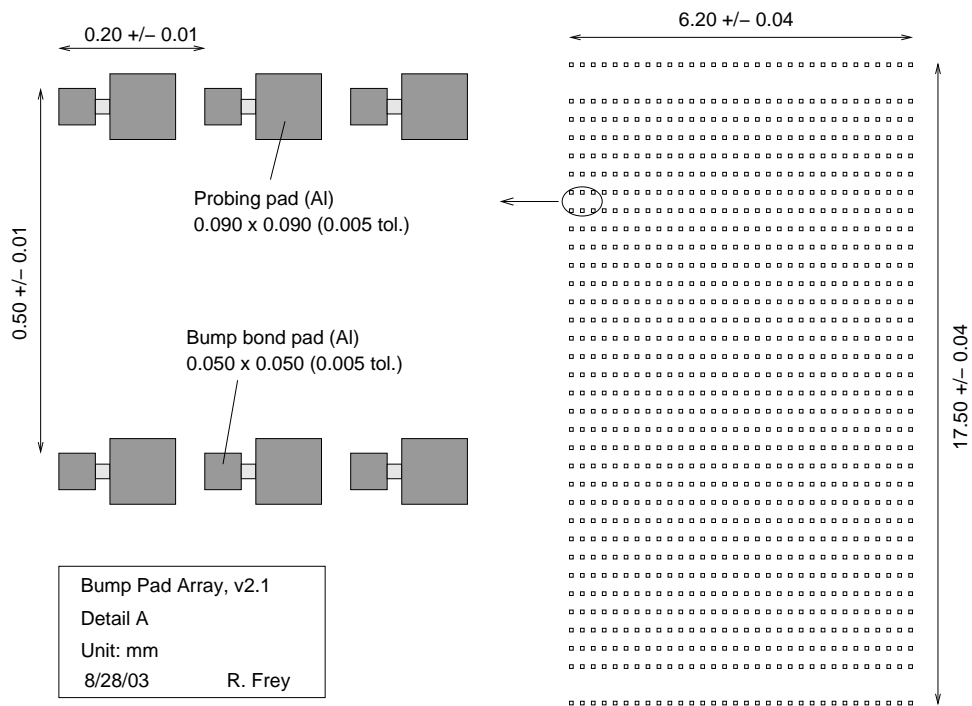


Figure 7: Bump-bond array detail.

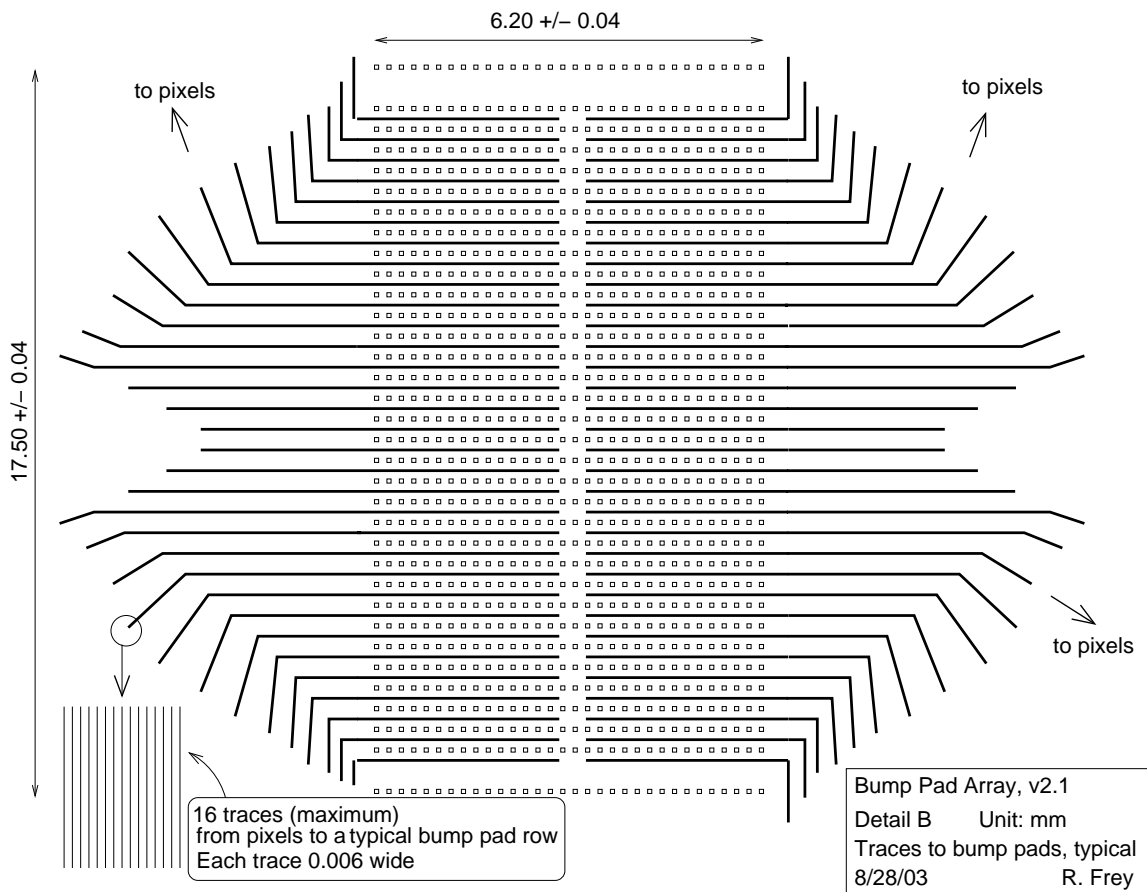


Figure 8: Bump-bond array and signal traces. The indicated layout of traces is conceptual only.

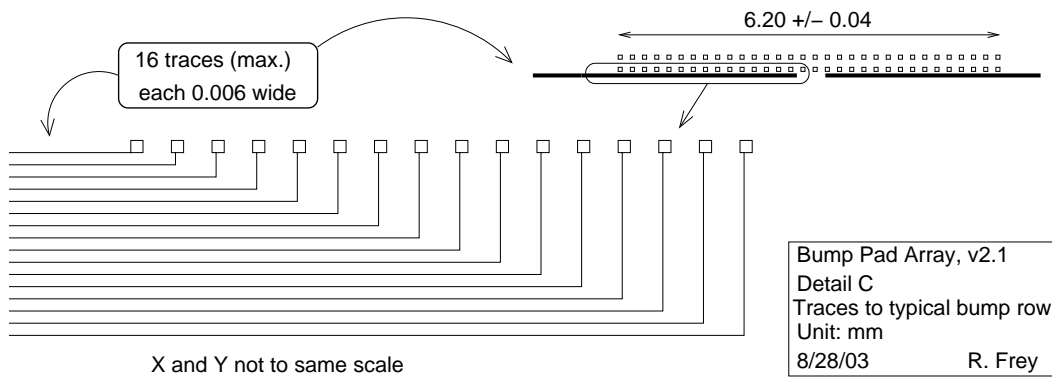


Figure 9: Bump-bond array and signal trace detail.

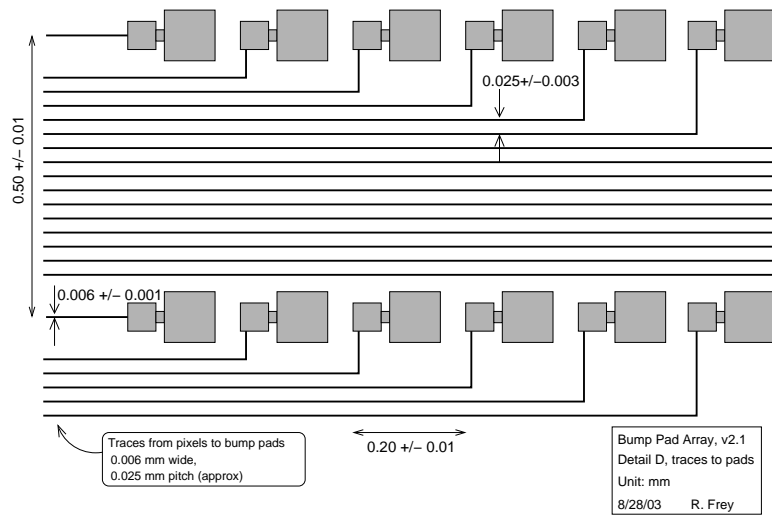


Figure 10: Bump-bond pads and signal traces detail.

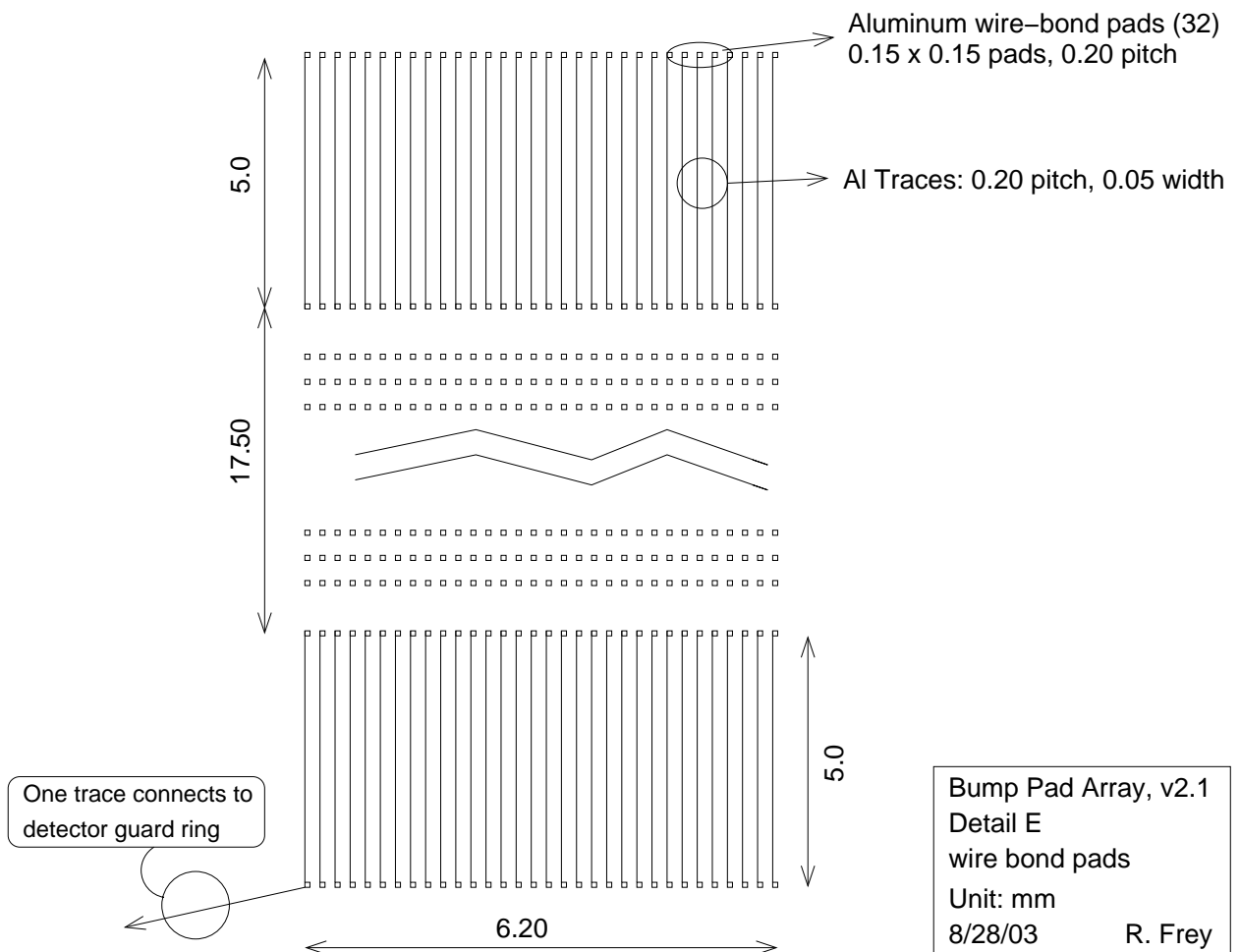


Figure 11: Bump bond array detail showing the wire bond pads and traces. We include one trace which connects to the detector guard ring, to allow its grounding to the mother board.