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THE DEVELOPMENT OF THE ELECTRICALLY CONTROLLED HIGH POWER RF SWITCH AND ITS APPLICATION TO ACTIVE RF PULSE COMPRESSION SYSTEMS

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I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and quality, as dissertation for the degree of Doctor of Philosophy.

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ABSTRACT

In the past decades, there has been increasing interest in pulsed high power RF sources for building high-gradient high-energy particle accelerators. Passive RF pulse compression systems have been used in many applications to match the available RF sources to the loads requiring higher RF power but a shorter pulse. Theoretically, an active RF pulse compression system has the advantage of higher efficiency and compactness over the passive system. However, the key component for such a system – an element capable of switching hundreds of megawatts of RF power in a short time compared to the compressed pulse width – is still an open problem.

In this dissertation, we present a switch module composed of an active window based on the bulk effects in semiconductor, a circular waveguide three-port network and a movable short plane, with the capability to adjust the S-parameters before and after switching. The RF properties of the switch module were analyzed. We give the scaling laws of the multiple-element switch systems, which allow the expansion of the system to a higher power level.

We present a novel overmoded design for the circular waveguide three-port network and the associated circular-to-rectangular mode-converter. We also detail the design and synthesis process of this novel mode-converter.

We demonstrate an electrically controlled ultra-fast high power X-band RF active window built with PIN diodes on high resistivity silicon. The window is capable of handling multi-megawatt RF power and can switch in 2-300ns with a 1000A current driver. A low power active pulse compression experiment was carried out with the switch

module and a 375ns resonant delay line, obtaining 8 times compression gain with a compression ratio of 20.

ACKNOWLEDGMENTS

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I am also grateful to all the staff at the Stanford Nanofabrication Facility, where I completed the fabrication of the switch window. I would thank Eric Perozziello for the insightful discussion regarding the process of the devices. I would also appreciate Maurice Stevens, Uli Thumser, Nancy Latta, Gladys Sarmiento, and all the other SNF staff, for providing the training, support, and consultation on the processing equipments.

DEDICATION

The author wishes to dedicate this dissertation to his grandparents Hanxiang Guo and Zunde Liu, who have been consistently encouraging him for the pursuit of higher academic achievements since his childhood.

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CHAPTER 1: INTRODUCTION

1.1 HIGH ENERGY CHARGED PARTICLE ACCELERATORS

High-energy particle accelerators are essential tools for particle physics research and other fundamental sciences. Accelerators can provide controllable charged particle beams with high energy and high intensity. When two high-energy particle beams collide, different elementary particles, which are rare under normal circumstances, can be generated for particle physics research. By curving high-energy charged particle beams (usually using particles with small rest mass, such as electrons or positrons) in magnetic fields, or by colliding a charged particle beam with a photon beam, high intensity photon beams of different wavelengths can be generated as Synchrotron Radiation or as a Free Electron Laser (FEL) output. These photon beams have high intensity and many other advantages that are not available with conventional light sources, especially in the shorter wavelength region, for example X-Rays. This makes accelerator based light sources very useful for research in the fields of physics, chemistry, biology, and material science.

Currently, most of the world's existing high energy accelerator-based light sources or colliders are circular storage rings. In storage rings, the particles are confined within designated circular orbits by bending magnets and focusing magnets. Usually there are several microwave accelerator cavities along the orbit. Each time the particles pass through the cavities with a certain phase, they can get accelerated. After injection and being accelerated to a desired energy, the particles can be stored for hours or days. The microwave cavities are mainly used to replenish the energy loss from synchrotron radiation and to provide longitudinal focusing. Thus the microwave load is usually close to constant and comparatively low. Nonetheless, the particle energy loss per turn from the synchrotron radiation in bending magnets is proportional to the cube of γ (the ratio of the particle energy to its rest mass) with a given field strength in the bending magnets. This

loss is more significant in electron/positron storage rings due to the smaller rest mass. The largest electron/positron circular accelerator ever built is the Large Electron and Positron collider (LEP) at CERN, which has a circumference of 27km, with particle energy loss per turn close to 3% of its 100 GeV beam energy. This requires a very expensive and powerful RF system. If a 500GeV electron storage ring is going to be built with a similar bending magnet field, the particle energy loss per turn will be about the same as the beam energy, and the circumference of the storage ring will be more than 100km. Storage rings are also very sensitive to beam disturbances. The maximum luminosity in the storage ring colliders is often limited by beam-beam interactions. The field-beam interaction in an FEL may also lead to serious instability of the charged particle beams in the storage rings. These facts suggest that both the e^--e^+ collider following LEP and future FELs should use linear accelerators.

1.2 FUTURE HIGH ENERGY LINEAR COLLIDERS

The Stanford Linear Collider (SLC) is currently the largest linear accelerator in the world. The two mile linear accelerator has produced 50GeV beams for both electrons and positrons.

Since the late 1980s, the need for next generation energy-frontier electron-positron linear colliders has been discussed, with the center of mass (CMS) energy at 0.5-1.5TeV and beyond. Several R&D programs have been carried out worldwide to explore different accelerator schemes. The designs can be summarized as 3 major design approaches.

One approach is similar to SLC, using klystrons to provide RF power to the normal conducting accelerating structures. This approach is represented by the Next Linear Collider (NLC) [1]. Figure 1 shows the schematic layout of NLC.

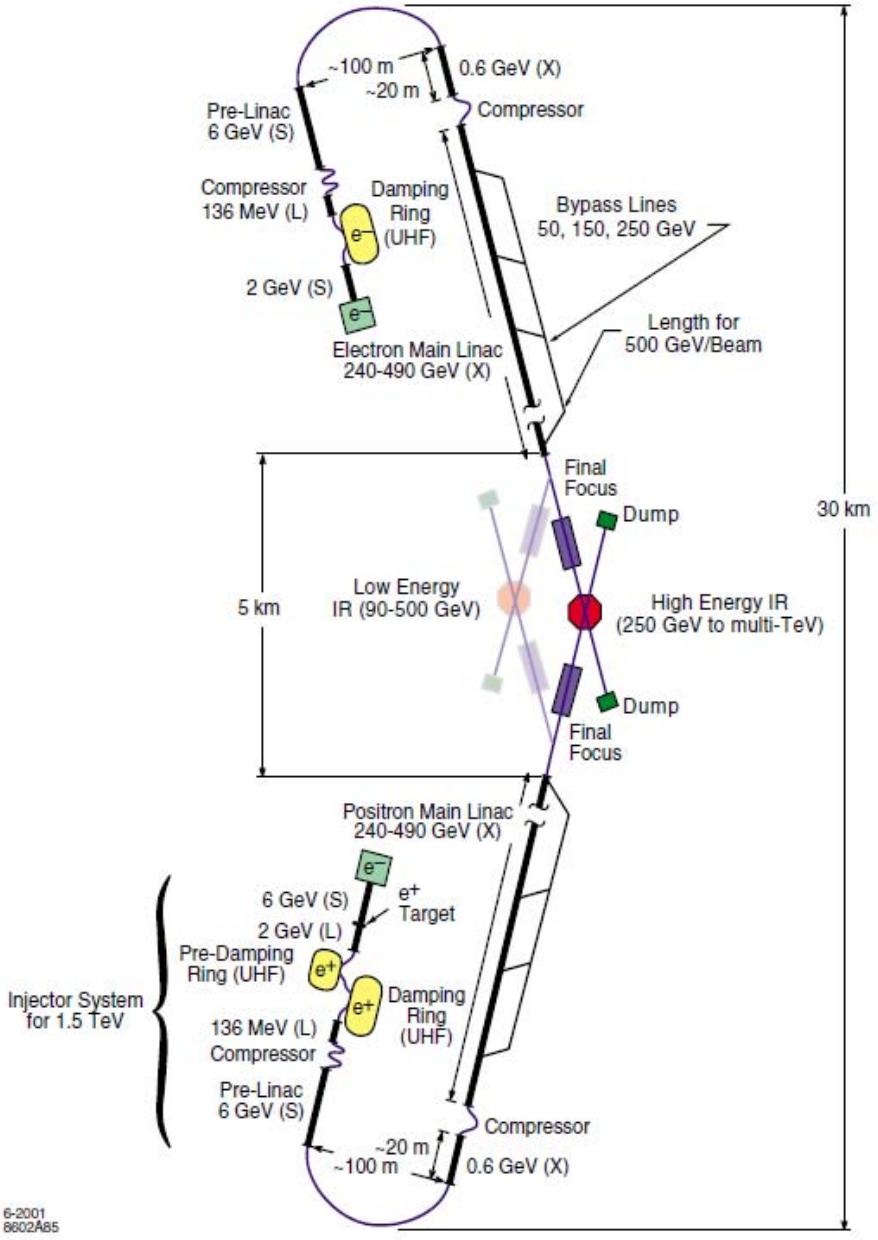

Figure 1. Schematic layout of NLC

One of the major challenges for the NLC type design is that it requires a very high peak-power pulsed RF source to obtain the high accelerating field. For a given accelerating

gradient, both the peak power and the average power depend on the RF fill time, which is the time required for the accelerating field to build up in the structures. Shorter fill time is desired since it can reduce the wall loss in the structure and lower the required average power. However, a short fill time will require a higher peak power. For example, with a fill time of about 100ns, it requires about 100MW peak RF power per meter of the accelerator structure for the 500GeV NLC design to build up the accelerating gradient of 65MV/m. With about 2□5km total structure length, almost 1TW of total peak RF power is needed. The desired RF pulse width is ~400ns, which is much shorter than the optimum output pulse width of the microwave tubes. A pulse compression system is then required to match the pulse width of the RF source and load, so that the total number of klystrons can be reduced and the total RF efficiency of the system can be enhanced to an acceptable level. In the 500GeV NLC design, with the use of a Delay Line Distribution System (DLDS), the 3.2μs pulse from eight 75MW klystrons will be combined into a 510MW pulse, then split into 8 pulses of about 400ns and fed into different structures, with an efficiency of approximately 85%. Approximately 1872 klystrons with 75MW peak power are required, a significant reduction in total peak klystron power compared to the case that the structures are directly fed by klystrons with 400ns pulse width.

The 2nd approach uses superconducting accelerating structures, which was represented by the ILC (International Linear Collider) design [2]. The superconducting design eliminates the need for the ultra-short RF pulse, because the loss in the superconducting structure is so low that longer filling time is allowed. In the ILC 500GeV design, the fill time of the structure is ~500μs, and the RF pulse width is ~1.5ms. The total peak power in the structures is about 6GW, a factor of more than 100 reduction compared to normal conducting structures. Only about 600 klystrons with 10MW peak power each will be used. The repetition rate of the RF pulses is also reduced dramatically from more than 100Hz to 5Hz, which can reduce the RF energy needed to fill the structures at the beginning of each pulse. With the superconducting structure, it is possible to yield a higher RF to beam power efficiency, due to the low wall loss in the structures.

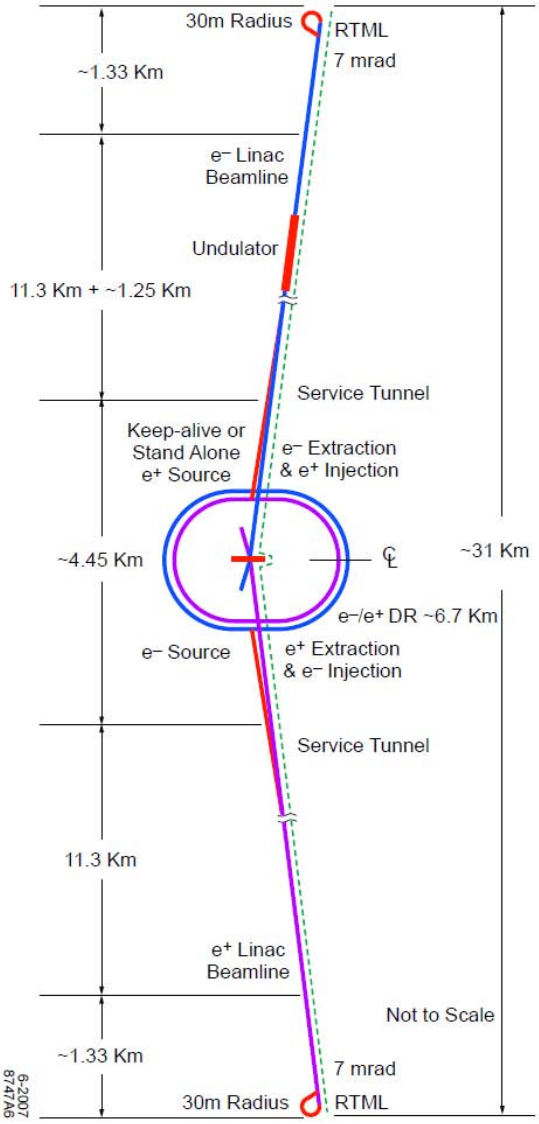

Figure 2. Schematic layout of ILC

In August 2004, the International Technology Recommendation Panel (ITRP) recommended that the International Linear Collider (ILC) should be based on the 1.3 GHz superconducting RF technology. Nonetheless, using current technology, the optimum accelerating gradient in superconducting structures is still far lower than normal conducting structures. To reach a certain goal of beam energy, the length of the

accelerator has to be longer. In the current 500GeV design, the accelerating gradient is 31.5MV/m, which is lower than in the normal conducting structures, and the total active length of the linacs is around 2□10km. The structures operate at 1.8-2 Kelvin, which requires a powerful cryogenic system.

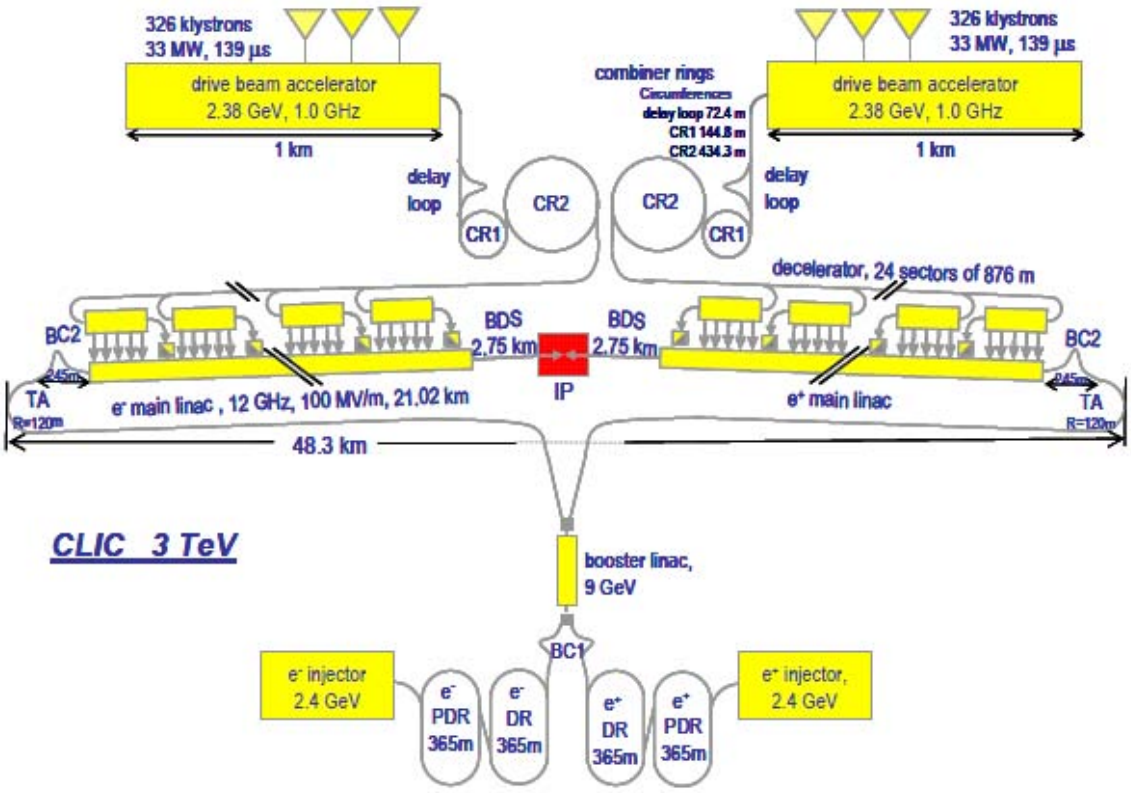

Figure 3. Schematic layout of CLIC

The CLIC (Compact Linear Collider) [3] of CERN represents the 3rd approach, which employs the two beam acceleration concept. A drive beam is generated efficiently in the drive beam accelerator with a long pulse length of about 140μs, and then compressed in the storage rings to a shorter pulse of several microseconds. The beam is transported to the decelerators parallel to the main linacs and split into ~240ns pulses for each sector of the decelerators. The short RF pulse is generated in the decelerator sectors from the drive

beam and fed into the accelerating structures in the main linacs. The two beam scheme is expected to achieve the high gradient of 100-150MV/m with a simple tunnel layout. The CLIC is the candidate for the future e^--e^+ colliders beyond 1 TeV, and has the potential to enhance the CMS energy to 5TeV.

	NLC [1]	ILC [2]	CLIC-G [3, 4]
CMS Energy	500 GeV	500 GeV	3 TeV
Possible Energy Upgrade	1-1.5 TeV	1 TeV	5 TeV
Luminosity($10^{34}cm^{-2}s^{-1}$)	2	2	1.22
Repetition Rate(Hz)	120	5	50
Particles per Bunch(10^{10})	0.75	2	0.372
Bunches per Pulse	190	2625	312
Bunch Separation (ns)	1.4	369	0.50
RF Frequency(GHz)	11.424	1.3	12
Loaded Gradient (MV/m)	55	31.5	>100
Fill Time	104ns	596μs	62.9ns
RF Pulse Length	396ns	1.565ms	240.8ns
Klystron Peak Power (MW)	75	10	33 (999.5MHz)
Klystron Pulse Length	3.168μs	1.565ms	139μs
Number of Klystrons	~1872	560	652
Active Two Linac Length(km)	~12	~20	NA
Beam Power (MW)	2□6.6	2□10.8	NA
Linac AC Power (MW)	~132	149.3	NA

Table 1. Major beam and RF parameters of different types of linear accelerators

Table 1 gives a comparison of the design parameters of the 3 types of linear collider designs. Since the designs are not final, there may be other versions of parameters.

1.3 RF PULSE COMPRESSION SYSTEMS

As mentioned in the previous section, RF load such as the high gradient accelerator structure requires high power sub-microsecond input pulses at the multi-megawatt level. At this power level, it is a huge waste to feed a much longer than needed pulse into the load. Neither it is economical to build and operate a high power RF source such as a klystron with the output pulse width reduced to sub-microsecond level. When a certain klystron is being operated at such a short pulse width, the peak output does not increase significantly as the pulse width shrinks, and the RF power in one pulse is much lower compared to a longer pulse of several microseconds [5]. The efficiency of such a system will also be very low, since the switching time of the modulator is at the level of several hundred nanoseconds and the loss during the switching is huge. A better alternative is to use klystrons with reasonable output pulse width and employ a pulse compression system to match the longer output pulse of the RF source to the shorter input pulse for the load, resulting to higher efficiency and lower cost for the whole system, even if the compression system has some losses and cost itself.

There are also some possible applications for the pulse compression systems other than linear accelerator structures, as long as the sub-microsecond multi-megawatt RF pulse is needed. An example of such applications is the RF undulator for synchrotron radiation light sources or FELs, which can provide more freedom to control the undulator wavelength, polarization, and field compared to magnetic undulators [6].

High power RF pulse compression systems and their application to RF accelerator systems were first introduced by Z. Farkas and P. Wilson through the invention of the SLED (SLAC Energy Doubler) pulse compression system in the 1970’s [7]. The application of SLED almost doubled the energy of the SLC without adding extra expensive klystrons. However, this system produces a non-flat RF output and is not suitable to accelerate the long bunch trains.

In the R&D of NLC type colliders, RF pulse compression was researched extensively during the last two decades. These collider designs are based on multi-bunch collision to achieve higher luminosity, which in turn need an RF system that can produce a flat top RF pulse. One such system is the Binary Pulse Compression system (BPC) invented by Farkas [8]. This system can produce flat top output pulses at extremely high efficiency, namely 100% for lossless systems. Nonetheless, it contains a cumbersome assembly of overmoded waveguides, which act as low-loss delay lines. Due to the cost and the space required for the delay lines, BPC is not a practical choice.

To make the system more compact, resonant delay pulse compression system was invented by Wilson et al [9] and Fiebig et al [10] independently. The Wilson version is also referred to as SLED-II. This system is much more compact than the BPC system, but it suffers from a reduced intrinsic efficiency. The efficiency of a SLED-II type system deteriorates very fast with high compression ratios and it has a theoretical maximum power gain of 9 for lossless systems.[1] A 150ns pulse with about 470MW peak power has been produced at SLAC from two 50MW klystrons with a compression ratio of 8 [11].

To improve the efficiency of the resonant delay line pulse compression systems with a higher compression ratio, the active pulse compression system using a switchable iris have been suggested [12]. The theory of the active resonant delay line pulse compression was also introduced in [12]. There is no intrinsic limit on power gain for the active system, and the intrinsic efficiency will be kept close to 81.5% with a very high compression ratio. Such a system was demonstrated with a silicon switch excited by a high power laser [13], achieving an 11 times power gain with a compression ratio of 32.

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[1] For an RF pulse compression system, the compression ratio is defined as the ratio between the input pulse width and the output pulse width; the compression power gain (sometimes also referred as power gain) is defined as the ratio between the power of the output pulse and the input pulse.

The delay line distribution system (DLDS) was introduced by Mizuno and Otake in 1994 [14]. This system can divide a long pulse generated by klystrons into several short pulses with high efficiency like that in the BPC, but then are never combined again. The total length of delay lines can be reduced compared to the BPC, since part of the delay time is provided by the particle beam itself. In the NLC design, DLDS was adopted as an upgrade scheme for pulse compression and power distribution. However, the total length of the delay lines scales as the square of compression ratio and is still much longer than SLED-II. The cost and space requirement is still a challenge for the DLDS.

To reduce the total delay line length of the DLDS further, active DLDS was proposed by Tantawi et al [15]. It consists of one single-moded delay line parallel to the beam and uses Single Pole Double Throw (SPDT) switches to extract slices of short pulses to each section of the load. The intrinsic efficiency remains at 100%. The synthesis of the SPDT switches was introduced in [16]. Another DLDS scheme, namely the multi-mode DLDS, can also delivery 100% intrinsic efficiency with only one delay line parallel to the accelerator structures [17]. However, the multi-mode DLDS needs some very complicated mode-launchers and mode-extractors.

Theoretically, both the active DLDS and the active resonant delay line compression system have shown advantages over their passive counterparts. With the active switching element, the active system can achieve higher efficiency at high compression ratio while keeping a compact and low cost design.

1.4 HIGH POWER RF SWITCHES

In the previous sections, we have addressed the need of an RF switch for the active RF pulse compression system. This switch needs to be able to handle a very high level of RF power, a value desired to be 100MW or more. The switching time needs to be a fraction of the desired output pulse width. For NLC, the output pulse width is about 400ns, so the desired switching time should be 100ns or less.

There are several types of commercially available microwave switches widely used in the industry. Discrete component PIN diodes have a history of more than half a century and are commonly used as RF switches. The switching time for a discrete PIN diode can be as short as several nanoseconds and the RF power handling capacity can be up to 100 watt CW or several hundred watt peak. Ferrite waveguide switches are popular for applications at higher power levels, i.e., several megawatts peak power at S-Band. Switching is realized by applying magnetic field to change the permeability of the ferromagnetic material. A lot of energy is required to build the strong magnetic field in a large space, especially when the power handling capacity is high. Thus the switching speed is generally slow. Usually the switching time is several milliseconds with several megawatts of power handling capacity. Another high power switch is the mechanical switch, which performs switching by moving some metal parts in the waveguide. Although mechanical switches can have even higher power handling capacity, their switching time will increase as the power handling capacity and the size of the components grow. Typically it needs several hundred ms with several megawatts of peak power. In the recent years, with the boom in micro-fabrication technology, RF MEMS (Micro Electromechanical System) switches have gained significant interest for wireless communication applications. Usually MEMS switches have similar power handling capacity compared to PIN diodes, and slow switching time of around 1ms. Compared to the PIN diodes, the major advantages of the MEMS switches are the better isolation between channels and lower power consumption. Obviously, none of these commercial available switches can meet both the power and speed requirements for active pulse compression.

In recent years, several high power switching elements are under development for the high power active pulse compression applications. Among them are plasma [21], ferromagnetic [19], ferroelectric [20], and semiconductor switches [22, 25, 26].

The early research on plasma switch can be traced back to the 1970's by Birx [18]. In such a switch, conducting plasma can be generated by arcing in either a vacuum or gas ambience and the RF transmission in the waveguide can be changed. Plasma switches are ideal in terms of speed and power handling capacity, but the system typically requires a driver with 100KV voltage.

In the ferroelectric switches, the dielectric permittivity of the ferroelectric material is controlled by the electric field, thus the switching is achieved. For the low loss ferrite materials which have been investigated, a high field is necessary to perform switching. Given the large size of the component required to handle multi-megawatt RF power, a typical ferroelectric switch needs 100KV biasing voltage.

The ferromagnetic switch uses similar switching mechanism as commercial ferrite switches, changing the permeability of the material by switching the magnetic field. Due to the difficulty to limit the magnetic field inside the ferrite, the ferromagnetic switch typically needs tens of Joules of energy to form the switching magnetic field, which demands enormous power for fast switching.

In the 1960's, the idea of waveguide semiconductor window switch based on bulk effects in the semiconductor was suggested, and several switches were developed [25, 26]. The window switch comprises a high resistivity silicon wafer integrated with a set of PIN diodes. When the switch is inserted into the waveguide, the PIN diodes can inject carriers into the bulk silicon to form the conductive plasma and switch the RF reflectivity. Such a switch was developed in rectangular waveguides, and was tested up to 100kW power level at X-band. The power level is mainly limited by the choke structure, which is employed to avoid the RF leakage at the gap where the window switch is inserted.

An optical semiconductor switch was also demonstrated by Tantawi in 1997 [13]. This switch is based on the excitation of electron-hole plasma on the surface of a semiconductor using a laser pulse. This switch window operates under the TE_{01} mode in

a circular waveguide. This mode has no radial electric field and no azimuthal magnetic field; hence, a small gap in the waveguide will not lead to RF leakage without the choke structure.

Although the optical switch can be very fast, it requires a very expensive high power laser system. To eliminate the laser from the system described in [13], Tamura and Tantawi designed a switch using PIN diode junctions to inject the carriers into the bulk of a semiconductor wafer [22], still operating under the TE_{01} mode in a circular waveguide. The switch was able to handle multi-megawatts of RF power. However, the device described in [22] demonstrated only the possibility of the use of such technology with ultra-high power microwave systems. This device was too slow for pulse compression application and had high losses.

The research described in this thesis is focused on the development of the semiconductor based high power RF switches for active pulse compression applications. An electrically controlled silicon window has been built and characterized. This switch is based on injecting the carrier at the surface of a silicon wafer using an array of PIN surface diodes, but with significant improvement in speed and loss compared to Tamura's switch, achieving 2-300ns switching time. Such a switch is expected to handle tens of megawatts. A switch module was also developed to match the coupling coefficients of the active window to the requirement of the pulse compression systems. Active pulse compression under low power has been demonstrated with such a switch, obtaining almost 8 times power gain from a compression ratio of 20.

The switch and the pulse compression system presented in this dissertation may have other applications beyond the NLC type high gradient accelerators. For example, the compression system can be used for other systems requiring the sub-microsecond multi-megawatts pulse, such as an RF undulator in FEL applications.

1.5 OUTLINE OF THIS THESIS

In this thesis, we will discuss the development of the high power RF switches based on bulk effects in semiconductors and its application to high power RF pulse compression systems.

The thesis outlines as the following:

In Chapter 2, the mechanism of different types of RF pulse compression will be discussed. The theories for the passive and active resonant delay line pulse compression systems will be revisited and redeveloped. The requirements of the switch will be provided.

In Chapter 3, we will introduce the high power active element module containing an active window and a Tee, which can provide tunable coupling coefficients. The factors determining the performance of the module will be discussed. We will also give the design detail of the circular waveguide Tee.

Chapter 4 will discuss the synthesis of the switch system with multiple active elements. Such systems can combine the power handling capacity of several active elements to meet the power requirement of close to Gigawatt level.

Chapter 5 will provide the theory, design and process for the active window. We will focus on the electrically controlled active window. Other options such as an optical controlled window will also be discussed.

In Chapter 6, the low power characterization test of the switch is discussed, and the results are given. The test includes cold network analyzer measurements and the active switching test, with both the window and the module. The results of the low power active pulse compression experiments will also be presented.

In the last chapter, we will give a summary of the thesis. Suggestion for future work will be also discussed.

CHAPTER 2: RF PULSE COMPRESSION SYSTEMS

In the previous chapter, we have briefly reviewed the history of RF pulse compression systems. This chapter will compare the mechanisms and theories of different systems, with the focus on the passive and active resonant delay line systems.

2.1 OPERATION MECHANISMS OF THE MAJOR TYPES OF RF PULSE COMPRESSION SYSTEMS

SLED

SLED is the first high power RF compression system with application to particle accelerators. The SLED system uses overcoupled RF cavities to store RF energy provided by a klystron. The cavities are charged and the amplitude of the emitted wave from the cavity will increase. The radiated wave from the cavities is the combination of the emitted wave and the reflected wave. When the charging saturates, the radiated wave will have the same amplitude as the input from the klystron; thus the emitted wave can have a maximum of twice the amplitude of the input, if the reflected wave has same amplitude as the input and opposite phase as that of the emitted wave. By turning the klystron input off, the radiated power will have the same amplitude as the emitted wave, and a maximum of 4 times the value of the input power. To enhance the power gain further, the klystron input can be kept on during the discharging phase but with a reversed phase, so the reflected wave can add to the amplitude of the emitted wave to as much as 3 times that of the input, and the power gain can achieve a theoretical maximum of 9. However, the output amplitude decreases exponentially during the discharging period as the stored energy dissipates. This produces a non-flat output which is only suitable for the acceleration of short bunch trains, and the effective peak output power gain is lower than the theoretical value of 9.

The actual SLED system uses a microwave network, usually a 3db coupler, to redirect the microwave radiated from the cavities to the external load, usually the accelerator structures. Given the limited input pulse width and losses, the system has close to a 4 times power gain; this almost doubled the accelerating gradient and the beam energy of SLC without adding more klystrons. Figure 4 shows the schematic drawing of the RF network of the SLED type pulse compression system. When the storage cavities are replaced with resonant delay lines, it becomes the SLED-II system, which will be discussed later in this chapter.

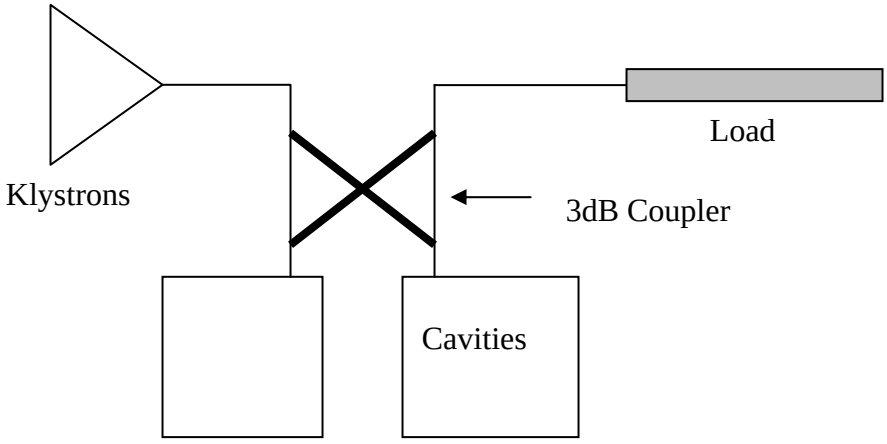


Figure 4. RF Network of a SLED type Pulse Compression System

BPC

The Binary Pulse Compression system (BPC) was introduced in the 1980's. This system was designed to produce flat RF output pulses with very high efficiency.

The operation principle of a two stage BPC system is illustrated in Figure 5. The compression ratio of such a system is 4 (the compression ratio for an *n* stage system is $N = 2^n$). The system is driven by two independently controlled klystrons. The output is divided into 4 time bins, with a different phase in each time bin. The two pulses are combined in the 3dB hybrid "H1". When the two input pulses have the same phase, the output goes to port 3 of the hybrid; the output goes to port 4 when the input phases are

opposite. The first half of the output pulse (coming from port 3 of H1) is guided through a delay line “D1”. The delay time of D1 is same as the pulse width, so the two pulses can be synchronized. The first stage of the compression is then accomplished, with the RF pulse width cut in half. The compression stage can be repeated, with 2^n times of power gain after *n* stages. After the last stage, the two synchronized pulses can also be combined with a combiner.

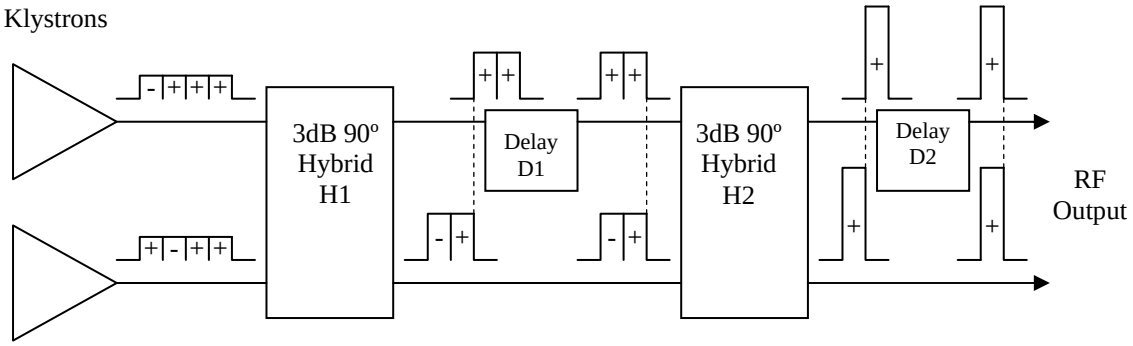


Figure 5. Operation scheme of a 2 stage BPC system

The intrinsic efficiency of BPC is 100% with lossless delay lines. However, the BPC requires very long delay lines, especially when the compression ratio is high. The length of the delay line in the first stage is

$$L_{\max} = 2^{n-1} T_p v_g \tag{2.1}$$

And the total length of the delay lines in all the stages is

$$L_{total} = (2^n - 1) T_p v_g \tag{2.2}$$

where T_p is the pulse width of the compressed output, and v_g is the group velocity of the microwave in the delay lines.

In the case that only the loss in the delay lines is considered, the power gain of the system can be written as:

$$G_{power} = \frac{(1+p^{2^{n-1}})^2}{2}\frac{(1+p^{2^{n-2}})^2}{2}.....\frac{(1+p)^2}{2} \qquad (2.3)$$

or

$$G_{power} = \left(\frac{1-p^{2^n}}{1-p}\right)^2 \Big/ 2^n = \left(\frac{1-p^N}{1-p}\right)^2 \Big/ N \qquad (2.4)$$

$p = e^{-j\beta l}$, which is related to the single trip loss in the delay line with delay time of T_p and length *l*. In the case where the delay line with length T_p has the single trip loss of 4% and the system has 3 stages, the power gain is 6.95. The gain of the actual system is even lower due to the losses in the hybrid etc.

DLDS

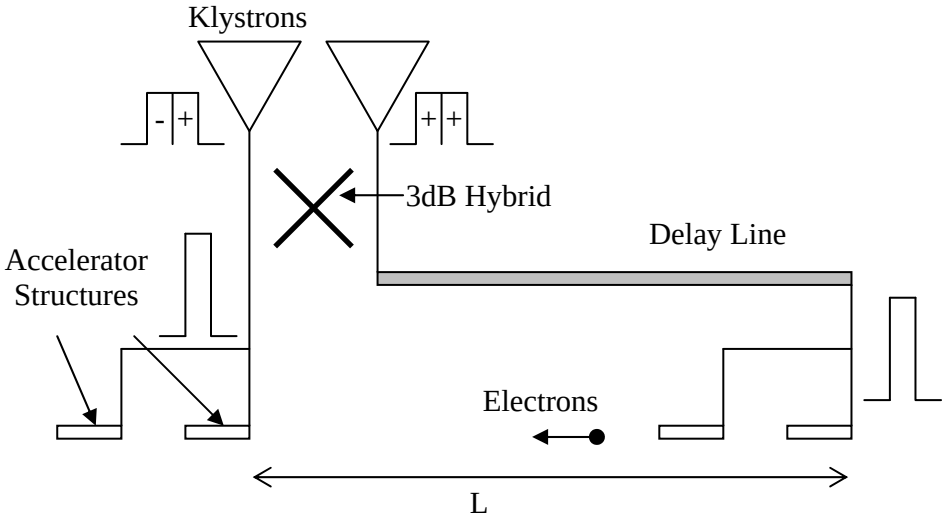


Figure 6. Operation scheme of the DLDS

The delay line distribution system (DLDS) utilizes a similar principle as that of BPC, dividing a long pulse into short slices. But unlike the BPC, the short output pulses are synchronized with the delay from the particle beam in the structure and the delay in the

waveguide transmitting RF to the load. The beam will provide approximately half of the delay time, so the delay time in the waveguides can be reduced.

A DLDS with compression ratio of 2 is shown in Figure 6. Through a 3dB hybrid, the output of two independently controlled klystrons is combined in power, but split into two short slices in time and redirected into two ports. The earlier pulse will travel through a delay line of L and be fed into the upstream accelerator structures, and the following pulse will be fed directly into downstream structures. The two pulses will be synchronized with the beam if the pulse width equals the sum of the delay time in the delay line and the beam travel time from the upstream structures to the downstream structures.

$$T_p = T_d + T_b = L/v_g + L/v_b \tag{2.5}$$

where v_b is the velocity of the beam. Usually v_b is very close to the velocity of light c for high energy beams, and v_g is also of the same order as c.

For a system with compression ratio 2^n, a hybrid network will combine the output of 2^n independently controlled klystrons in power, but split the output into 2^n short pulses in time. The pulses will be fed into 2^n groups of accelerator structures. A schematic view of a factor-4 DLDS is shown in Figure 7. The length of the longest delay line is

$$L_{\max} = \frac{(2^n - 1)T_p}{1/v_g + 1/v_b} \tag{2.6}$$

and the total length of the delay lines for a system with 2^n loads is

$$L_{total} = \frac{2^{n-1}(2^n - 1)T_p}{1/v_g + 1/v_b} \tag{2.7}$$

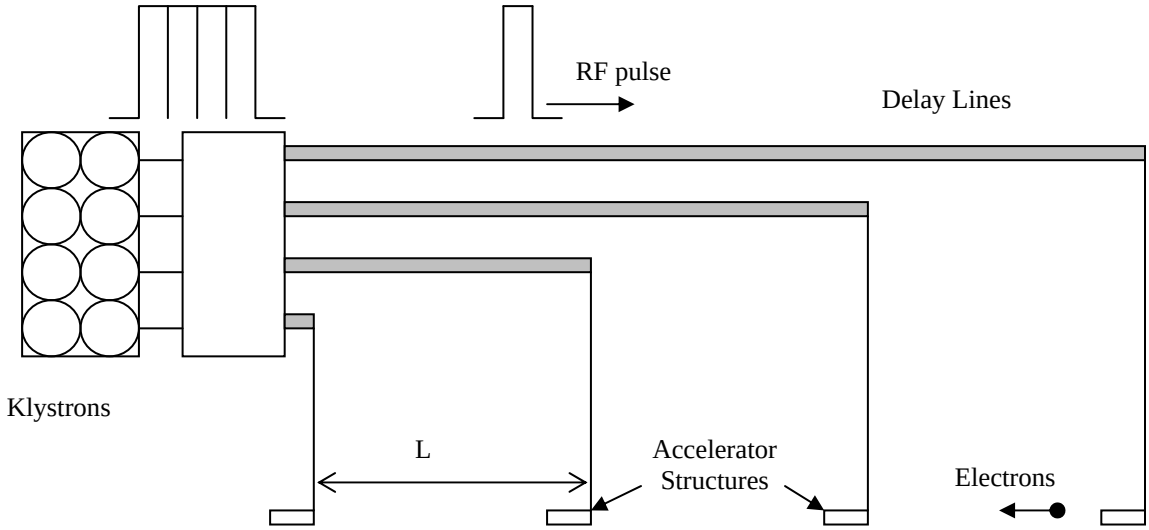


Figure 7. Schematic view of a 4/4 DLDS

The intrinsic efficiency of the DLDS is 100%, the same as that of BPC. The losses in the delay lines vary between the loads, since the lengths of the delay lines are different. For actual systems with the same compression ratio, the longest delay line in DLDS is shorter than the total length of the delay lines in BPC, so the efficiency in DLDS should be higher.

In the NLC design, the DLDS has been adopted as the upgrade scheme for RF pulse compression and distribution. However, DLDS is only suitable for linear accelerator applications, in which the beam can provide the delay, and there are a big number of loads. It is not efficient for applications with only one load demanding short pulsed power.

ACTIVE DLDS

Although the DLDS needs shorter delay lines compared to BPC, it still needs several delay lines in parallel. To host the low loss delay lines with large diameters, the cross section of the linear collider tunnel has to be increased, adding the construction cost. To make the system more compact, active DLDS was then proposed, in which only one

delay line is needed. Figure 8 shows the schematic view of an active DLDS with compression ratio of 4.

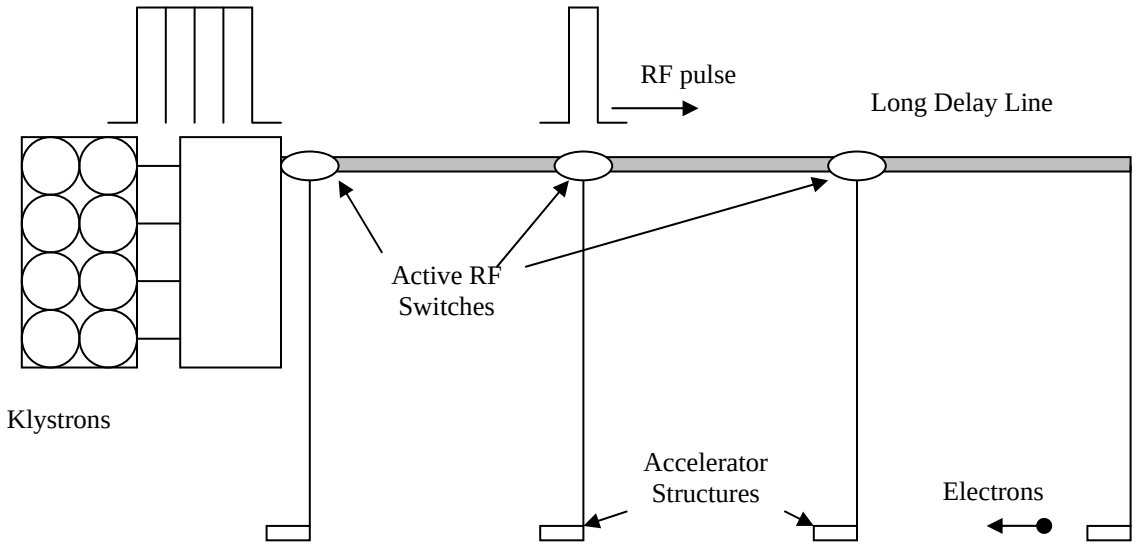


Figure 8. Operation scheme of an active DLDS

In an active DLDS, a long pulse is fed into a delay line in the direction of the upstream accelerator structures. The power of the long pulse can come from either one single klystron or from the combination of several klystrons. There will be active RF switches along the delay line. The switch will be a Single Pole Double Throw (SPDT) switch. When the trigger of the switch stays off, the RF will go forward along the delay line; when the switch is triggered on, the RF will be directed to the 3rd port of the switch and fed into the load connected to the switch.

The intrinsic efficiency of the active DLDS is 100%, the same as that of the passive DLDS. In the actual system, the major losses come from the delay lines and the switches. The loss over the switches will be compounded as the RF pulse traveling through several switches. As a result, the switches must have a very low insertion loss, especially for the switching state where RF goes through the switch along the delay line.

SLED-II: RESONANT DELAY LINE PULSE COMPRESSION SYSTEMS

Another compact pulse compression system with flat pulse output is the resonant delay line pulse compression system, which was invented by Wilson et al [9] and Fiebig et al [10] independently. The Wilson design is also referred to as SLED-II. Such a system uses a similar principle as the SLED system does, but replaces the RF cavities in SLED with resonant delay lines as the energy storage device, so the output pulse can be flat and the efficiency is enhanced. This system is much more compact than the BPC system. The system only requires a delay line with length of $T_p / 2$, regardless of the compression ratio. However, the intrinsic efficiency of resonant delay lines deteriorates very fast when compression ratios increase, and the theoretical power gain for lossless systems is limited to a maximum of 9. A 400ns pulse with about 470MW peak power has been produced from two 50MW klystrons with a compression ratio of 8 at SLAC [11].

To improve the efficiency of the resonant delay pulse compression system, active pulse compression systems have been suggested and demonstrated [12]. In such a system, active irises are used between the input and the delay lines so the coupling coefficients can be optimized separately for the charging and discharging phase. The limit on the maximum power gain is lifted. The system has an intrinsic efficiency of more than 80% regardless of the compression ratio.

The following section will provide the theories for both passive and active resonant delay pulse compression systems.

2.2 THEORY OF PASSIVE PULSE COMPRESSION SYSTEMS USING RESONANT DELAY LINES

In this section, we will discuss the theory of the single event switched pulse compression system using resonant delay lines, and compare it with the passive pulse compression system.

Figure 9. A resonant delay line

Consider a waveguide delay line with a coupling iris shown in Figure 9. The iris is reciprocal and lossless, hence the scattering matrix is unitary and symmetric. With the proper choice of reference planes, the scattering matrix can be written in the following form:

$$S = \begin{pmatrix} -R_0 & -j\sqrt{1-R_0^2} \\ -j\sqrt{1-R_0^2} & -R_0 \end{pmatrix} \tag{2.8}$$

R_0 is the reflection coefficient of the iris. When the iris is lossy, the general form of the S-matrix is

$$S = \begin{pmatrix} -R_0 q_1^2 & -j\sqrt{1-R_0^2}\, q_1 q_2 \\ -j\sqrt{1-R_0^2}\, q_1 q_2 & -R_0 q_2^2 \end{pmatrix} \tag{2.9}$$

For an iris with two symmetric ports, the S-matrix reduces to

$$S_0 = \begin{pmatrix} -R_0 q_0 & -j\sqrt{1-R_0^2}\, q_0 \\ -j\sqrt{1-R_0^2}\, q_0 & -R_0 q_0 \end{pmatrix}$$

in which q_0^2 represents the power loss in the iris. The forward and reflected fields around the iris are related as:

$$V_1^- = -R_0 q_0 V_1^+ - j\sqrt{1-R_0^2}\, q_0 V_2^+ \tag{2.10}$$

$$V_2^- = -j\sqrt{1-R_0^2}\, q_0 V_1^+ - R_0 q_0 V_2^+ \tag{2.11}$$

With the exception of some phase change, the incoming signal V_2^+ at time instant t is the same as the outgoing signal V_2^- at time instant $t - \tau$; where τ is obviously the round trip delay through the line; i.e.

$$V_2^+(t) = V_2^-(t-\tau)e^{-j2\beta l}. \tag{2.12}$$

where β is the wave propagation constant within the delay line, and l is the length of the line. Substituting from Eq. (2.12) into Eq. (2.11), we get a difference equation that governs the system. During the charging phase we assume a constant input V_{in}. If the delay line has small losses (i.e., β has a small imaginary part), at resonance the term $e^{-j2\beta l} = -p$, where p is a positive real number close to 1.

$$V_2^-(t) = -j\sqrt{1-R_0^2}\,q_0 V_1^+(t) + R_0 q_0 V_2^-(t-\tau)\,p \tag{2.13}$$

We assume that all the voltages are equal to zero at time $t < 0$, and $V_1^+ = V_{in}$ during the time interval $0 \le t < (n-1)\tau$. So in the ith time interval $(i-1)\tau \le t < i\tau$ we have

$$\begin{aligned} V_2^-(i) &= -j\sqrt{1-R_0^2}\,q_0 V_{in} \sum_{k=0}^{i} (R_0 q_0 p)^k \\ &= -j\sqrt{1-R_0^2}\,q_0 V_{in}\,\frac{1-(R_0 q_0 p)^i}{1-R_0 q_0 p} \end{aligned} \tag{2.14}$$

$$V_2^+(i) = -pV_2^-(i) = j\sqrt{1-R_0^2}\,q_0 V_{in}\,\frac{1-(R_0 q_0 p)^i}{1-R_0 q_0 p}\,p \tag{2.15}$$

After the energy has been stored in the delay line, one may dump part of the energy in a time interval τ by flipping the phase (changing it suddenly by π) of the incoming signal just after a time interval $(n-1)\tau$. The output pulse level during the nth time interval $(n-1)\tau \le t < n\tau$ is

$$V_{out} = V_1^-(n-1) = V_{in}\left[R_0 + (1-R_0^2)q_0^2\,\frac{1-(R_0 q_0 p)^{n-1}}{1-R_0 q_0 p}\,p\right] \tag{2.16}$$

n is also called the compression ratio, which is the ratio between the length of the input pulse and output. The maximum power gain is limited. Using Eq. (2.15), the maximum power gain as $n\to\infty$ is,

$$G_{\max} = \left(\frac{3 - \sqrt{8(1 - p^2 q_0^2)}}{p} \right)^2 \tag{2.17}$$

which occurs with a reflection coefficient:

$$R_0 = \frac{1 - \sqrt{\frac{1}{2}(1 - p^2 q_0^2)}}{p q_0}$$

For a typical passive iris made of metal, the loss in the iris can be neglected i.e., $q_0 = 1$, and the output amplitude can be expressed as

$$V_{out} = V_1^-(n-1) = V_{in}\left[R_0 + (1 - R_0^2)\frac{1 - (R_0 p)^{n-1}}{1 - R_0 p}\, p \right]. \tag{2.18}$$

And the maximum power gain reduces to

$$G_{\max} = \frac{17}{p^2} - 8 - \frac{12\sqrt{2(1 - p^2)}}{p^2} \tag{2.19}$$

which occurs at $R_0 = \dfrac{1 - \sqrt{\frac{1}{2}(1 - p^2)}}{p}$. The maximum power gain is limited to 9 as $p\to 1$. Furthermore, this maximum is greatly affected by the losses in the delay line; for example, the gain is limited to 7.46 if the line has 1% round trip power losses. With limited input pulse length, the gain will be even worse. The losses at the iris will also reduce the power gain.

The low intrinsic gain of the passive resonant delay line pulse compression system comes from two types of losses: 1) During the charging phase, a big portion of the input is emitted and cannot enter the delay line. 2) In the discharging phase, the energy stored in

the delay line cannot be fully discharged in one time interval. The power wasted in both of the scenarios become more significant with higher compression ratio. The losses can be reduced significantly if active elements are used in the system.

2.3 THEORY OF ACTIVE PULSE COMPRESSION SYSTEMS USING RESONANT DELAY LINES

Ideally, if a lossless continuously variable iris could be used in a resonant delay line pulse compression system, both the RF emission during the charging phase and the incomplete discharging can be eliminated by setting the coefficients of the iris to certain value during each of the time intervals. The intrinsic efficiency of such a system is 100% and has no limit on maximum power gain. However, such an iris is not practical to build, if even possible.

A more practical approach to enhance the efficiency of the resonant delay line compression system is to switch the iris just one time and fully discharge the delay line. To discharge the line, one can keep the input signal at a constant level during the time interval $0 \le t < n\tau$ and switch the iris reflection coefficient R_d to zero at $n\tau$, so that all the energy stored in the line is dumped out. The S-matrix of the iris during the discharging is

$$S_d = \begin{pmatrix} -R_d q_d & -j\sqrt{1-R_d^2}\, q_d \\ -j\sqrt{1-R_d^2}\, q_d & -R_d q_d \end{pmatrix} \tag{2.20}$$

In this case,

$$V_{out} = \frac{1-(R_0 q_0 p)^n}{1-R_0 q_0 p}\sqrt{1-R_0^2}\, q_0 \sqrt{1-R_d^2}\, q_d\, p V_{in} \tag{2.21}$$

This is a very important application of an active pulse compression system since we do not require the change of the phase of the input pulse. It enables us to use this system with oscillator like sources, for example the magnetron.

To reduce the burden on the switch, one can reverse the phase together with changing the iris reflection coefficient at the beginning of the last time interval $(n-1)\tau \le t < n\tau$. In this case all the energy can still be extracted out of the line, but the iris reflection coefficient need not be completely reduced to zero. This reflection coefficient during the discharging phase R_d is greater than zero and the switch need only change the iris between R_0 and R_d. In this case the output reduces to

$$V_{out} = \left[R_d q_d + \sqrt{1-R_d^2}\, q_d \left(\frac{1-(R_0 q_0 p)^{n-1}}{1-R_0 q_0 p} \right) \sqrt{1-R_0^2}\, q_0 p \right] V_{in} \qquad (2.22)$$

or

$$V_{out} = \left(q_d \big/ R_d \right) V_{in} \qquad (2.23)$$

where the R_d required to completely discharge the line is given by

$$R_d = \cos\left[\tan^{-1}\left(\frac{1-(R_0 q_0 p)^{n-1}}{1-R_0 q_0 p} \right) \sqrt{1-R_0^2}\, q_0 p \right] \qquad (2.24)$$

The compressed output pulse takes place in the time interval $(n-1)\tau \le t < n\tau$. The optimal value of R_0 is such that it fills the system with a maximum possible amount of energy in the time interval $(n-1)\tau$. For a lossless active system with compression ratio of 8, the optimized value of the reflection coefficients will be $R_0 = 0.835$ and $R_d = 0.386$, if the input phase can be reversed during the last time bin. For a similar system without phase reversal, the coefficients will be $R_0 = 0.854$ and $R_d = 0$.

Unlike the passive systems, the maximum power gain has no intrinsic limit. It is only limited by the compression ratio *n* and the amount of loss in the system. For lossless systems with *n>12*, the compression efficiency is flat at 81.5%, which means that the power gain is 81.5% of *n*, even when the compression ratio goes to infinity. At higher compression ratio, the advantage of active compression is more obvious.

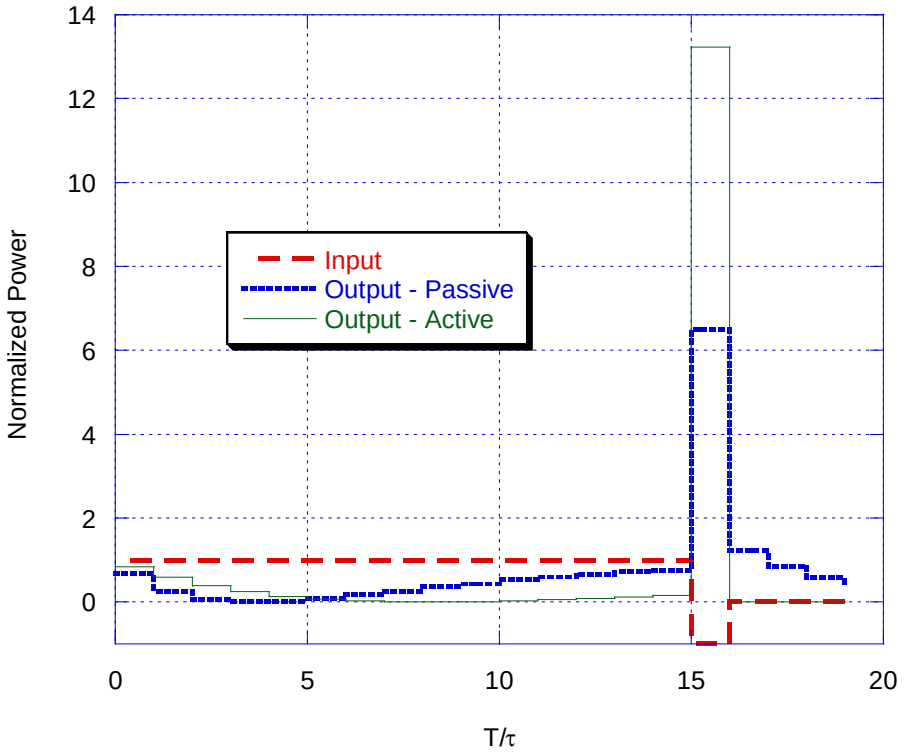


Figure 10. Comparison of the theoretical power gain of the lossless active and passive resonant delay line pulse compression systems, with the compression ratio of 16 and the input phase flip

When the compression ratio is high, the charging phase loss of the iris and the delay line round trip loss have a large impact on the power gain in the active system. The loss at the iris will accumulate during each round trip of the RF, while the loss during discharge is a one time effect. The losses determine the maximum power gain of the active compression

system as $n\to\infty$. For the active compression scheme with phase flipping during discharge, the maximum power gain is:

$$G_{\max} = q_d^2 \Big/ (1 - p^2 q_0^2) \tag{2.25}$$

which occurs when $R_0 = pq_0$. For the case without phase flipping, the maximum gain is

$$G_{\max} = q_d^2 \left(\frac{1}{1 - p^2 q_0^2} - 1\right) \tag{2.26}$$

Compression Ratio	Optimized power gain					
	SLED-II		Active resonant delay line compression system			
			switch and phase flip before last bin		switch after last bin, no phase flip	
	Intrinsic	With loss*	Intrinsic	With loss*	Intrinsic	With loss*
2	1.56	1.53	2	1.73	1.69	1.36
4	3.44	3.29	3.48	2.84	3.29	2.50
8	5.15	4.76	6.72	4.86	6.53	4.39
16	6.49	5.72	13.23	7.63	13.04	6.99
20	6.84	5.91	16.48	8.56	16.30	7.85
32	7.45	6.11	26.25	10.22	26.07	9.41
64	8.08	6.17	52.32	11.37	52.13	10.47
128	8.47	6.17	104.44	11.47	104.26	10.58

Table 2. Optimized power gain for passive and active pulse compression systems

*The loss in SLED-II is assumed as a 4% round trip loss in the delay line. The losses in active compression system are assumed as a 4% round trip loss in the delay line, a 4%

charging phase loss and a 10% discharging phase loss in the iris. These numbers are very close to what we actually obtained in our experiments, where the delay line has an approximately 375ns round trip time.

To take advantage of the active pulse compression system, the losses during the charging phase must be very low. Cutting the charging state losses will be more effective in enhancing the efficiency and gain of the system. Assume a 4% round trip loss for the delay line and the compression ratio of 20. Further assuming the switch has a 4% off (charging) state loss and a 10% on (discharging) state loss, the optimized gain for the active system with phase flipping will be 8.56 (efficiency of 42.8%), which is already close to the intrinsic limit of the passive system; for the active system without phase flipping, the gain will be 7.85. If the assumed losses at the iris are reversed, as 10% for the charging phase and 4% for the discharging, the optimized gain for an active system with phase flipping will decrease to 6.48, while it will be 5.59 for the system without phase flipping. For comparison, the passive system without the loss at the iris will give an optimized gain of 5.91 with phase flipping.

If both the delay line roundtrip losses and the charging state losses in the switch can be reduced to 1%, and the assumed discharging state loss is kept at 10%, the optimized power gain in the active system with phase flipping will be 12.79 for a compression ratio of 20 (efficiency of 64.0%), or 18.63 for a compression ratio of 32. For the SLED-II type delay line, the losses mainly come from the wall losses when the RF travels, and the losses are approximately proportion to the length of the delay line. If the roundtrip time can be reduced to about 100ns, the roundtrip loss can be close to 1%. In this case, the switch is also required to have a shorter switching time.

SUMMARY

In this chapter, we have discussed the operation principles of various RF compression systems. The following table gives a comparison of those systems. Both the active DLDS

and the active resonant delay compression system can provide a compact solution with high efficiency, which is impossible for their passive counterparts. Both of the active systems require an RF switch which can provide high power handling capacity, a fast switching time that is a fraction of the output pulse width, and very low insertion loss.

	Size	Intrinsic Efficiency	High Compression Gain
SLED-II	Compact	Low	Maximum = 9
BPC	Needs long delay line	100%	Difficult
DLDS	Needs long delay line	100%	Difficult
Active DLDS	Medium	100%	Possible
Active SLED-II	Compact	≥81.5%	Easy

Table 3. Comparison of RF pulse compression systems

CHAPTER 3: HIGH POWER MICROWAVE SWITCH ELEMENTS WITH SINGLE ACTIVE WINDOW

INTRODUCTION

In Chapter 2, we have addressed the need for high power RF switches for active RF pulse compression systems.

The active resonant delay-line pulse compression system requires a switchable iris with certain coupling coefficients at charging and discharging states respectively. The optimized coefficients are functions of many variables such as compression ratio, losses in the delay line and losses at the iris. So a tunable switch is needed. Even if the coupling coefficients are predetermined, in most cases it's not possible to build an active window with exactly the required coefficients. A tunable iris element was then designed to match the coupling coefficients of the active window to desirable values at both *on* and *off* states. In this thesis, the *on* state of a switch is the state that the active window is excited by external sources, and in most cases the window is close to fully reflective.

In this chapter, the design methodology of the high power RF switch element with one active window will be presented. Such an element is composed of a Tee junction with an active window and a movable short plane connected to the 3rd port, as shown in Figure 11. The coupling coefficients of the element are determined by the reflection phase in the 3rd arm. When the active window is turned on, it acts as a short plane and the phase of the reflected signal from the third-port changes. Hence, the coupling coefficients relating the remaining two ports are switched. These coefficients depend on the location of the active window, which determines the coupling in the *on* state, and the location of the movable short, which determines the coupling in the *off* state.

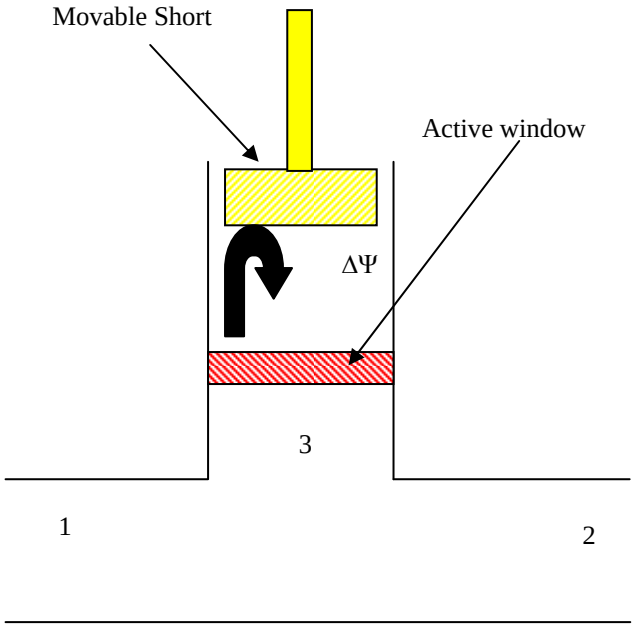


Figure 11. The active element

3.1 S-MATRIX OF THE SWITCH ELEMENT

For a lossless symmetric Tee junction, the S-matrix can be written in the form

$$S = \begin{pmatrix} \frac{e^{j\phi} - \cos\theta}{2} e^{j\alpha} & \frac{-e^{j\phi} - \cos\theta}{2} e^{j\alpha} & \frac{\sin\theta}{\sqrt{2}} e^{j\alpha/2} \\ \frac{-e^{j\phi} - \cos\theta}{2} e^{j\alpha} & \frac{e^{j\phi} - \cos\theta}{2} e^{j\alpha} & \frac{\sin\theta}{\sqrt{2}} e^{j\alpha/2} \\ \frac{\sin\theta}{\sqrt{2}} e^{j\alpha/2} & \frac{\sin\theta}{\sqrt{2}} e^{j\alpha/2} & \cos\theta \end{pmatrix} \qquad (3.1)$$

where the parameters ϕ and θ determine the coupling between the ports of the tee, while α is the parameter related to the location of the reference planes of the ports.

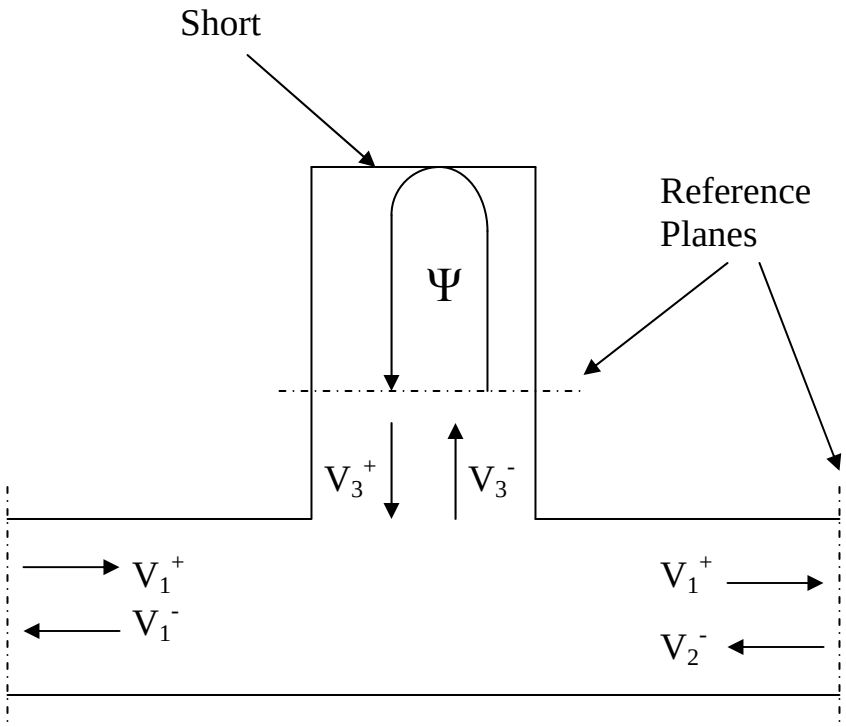


Figure 12. A symmetric Tee junction with a short plane in the symmetric arm

When the 3rd port of the Tee is shorted as shown in Figure 12, the reflected wave in third arm can be expressed as

$$V_3^+ = -e^{j\Psi} V_3^- \tag{3.2}$$

where Ψ is the roundtrip phase advance in the 3rd arm.

For the 3 port network, we have:

$$V^- = SV^+ \tag{3.3}$$

$$V_3^- = S_{31}V_1^+ + S_{32}V_2^+ + S_{33}V_3^+ \tag{3.4}$$

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ + S_{13}V_3^+ \tag{3.5}$$

Combining (3.2) and (3.4), we have:

$$\begin{cases} V_3^- = \dfrac{S_{31}}{1+S_{33}e^{j\Psi}}(V_1^+ + V_2^+) \\ V_3^+ = \dfrac{S_{31}e^{j\Psi}}{1+S_{33}e^{j\Psi}}(V_1^+ + V_2^+) \end{cases} \tag{3.6}$$

Substituting (3.6) in (3.5),

$$V_1^- = \left(S_{11} - \frac{S_{13}S_{31}e^{j\Psi}}{1-S_{33}}\right)V_1^+ + \left(S_{12} - \frac{S_{13}S_{31}e^{j\Psi}}{1-S_{33}}\right)V_2^+ \tag{3.7}$$

The resultant two-port network S-matrix is then obtained. Substituting the elements of the three-port network S-matrix into (3.1), the elements of the two port network S-matrix $\hat{S}$ can be expressed as:

$$\begin{cases} \hat{S}_{11} = S_{11} - \dfrac{S_{13}S_{31}e^{j\Psi}}{1-S_{33}} = \dfrac{1}{2}(e^{j\phi} - \cos\theta)e^{j\alpha} - \dfrac{1}{2}\left(\dfrac{\sin^2\theta}{1+\cos\theta e^{j\Psi}}\right)e^{j\alpha}e^{j\Psi} \\ \hat{S}_{12} = S_{12} - \dfrac{S_{13}S_{31}e^{j\Psi}}{1-S_{33}} = \dfrac{1}{2}(-e^{j\phi} - \cos\theta)e^{j\alpha} - \dfrac{1}{2}\left(\dfrac{\sin^2\theta}{1+\cos\theta e^{j\Psi}}\right)e^{j\alpha}e^{j\Psi} \end{cases} \tag{3.8}$$

The symmetry of the S-matrix gives the other two elements, $\hat{S}_{22} = \hat{S}_{11}$, $\hat{S}_{21} = \hat{S}_{12}$.

To simplify the expression, we can define a phase ζ as

$$e^{j\zeta} = \frac{-\cos\theta - e^{j\Psi}}{1+\cos\theta e^{j\Psi}} = -\cos\theta + \frac{\sin^2\theta}{1+\cos\theta e^{j\Psi}} \tag{3.9}$$

Then the S-parameters can be rewritten as:

$$\begin{cases} \hat{S}_{11}e^{-j\alpha} = \dfrac{1}{2}(e^{j\phi} + e^{j\zeta}) = \cos(\dfrac{\zeta-\phi}{2})e^{j(\frac{\zeta+\phi}{2})} \\ \hat{S}_{12}e^{-j\alpha} = \dfrac{1}{2}(e^{j\phi} - e^{j\zeta}) = \cos(\dfrac{\zeta-\phi}{2})e^{j(\frac{\zeta-\phi}{2})} \end{cases} \tag{3.2}$$

So the final form of the S-matrix for the two port network is:

$$\hat{S} = \begin{pmatrix} \cos\dfrac{\zeta-\phi}{2}e^{j(\frac{\zeta+\phi}{2}+\alpha)} & j\sin\dfrac{\zeta-\phi}{2}e^{j(\frac{\zeta+\phi}{2}+\alpha)} \\ j\sin\dfrac{\zeta-\phi}{2}e^{j(\frac{\zeta+\phi}{2}+\alpha)} & \cos\dfrac{\zeta-\phi}{2}e^{j(\frac{\zeta+\phi}{2}+\alpha)} \end{pmatrix} \tag{3.11}$$

When $\cos\theta \neq \pm 1$, i.e.; the third port is not decoupled from the three-port network, a change in Ψ will result in a change in ζ, so a switching in S-parameters can be achieved.

3.2 FIELD AND LOSSES

The amplitude of the normalized voltage in the 3rd arm is then given by (3.6). From (3.9), $e^{j\Psi}$ can be expressed as:

$$e^{j\Psi} = -\frac{\cos\theta + e^{j\zeta}}{1 + e^{j\zeta}\cos\theta} \tag{3.12}$$

$$\cos\Psi = -\frac{2\cos\theta + \cos\zeta(1+\cos^2\theta)}{1 + 2\cos\zeta\cos\theta + \cos^2\theta} \tag{3.13}$$

$$\sin\Psi = -\sin\zeta\frac{\sin^2\theta}{1 + 2\cos\zeta\cos\theta + \cos^2\theta} \tag{3.14}$$

Substituting (3.12) into (3.6),

$$V_3^- = \frac{1 + e^{j\zeta}\cos\theta}{\sqrt{2}\sin\theta}e^{j\alpha/2}(V_1^+ + V_2^+) \tag{3.15}$$

So the amplitude of the normalized voltage in the 3rd arm can be expressed as:

$$\left|V_3^+\right|^2 = \left|V_3^-\right|^2 = \frac{1}{2}\frac{(1+2\cos\theta\cos\zeta+\cos^2\theta)}{\sin^2\theta}\left|V_1^+ + V_2^+\right|^2 \qquad (3.16)$$

At the location with phase ξ from the short plane in the 3rd arm, the maximum electric field E_{max} of the standing wave is given by:

$$E_{\max} = 2\left|V_3^-\right|\left|\sin\xi\right|\Big/\sqrt{AG} \qquad (3.17)$$

$$E_{\max} = 2\sqrt{\frac{(1+2\cos\theta\cos\zeta+\cos^2\theta)}{2\sin^2\theta}}\left|\sin\xi\right|\sqrt{\frac{P_{in}Z_g}{AG}} \qquad (3.18)$$

A is the area of the cross-section of the waveguide and G is the geometric factor determined by the shape of the cross-section and the mode. For the TE_{01} mode in a circular waveguide, G=0.24. P_{in} is the equivalent power $\left|V_1^+ + V_2^+\right|^2 \Big/ Z_g$ and Z_g is the waveguide impedance.

When the active window is *off*, the major part of the loss P_{loff} dissipated in the active window comes from the loss in the dielectric in the active window and is proportional to $\left|E_{window}\right|^2$. The calculation of P_{loff} will be given later.

When the active window is *on* and becomes a short plane, the loss dissipated on the plane is

$$\begin{aligned} P_{lon} &= \left|H_{short}\right|^2 R_s \\ &= \left|2H^+\right|^2 R_s \\ &= 4\left|V_3^+\right|^2 \frac{R_s}{Z_g^2} \\ &= 2\frac{(1+2\cos\theta\cos\zeta+\cos^2\theta)}{\sin^2\theta}\frac{R_s}{Z_g}P_{in} \end{aligned} \tag{3.19}$$

where R_s is the surface resistance of the reflecting surface.

$$R_s = \sqrt{\frac{\omega\mu}{2\sigma}} \tag{3.20}$$

Both of the losses are proportional to $\left|V_3^+\right|^2$.

For different values of $\cos\zeta$, $\frac{(1+2\cos\theta\cos\zeta+\cos^2\theta)}{\sin^2\theta}$ is minimized at different value of $\cos\theta$. For $\cos\zeta = 0$, (3.16) will be minimized to 1 with $\cos\theta = 0$. If $\cos\zeta$ is close to -1, (3.16) will be close 0 when $\cos\theta$ is close to 1. However, when $\cos\theta$ is close to 1, as long as $\cos\zeta$ changes slightly, the value of $\frac{(1+2\cos\theta\cos\zeta+\cos^2\theta)}{\sin^2\theta}$ will be extremely large.

In normal operation, $\cos\zeta$ will change its value after switching. The value of $\cos\theta$ can be chosen after balancing the requirements of maximum E-field on the active window during the *off* state and the loss during both the *off* and *on* states. The detail will be discussed in the following sections.

In a more general case, the active window will be used for different setups, and the values of $\cos\zeta$ are usually uncertain. To avoid the cases of extremely large losses and high E-fields, the preferred value of $\cos\theta$ is 0. This can be achieved by matching the third-port

with splitting the power equally between the other two ports for an incident wave on the 3rd port.

3.3 THIN ACTIVE WINDOW

When the active element is switched from off to on, the round trip RF phase in the 3rd arm of the Tee will change from Ψ_0 to Ψ_1. During the *off* state, if the active window is thin enough, the phase advance inside the window and the reflection from the window can be ignored, so $\xi = (\Psi_0 - \Psi_1)/2$. In this case, the RF loss in the window during the *off* state will be minimal and it is not necessary to be considered. The maximum E-field will be the major concern for the *off* state.

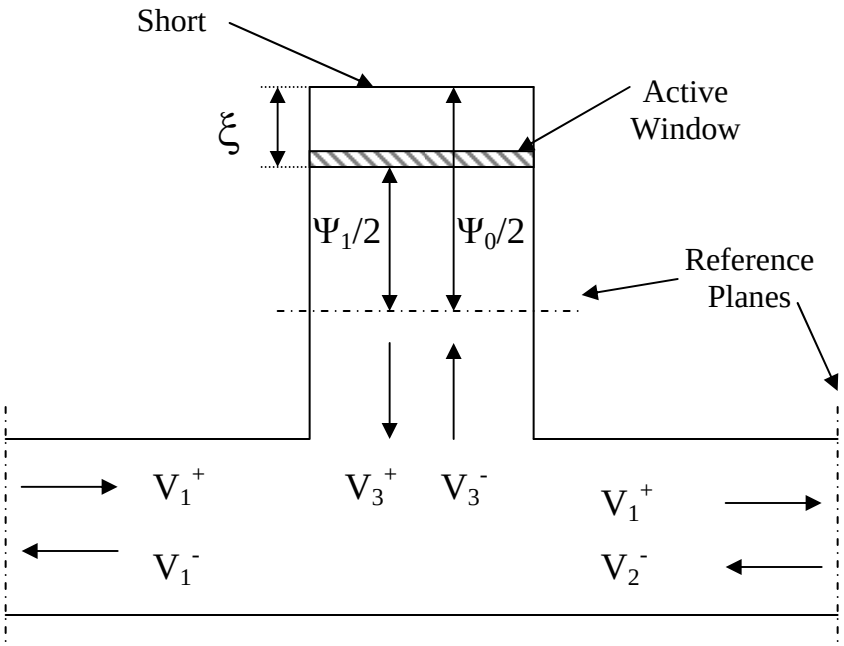


Figure 13. Thin active window in the active element

In the operation of the active element, the reflection coefficient will change from $\cos\psi_0$ to $\cos\psi_1$ after the switching. From (3.11), phase ζ before and after switching will be

$$\begin{aligned}\zeta_0 &= \phi + 2\psi_0 \\ \zeta_1 &= \phi + 2\psi_1\end{aligned} \tag{3.21}$$

The phase in the 3rd arm before and after switching can be calculated using (3.12)

$$\begin{aligned}e^{j\Psi_0} &= -\frac{\cos\theta + e^{j\zeta_0}}{1 + e^{j\zeta_0}\cos\theta} \\ e^{j\Psi_1} &= -\frac{\cos\theta + e^{j\zeta_1}}{1 + e^{j\zeta_1}\cos\theta}\end{aligned} \tag{3.22}$$

The loss during the *on* state is

$$P_{lon} / P_{in} = 2\frac{(1 + 2\cos\theta\cos\zeta_1 + \cos^2\theta)}{\sin^2\theta}\frac{R_s}{Z_g} \tag{3.23}$$

During the *off* state, the electric field on the window is

$$V_{window} = 2\left|V_3^+\right|\left|\sin\frac{\Delta\Psi}{2}\right| \tag{3.24}$$

$$E_{\max} = 2\sqrt{\frac{(1 + 2\cos\theta\cos\zeta_0 + \cos^2\theta)}{2\sin^2\theta}}\left|\sin\frac{\Delta\Psi}{2}\right|\sqrt{\frac{P_{in}Z_g}{AG}} \tag{3.25}$$

where

$$\Delta\Psi = \Psi_1 - \Psi_0$$

From (3.22), $\Delta\Psi$ can be calculated as

$$\begin{aligned}e^{j\Delta\Psi} &= \frac{1 + e^{j\zeta_0}\cos\theta}{\cos\theta + e^{j\zeta_0}}\frac{\cos\theta + e^{j\zeta_1}}{1 + e^{j\zeta_1}\cos\theta} \\ &= \frac{2\cos\theta + e^{j\zeta_0}\cos^2\theta + e^{-j\zeta_0}}{1 + 2\cos\zeta_0\cos\theta + \cos^2\theta}\frac{2\cos\theta + e^{-j\zeta_1}\cos^2\theta + e^{j\zeta_1}}{1 + 2\cos\zeta_1\cos\theta + \cos^2\theta}\end{aligned} \tag{3.26}$$

The real part of (3.26) is

$$\cos\Delta\Psi = \frac{(1+\cos^4\theta)\cos(\zeta_0-\zeta_1)+\cos^2\theta(2\cos(\zeta_0+\zeta_1)+4)+2(\cos\zeta_0+\cos\zeta_1)(\cos^3\theta+\cos\theta)}{(1+2\cos\zeta_0\cos\theta+\cos^2\theta)(1+2\cos\zeta_1\cos\theta+\cos^2\theta)} \tag{3.27}$$

So

$$\begin{aligned}\sin^2\frac{\Delta\Psi}{2} &= \frac{1-\cos\Delta\Psi}{2} \\ &= \frac{\sin^4\theta(1-\cos(\zeta_0-\zeta_1))}{2(1+2\cos\zeta_0\cos\theta+\cos^2\theta)(1+2\cos\zeta_1\cos\theta+\cos^2\theta)} \\ &= \frac{\sin^4\theta\sin^2(\psi_1-\psi_0)}{(1+2\cos\zeta_0\cos\theta+\cos^2\theta)(1+2\cos\zeta_1\cos\theta+\cos^2\theta)}\end{aligned} \tag{3.28}$$

Combining (3.25) and (3.28) we get

$$E_{\max}^2 = \frac{2\sin^2\theta\sin^2(\psi_1-\psi_0)}{(1+2\cos\zeta_1\cos\theta+\cos^2\theta)}\frac{P_{in}Z_g}{AG} \tag{3.29}$$

If there is a certain limit of the maximum *on* state loss L for the active element, (3.23) can be rewritten as

$$L = P_{lon}/P_{in} = 2\frac{(1+2\cos\theta\cos\zeta_1+\cos^2\theta)}{\sin^2\theta}\frac{R_s}{Z_g} \tag{3.30}$$

θ and ϕ can be carefully chosen to satisfy this condition. Multiplying (3.29) by (3.30), the equivalent input power is expressed as

$$P_{in} = \frac{AGL}{4R_s\sin^2(\psi_1-\psi_0)}E_{\max}^2 \tag{3.31}$$

Equation (3.31) shows the factors determining the power handling capacity of the active element. The power handling capacity is proportional to the acceptable *on* state loss and the allowable electric field, but inversely proportional to the surface resistance. It's independent of the waveguide impedance.

During the *off* state, the major part of the attenuation in the window comes from the conductivity σ of the material.

$$\alpha = \frac{\sigma Z_2}{2} \tag{3.32}$$

The *off* state loss is

$$\begin{aligned} P_{loff} &= \frac{2\alpha l}{Z_2}\left|V_{window}\right|^2 \\ &= \sigma l\left|2V_3^+ \sin\frac{\Delta\Psi}{2}\right|^2 \\ &= \sigma l \frac{2\sin^2\theta}{(1+2\cos\theta\cos\zeta_1+\cos^2\theta)} P_{in} Z_g \sin^2(\psi_1-\psi_0) \end{aligned} \tag{3.33}$$

$$\frac{P_{lon}P_{loff}}{P_{in}^2} = 4\sigma l R_s \sin^2(\psi_1-\psi_0) \tag{3.34}$$

3.4 THICK ACTIVE WINDOW

For an actual silicon window, the thickness would be too large to ignore. The 3rd arm of the Tee can be illustrated by Figure 14. The active window is simplified to be a slab of silicon with thickness *l* inserted in the waveguide. The vacuum (or air) part of the waveguide will have waveguide impedance Z_1 and wavenumber β_1, while the silicon part has waveguide impedance Z_2 and wavenumber β. The phase between the wafer and the short plane is ξ. The *on* state property of the active element is still the same as that of the

thin window approximation. But the *off* state model has to be modified due to the reflection at the silicon-vacuum interface.

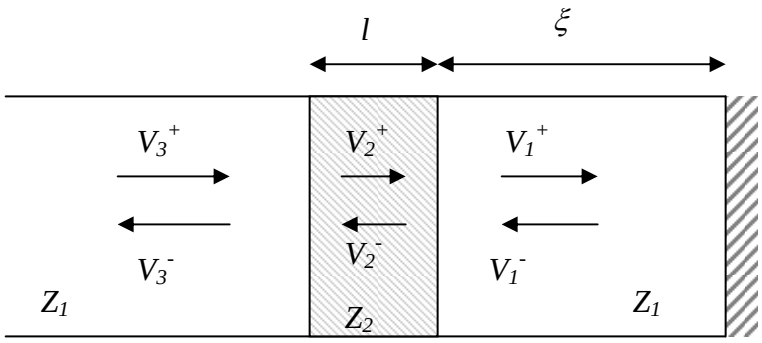


Figure 14. Thick active window

The reference plane of V_1 is chosen at the right surface of the active window, while the left surface of the window is the reference plane for V_2 and V_3. During the *on* state, the incoming and reflected RF has opposite phase at the left surface of the window, i.e. $V_3^- = -V_3^+$. If the phase change from the *off* state to the *on* state is $\Delta\Psi$, during the *off* state we will have $V_3^- = -V_3^+ e^{-j\Delta\Psi}$. The boundary condition at the interfaces gives the following equations for the forward and reflected field:

$$\begin{cases} V_3^+ + V_3^- = V_2^+ + V_2^- \\ V_2^+ e^{j\beta l} + V_2^- e^{-j\beta l} = V_1^+ (1 - e^{j2\xi}) \\ \dfrac{V_3^+ - V_3^-}{Z_1} = \dfrac{V_2^+ - V_2^-}{Z_2} \\ \dfrac{V_2^+ e^{j\beta l} - V_2^- e^{-j\beta l}}{Z_2} = \dfrac{V_1^+}{Z_1}(1 + e^{j2\xi}) \end{cases} \tag{3.35}$$

The solution for the amplitudes will be

$$\begin{cases} V_2^+ / V_3^+ = \dfrac{1}{2}\left[(1-e^{-j\Delta\Psi}) + \dfrac{Z_2}{Z_1}(1+e^{-j\Delta\Psi})\right] \\ V_2^- / V_3^+ = \dfrac{1}{2}\left[(1-e^{-j\Delta\Psi}) - \dfrac{Z_2}{Z_1}(1+e^{-j\Delta\Psi})\right] \\ V_1^+ / V_3^+ = \cos\beta l + \dfrac{1}{2}\, j \sin\beta l\left[\dfrac{Z_1}{Z_2}(1-e^{-j\Delta\Psi}) + \dfrac{Z_2}{Z_1}(1+e^{-j\Delta\Psi})\right] \\ e^{j2\xi} = \dfrac{\cos\beta l e^{-j\Delta\Psi} + \dfrac{1}{2}\, j \sin\beta l\left[\dfrac{Z_1}{Z_2}(1-e^{-j\Delta\Psi}) - \dfrac{Z_2}{Z_1}(1+e^{-j\Delta\Psi})\right]}{\cos\beta l + \dfrac{1}{2}\, j \sin\beta l\left[\dfrac{Z_1}{Z_2}(1-e^{-j\Delta\Psi}) + \dfrac{Z_2}{Z_1}(1+e^{-j\Delta\Psi})\right]} \end{cases} \tag{3.36}$$

The field inside the wafer is

$$\frac{V_2^+(x) + V_2^-(x)}{V_3^+} = \cos(\beta x)(1-e^{-j\Delta\Psi}) + j\sin(\beta x)\frac{Z_2}{Z_1}(1+e^{-j\Delta\Psi}) \tag{3.37}$$

$$\left|\frac{V_2^+(x) + V_2^-(x)}{V_3^+}\right| = 2\left|\cos(\beta x)\sin\frac{\Delta\Psi}{2} + \sin(\beta x)\frac{Z_2}{Z_1}\cos\frac{\Delta\Psi}{2}\right| \tag{3.38}$$

x is the distance from the left side of the window.

The loss in the wafer can be calculated as

$$\begin{aligned} P_{loff} &= \int_0^l 2\alpha \frac{\left|V_2^+(x) + V_2^-(x)\right|^2}{Z_2} dx \\ &= 2Z_g \sigma P_3 \left\{ \sin^2\frac{\Delta\Psi}{2}\left[l + \frac{\sin(2\beta l)}{2\beta}\right] \right. \\ &\quad \left. + \cos^2\frac{\Delta\Psi}{2}\left(\frac{Z_2}{Z_1}\right)^2\left[l - \frac{\sin(2\beta l)}{2\beta}\right] + \frac{1}{\beta}\frac{Z_2}{Z_1}\sin\Delta\Psi\sin^2(\beta l)\right\} \end{aligned} \tag{3.39}$$

$$\frac{P_{lon}P_{loff}}{P_{in}^2} = 2\left\{\left[l + \frac{\sin(2\beta l)}{2\beta}\right] + \cot^2\frac{\Delta\Psi}{2}\left(\frac{Z_2}{Z_1}\right)^2\left[l - \frac{\sin(2\beta l)}{2\beta}\right] + \cot\frac{\Delta\Psi}{2}\frac{Z_2}{Z_1}\frac{2}{\beta}\sin^2(\beta l)\right\}\sin^2(\psi_1 - \psi_0)\sigma R_s \tag{3.40}$$

To keep the power handling capacity of the thick window to be not worse than that of the thin window, the maximum value of (3.38) should be same as (3.24), i.e., the peak electric field happens at the left surface of the window. The value of $\Delta\Psi$ should be carefully chosen. One general choice is $\Delta\Psi = \pi$, which makes the E-fields described in (3.38) equal to that of (3.24) constantly. In this case, the power handling capacity is

$$P_{in} = \frac{AGL}{4R_s\sin^2(\psi_1 - \psi_0)}E_{\max}^2 \tag{3.31}$$

By choosing $\Delta\Psi = \pi$, the *off* state loss is

$$\frac{P_{lon}P_{loff}}{P_{in}^2} = \left(2l + \frac{\sin 2\beta l}{\beta}\right)\sin^2(\psi_1 - \psi_0)\sigma R_s \tag{3.41}$$

When the wafer is thinner than the half wavelength, the electric field inside the window can be kept lower than the left surface if $\Delta\Psi$ is in the range

$$\pi \le \Delta\Psi \le 2\left[\pi - \arctan\left(\tan(\beta l/2)\frac{Z_2}{Z_1}\right)\right] \tag{3.42}$$

By choosing $\Delta\Psi = 2\left[\pi - \arctan\left(\tan(\beta l/2)\frac{Z_2}{Z_1}\right)\right]$, the *off* state loss is minimized.

$$\frac{P_{lon}P_{loff}}{P_{in}^2} = \frac{2}{\sin^2(\beta l/2)}\left[l - \frac{\sin(\beta l)}{\beta}\right]\sin^2(\psi_1 - \psi_0)\sigma R_s \tag{3.43}$$

In this case, peak field occurs on both sides of the window, and the center of the wafer will be a node with low field. When the window thickness is small, (3.43) reduces to one third of (3.34) or (3.41).

$$\frac{P_{lon}P_{loff}}{P_{in}^2} = \frac{4}{3} l \sin^2(\psi_1 - \psi_0)\sigma R_s \tag{3.44}$$

For given values of ψ_0 and ψ_1, a certain value of $\Delta\Psi$ can be achieved by adjusting the parameters θ and ϕ of the Tee, so that the power handling capacity and *off* state loss can be optimized. The value of these two parameters also needs to satisfy the requirement of *on* state loss (3.30).

For example, if $\Delta\Psi = \pi$ is desired, $\psi_0 = 0$ and $\psi_1 = \pi/2$,

$$\begin{aligned} \zeta_0 &= \phi \\ \zeta_1 &= \phi + \pi \end{aligned} \tag{3.45}$$

$$e^{j\Delta\Psi} = \frac{1 + e^{j\phi}\cos\theta}{\cos\theta + e^{j\phi}} \frac{\cos\theta - e^{j\phi}}{1 - e^{j\phi}\cos\theta} \tag{3.46}$$

We can choose $\phi = 0$, then

$$\begin{aligned} e^{j\Delta\Psi} &= -1 \\ \Delta\Psi &= \pi \end{aligned} \tag{3.47}$$

3.5 PHYSICS OF THE ON STATE OF THE ACTIVE ELEMENT

In this section, we will discuss the basic physics when the active window is reflective.

During the *on* state of the active window, we assume that a uniform conducting layer is formed in the active window to reflect the RF. The loss at the short plane is

$$\begin{aligned} P_{lon} &= \left|H_{short}\right|^2 R_s \\ &= 4\left|V_3^+\right|^2 \frac{R_s}{Z_g^2} \\ &= 4P_3 \frac{R_s}{Z_g} \end{aligned} \tag{3.45}$$

R_s is the surface resistivity given by (3.20)

$$R_s = \sqrt{\frac{\omega\mu}{2\sigma}}$$

If the active window is made of semiconductor materials, the conductivity of the semiconductor is given by

$$\sigma = e(\mu_n n + \mu_p p) \tag{3.46}$$

where e is the charge of electron, n and p are the density of electrons and holes respectively, μ_n and μ_p are the mobility of electrons and holes respectively. Since the electrons and holes are generated in pairs and the number of the generated carriers is much larger than the equilibrium carriers in the intrinsic region, n and p can be considered equal during the *on* state. So the conductivity can be simplified to be $\sigma = 2e\mu_{eff} n$, with μ_{eff} defined as the effective mobility, which is the average of the mobility of the *n* and *p* type carries. The mobility is dependent on several parameters, like temperature, electric field, impurity (dopant) concentration and carrier density, etc. With higher carrier or impurity concentration, the scattering of carriers becomes more frequent and results in lower mobility. However, the mobility's dependence on carrier density is weak and can be treated as a constant for a rough estimation.

To accomplish full reflection, the required thickness of the conducting layer is approximately the skin depth. The skin depth of a conductor is given by

$$\delta_s = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{3.47}$$

The total number of the required carrier pairs will be

$$\begin{aligned} N &= \delta_s A n \\ &= \frac{A}{2R_s e\mu_{eff}} \end{aligned} \tag{3.48}$$

where A is the area of the waveguide cross-section.

Combining (3.31), (3.33) and (3.48),

$$P_{in} = \frac{GLNe\mu_{eff}}{2\sin^2(\psi_1 - \psi_0)} E_{\max}^2 \tag{3.49}$$

$$\frac{P_{loff}}{P_{in}} = \frac{2\sigma_{off} l \sin^2(\psi_1 - \psi_0) A}{LNe\mu_{eff}} \tag{3.50}$$

(3.50) represents the case of the thin film approximation. If θ and ϕ are optimized for the *off* state loss in the case that the window is thick, the *off* state loss is 1/3 of (3.50). From (3.49) and (3.50), we can summarize the factors determining the performance of the switch as the following:

- The power handling capacity is proportional to the square of the maximum allowable electric field of the window times a geometric factor. To maximize the power handling capacity, it's necessary to choose a material and design which can sustain high electric field.

- The *off* state loss is proportional to the conductivity and the thickness of the window. The window should use high resistivity material with small thickness to reduce the loss. With a given value of the *on* state loss, the *off* state loss is inversely proportional to the surface density of carrier pairs during the *on* state, so higher surface density is preferred.

- With a given value of the *on* state loss, the number of carrier pairs and the effective mobility are proportional to the power handling capacity. The major factor determining the performance of the module is the capability to generate the carrier pairs on the surface of the window. Although the mobility is also proportional to the performance, it's basically determined by the choice of material, which will compromise other properties, such as the breakdown electric field and the carrier lifetime.

- The performance of the module is independent of the waveguide impedance Z_g. An increase of Z_g will increase the field and reduce the *on* state loss in the window, but the effect can be canceled by changing the parameters of the Tee.

- However, the above conclusions are based on the assumption that the loss at the waveguide wall and the *off* state loss are small compared to the *on* state loss of the window. When the *on* state loss of the window is low enough, the increase of carrier number will not help to enhance the power handling capacity, and the increase of Z_g will lower the performance. The *on* state loss of the window can not be too high, either. The derivation of the S-matrix of the terminated 3-port network (3.11) is based on the assumption that the reflection loss from the 3rd arm is low.

3.6 DESIGN EXAMPLE

Now we consider a design example. The window uses silicon material of 0.5mm thick in a circular waveguide (G=0.24) with 1.5 inch diameter. The working frequency is 11.424GHz, and the mode is TE_{01}. The resistivity of the silicon is chosen at 10KΩcm, so the *off* state conductivity is $\sigma_{off} = 0.01\mathrm{S}\cdot\mathrm{m}^{-1}$. The desired reflection coefficients are $\cos\psi_0 = 0.90$ and $\cos\psi_1 = 0.31$, which are the numbers optimized for an active resonant delay line compression system with compression ratio of 20 and phase flip before last bin considering the losses, as described in Table 2. This gives $\sin^2(\psi_1 - \psi_0) = 0.52$.

During the *on* state, the injected carrier density is $10^{16}/\mathrm{cm}^3$, and the desired loss is 10%. The relative dielectric constant of silicon is 11.9, and the maximum allowable electric field is $1\square 10^7$V/m, which is 1/3 of the DC breakdown field of silicon.

Using the concentration dependent low field mobility model [30], the mobility for a carrier density of $10^{16}/\mathrm{cm}^3$ will be $\mu_{eff} = 768\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. The high field mobility will be

even lower, but since the value of electric field is not certain, the low field mobility is used as an approximation. The *on* state conductivity can be calculated as $\sigma = 2e\mu_{eff} n = 246\mathrm{S}\cdot\mathrm{m}^{-1}$. The *on* state skin depth is $\delta_s = \sqrt{\frac{2}{\omega\mu\sigma}} = 300\mu\mathrm{m}$ and the total number of required carrier pairs will be $N = 3.4\times10^{15}$. The surface resistivity can be calculated as $R_s = \sqrt{\frac{\omega\mu}{2\sigma}} = 13.5\Omega$.

The power handling capacity is

$$P_{in} = \frac{GLNe\mu_{eff}}{2\sin^2(\psi_1 - \psi_0)} E_{\max}^2 = 97\mathrm{MW}$$

The power handling capacity of one active element may be even lower under certain conditions, such as the stricter requirement for the *on* state losses, the maximum allowed electric field is lower, or the surface resistance is higher. A multi-element module can be used to enhance the performance of the switch further, which will be discussed in the next chapter.

The *off* state loss in the window with the thin window approximation is

$$\frac{P_{loff}}{P_{in}} = \frac{2\sigma_{off} l \sin^2(\psi_1 - \psi_0) A}{LNe\mu_{eff}} = 4.2\times10^{-5}$$

We can see that the loss is very small. Even if the carrier density is lower and the *on* state loss requirement is stricter, the *off* state loss in the window can still satisfy the requirement.

3.7 THE CIRCULAR WAVEGUIDE TEE

The active window is preferred to be working in the circular waveguide under TE_{01} mode to avoid RF leakage and enhance power handling capacity. A low-loss circular waveguide Tee junction has been designed and fabricated for our test setup. This Tee is composed of a TE_{20} mode rectangular Tee and 3 circular-to-rectangular mode converters [23, 24]. The 3rd port reflection is eliminated (S_{33}=0). Figure 15 shows the model assembly of the circular waveguide Tee.

By selecting appropriate reference planes, the S matrix of this Tee can be expressed in the following form:

$$S = \begin{pmatrix} \frac{1}{2} & -\frac{1}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{1}{2} & \frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \end{pmatrix} \tag{3.51}$$

In the case that the active element needs a reflection of $\cos\theta$ in the 3rd port, an iris with reflection $\cos\theta$ can be added to the 3rd port. By adjusting the location of the iris and the reference plane of port 1 and 2, the S-matrix will be in the form of (3.1).

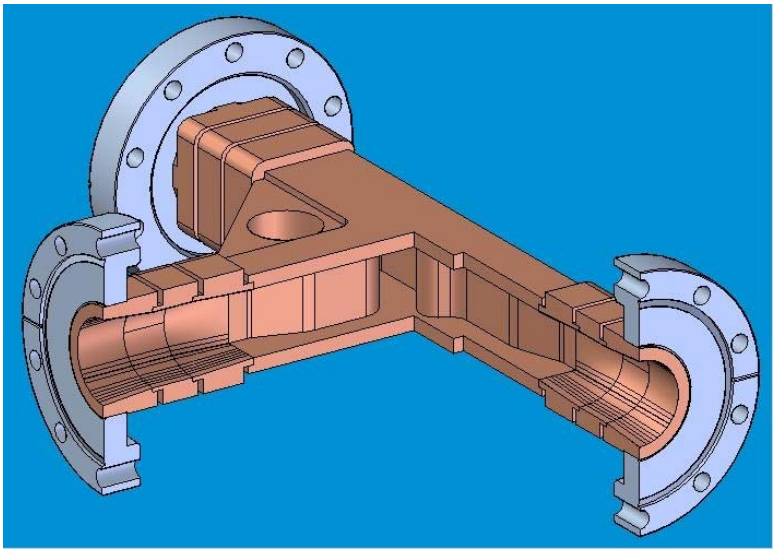


Figure 15. Model Assembly of the Circular Waveguide Tee

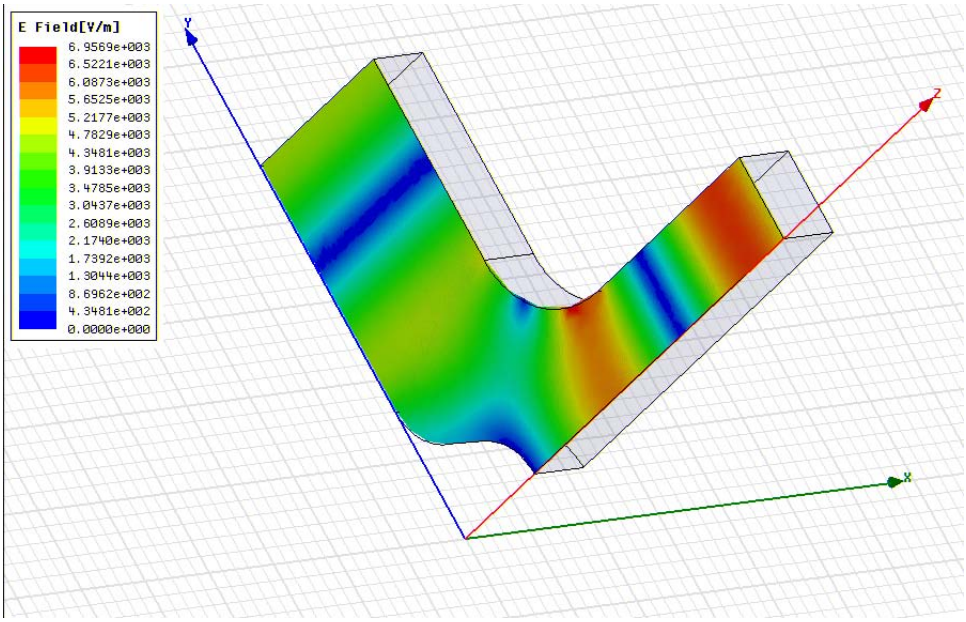


Figure 16. E-field in the rectangular Tee

Figure 16 shows the details in a quarter of the rectangular Tee and the E-field when the wave is fed from the 3rd port. When the 3rd port is excited, the Tee splits the incoming

wave equally into the other two ports. The x-z plane is the center cross-section of the 3rd arm, which can be considered as a perfect E boundary in this case. The y-z plane is the center cross-section of all three ports, which can be considered as a perfect H boundary under the TE_{20} mode. The geometry in the y-z plane is determined by matching the half of port 3 to the port 1. The rectangular Tee is an E-plane Tee with the E-field in the x-y plane only; hence the Tee geometry does not affect the mode index.

3.8 THE DESIGN OF THE CIRCULAR-TO-RECTANGULAR MODE CONVERTER

Circular waveguides are frequently used in ultrahigh power RF systems due to the high power handling capacity and low losses. However, in some instances, a rectangular waveguide is preferred to handle the RF and achieve certain functions, for example the Tee junction and the bend. A mode converter is required to transport RF between a circular waveguide and a rectangular waveguide.

To study the active switch, a compact circular-to-rectangular taper was designed. The taper is an adiabatic transition between two uniform waveguides. A single RF mode entering the adiabatic transition will not scatter into multiple modes, but will propagate as a single mode and exit the transition in the desired mode. The taper was first designed numerically and published in [24] and subsequently manufactured. The analytical procedure of the design was described in [28]. The taper has a smaller size and lower losses compared to the conventional mode converter designs.

The taper comprises three sections. The geometry of the taper is shown in Figure 18, and Figure 17 shows the cross-sections in different sections of the taper. The first taper takes the rectangular shaped waveguide into an approximately elliptical shaped waveguide. Both guides are overmoded, and several modes can propagate. However, the modes that are excited by the incident TE_{20} mode have to respect both geometric symmetries and the incident mode symmetries. The dimensions of the rectangular and the elliptic-like waveguide allow only two such modes to propagate, which, in the elliptic-like

waveguide, we call M_1 and M_2. The second section is a straight waveguide with the elliptic-like cross section. This is used to change the relative phase between M_1 and M_2. The third section is a taper between the elliptic-like waveguide and circular waveguide. Again, the circular waveguide is overmoded, with several modes that can propagate. However, only two modes that respect the excitation symmetries of M_1 and M_2 and the geometric symmetries of the taper can propagate in the circular waveguide, namely the TE_{01} mode and the TE_{21} mode. The first taper and the third (final) taper are matched with respect to M_1 and M_2 in the sense that the relative amplitudes of M_1 and M_2 are the same for either excitation by an incident TE_{20} from the rectangular port or TE_{01} from the circular port. Hence, by adjusting the phase relation through the middle section, the TE_{01} mode can be reconstructed perfectly at the circular port.

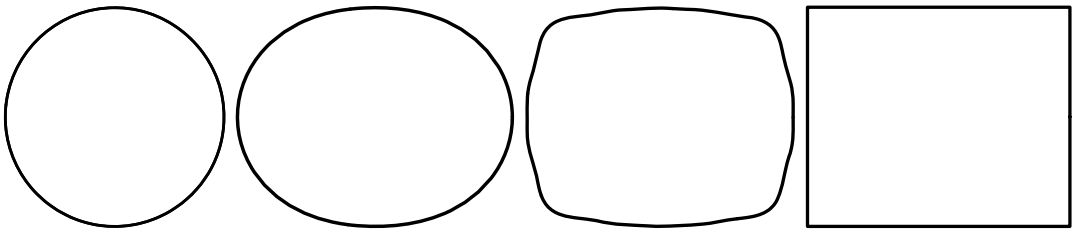


Figure 17. Cross sections of the circular waveguide, elliptical waveguide, middle of taper2, and rectangular waveguide

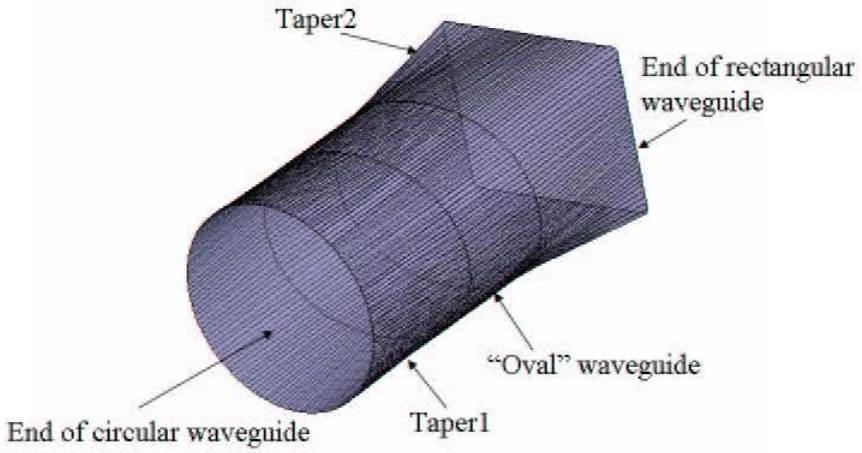


Figure 18. The three-section compact mode converter

3.9 THE ANALYSIS OF THE CIRCULAR-TO-RECTANGULAR TAPER

In this section, we will discuss the analytic design of the circular-to-rectangular taper. The geometry of the different sections of the taper will be parameterized, and then a analytic solution of the eigenmodes will be given. The mode coupling in the taper will be calculated, and finally, the geometric parameters of the taper will be optimized for the desired mode coupling. The advantage of this analytic method is that the solution can be obtained quickly without heavy computation. However, the analytic method has obviously limited accuracy due to the approximations made. Therefore, the analytic

method can only be used as a tool that gives a reasonable initial point for the traditional numerical optimization. The final solution will be found using HFSS.

In general, the wall radius of a waveguide with a twofold symmetric cross-section can be expanded as:

$$r_w(\phi) = a_0\left(1 + \varepsilon\sum_{p=1}^{P}\delta_p \cos(2p\phi)\right) \tag{3.52}$$

where ε is a small parameter which may be considered as a factor of perturbation to a circle with radius a_0 , and δ_p are Fourier expansion coefficients with δ_1 normalized to 1.

The mode converter has three sections. The first linear taper section starts with a circular cross-section:

$$r_{w,c}(\phi) = a_0 \tag{3.53}$$

and ends with an oval cross-section wall radius:

$$r_{w,oval}(\phi) = a_0(1 + \varepsilon_{oval}\cos(2\phi)) \tag{3.54}$$

The cross-section wall radius in the first linear taper (taper1 in Figure 18) is given by

$$r_{w,taper1}(\phi, z) = a_0(1 + \varepsilon_1\cos(2\phi)) \tag{3.55}$$

where

$$\varepsilon_1 = \varepsilon_{oval} z / L_1$$

L_1 is the length of taper1, and z is the distance to the starting cross-section. We can see that the wall radius in this section of taper has only the first order Fourier expansion.

For the final linear taper (taper2 in Figure 18), it starts with the oval cross-section $r_{w,oval}(\phi)$ and end with the rectangular cross-section. The wall radius of the rectangular cross-section with side lengths c and d is given as:

$$r_{w,rect} = \begin{cases} \dfrac{d}{2\cos\phi}, & 0 < \phi < \tan^{-1}\left(\dfrac{c}{d}\right) \\ \dfrac{c}{2\cos\phi}, & \tan^{-1}\left(\dfrac{c}{d}\right) < \phi < \dfrac{\pi}{2} \end{cases} \tag{3.56}$$

For the rectangular waveguide, the wall radius can be expanded in the form of (3.52) with coefficients as:

$$\begin{aligned} a_{0,rect} &= \frac{1}{2\pi} c\left\{\left[\log\left(\cos\frac{\varsigma}{2}+\sin\frac{\varsigma}{2}\right)-\log\left(\cos\frac{\varsigma}{2}-\sin\frac{\varsigma}{2}\right)\right]\right. \\ &\quad \left. + d\left[\log\left(\cos\frac{\varsigma}{2}\right)-\log\left(\sin\frac{\varsigma}{2}\right)\right]\right\} \\ \varepsilon_{rect} &= \frac{1}{a_{0,rect}\pi}\left\{c\left[\log\left(\cos\frac{\varsigma}{2}+\sin\frac{\varsigma}{2}\right)-\log\left(\cos\frac{\varsigma}{2}-\sin\frac{\varsigma}{2}\right)+2\sin\varsigma\right]\right. \\ &\quad \left. + d\left[\log\left(\cos\frac{\varsigma}{2}\right)-\log\left(\sin\frac{\varsigma}{2}\right)-2\cos\varsigma\right]\right\} \\ \delta_{p,rect} &= \frac{1}{a_{0,rect}\varepsilon_{rect}\pi}\left\{(-1)^{p+1}c\left[\log\left(\cos\frac{\varsigma}{2}+\sin\frac{\varsigma}{2}\right)-\log\left(\cos\frac{\varsigma}{2}-\sin\frac{\varsigma}{2}\right)\right.\right. \\ &\quad \left.\left. -\sum_{i=1}^{p}\frac{2(-1)^i}{2i-1}\sin[(2i-1)\varsigma]\right]\right. \\ &\quad \left. + d\left[\log\left(\cos\frac{\varsigma}{2}\right)-\log\left(\sin\frac{\varsigma}{2}\right)-\sum_{i=1}^{p}\frac{2}{2i-1}\cos[(2i-1)\varsigma]\right]\right\} \end{aligned} \tag{3.57}$$

The expansion coefficients in taper2 can be interpolated as:

$$\begin{cases} a_0 = a + \dfrac{z - L_2}{L - L_2}(a_{0,rect} - a) \\ \varepsilon_2 = \dfrac{1}{a_0}\left[\dfrac{z - L_2}{L - L_2}\left(a_{0,rect}\varepsilon_{rect} - a\varepsilon_{oval}\right) + a\varepsilon_{oval}\right] \\ \delta_p = \dfrac{z - L_2}{L - L_2}\dfrac{a_{0,rect}\varepsilon_{rect}}{a_0\varepsilon_2}\delta_{p,rect} \end{cases} \tag{3.58}$$

where L is the total length of the three taper sections, and L_2 is the length of the first two sections.

The wall radius in the taper2 can be expressed as:

$$r_{w,taper2}(\phi, z) = r_{w,oval} + \frac{z - L_2}{L - L_2}\left(r_{w,rect} - r_{w,oval}\right) \tag{3.59}$$

The transverse electric and magnetic fields inside the nonlinear waveguide can be written as the expansion of eigenmodes:

$$\begin{aligned} \vec{E}_\perp &= \sum_s V_s \vec{e}_s \\ \vec{H}_\perp &= \sum_s I_s \vec{h}_s \end{aligned} \tag{3.60}$$

where the expansion coefficients V_s and I_s are the voltage and current amplitude of the corresponding eigenmodes, while $\vec{e}_s$ and $\vec{h}_s$ are the mode vector functions. For the TE modes, the mode vector functions can be derived from the eigen mode function ψ_s:

$$\vec{e}_s = \hat{z} \times \nabla_\perp \psi_s ;\ \vec{h}_s = \nabla_\perp \psi_s \times \hat{z} \tag{3.61}$$

$\nabla_\perp$ is the gradient operator transverse to the waveguide axis while $\hat{z}$ is the unit vector in the direction of the waveguide axis. The eigen mode function satisfies

$$\begin{aligned} \nabla_\perp^2 \psi_s + k_{\perp s}\psi_s &= 0 \\ \frac{\partial \psi_s}{\partial n} &= 0, \text{at the waveguide wall} \end{aligned} \tag{3.62}$$

$k_{\perp s}$ is the cutoff wave number of the *s*th mode at any waveguide cross-section. $\frac{\partial}{\partial n}$ is the gradient in the direction normal to the waveguide wall, pointing outward. The solution of the eigen modes can be written as a Fourier series of the wave in a circular waveguide perturbed by a small expansion factor ε.

$$\psi_s = \sum_{i=0}^{H} \alpha_{2i} J_{2i}(k_{\perp s} r)\cos(2i\phi) \tag{3.63}$$

where $\alpha_{2i} = \sum_j A_{2i,j}\varepsilon^j$ and $k_{\perp s} = \sum_j \chi_j \varepsilon^j \Big/ a_0$, $A_{2i,j}$ are the expansion coefficients of the mode amplitude and χ_j are the mode cutoff wave numbers at any given cross-section.

The boundary condition at the waveguide wall is that the tangential component of the electric field is 0:

$$\vec{e}_s \cdot \frac{\partial \vec{r}_w}{\partial \phi} = 0 \tag{3.64}$$

Thus the expansion coefficients of the eigen mode satisfies

$$\begin{aligned}&\sum_{i=0}^{H}\sum_{j=0}^{H}\sum_{p=1}^{P} A_{2i,j}\varepsilon^j \{-\frac{4ip\delta_p\varepsilon}{1+\varepsilon\delta_p\cos(2p\phi)} J_{2i}(X_{jp})\sin(2i\phi)\sin(2p\phi) \\ &+ a_0\chi_j\varepsilon^j J'_{2i}(X_{jp})[1+\varepsilon\delta_p\cos(2p\phi)]\} = 0\end{aligned} \tag{3.65}$$

where $X_{jp} = a_0\chi_j\varepsilon^j[1+\varepsilon\delta_p\cos(2p\phi)]$

The left hand side of equation (3.65) can be expanded as power series of ε, so the coefficients of each power of ε are equal to 0. Thus the expansion coefficients $A_{2i,j}$ and χ_j can be solved at any cross section in the nonlinear waveguide. A symbolic solver such as Mathematica can be used for the calculation. We have made such a calculation,

using the radial expansion harmonics $P = 5$ to approximate the waveguide profile and the RF harmonics $H = 6$ to approximate propagating modes.

After the eigenmodes are found, we can estimate the level of mode coupling between scattered modes in the nonlinear waveguides. The study in this dissertation is limited to TE modes only.

The inter mode coupling in a nonlinear waveguide can be accounted through Telegrapher's equations [27]:

$$\begin{aligned} \frac{dV_i}{dz} &= -jk_{z_i} Z_i I_i + \sum_m T_{im} V_m \\ \frac{dI_i}{dz} &= -j\frac{k_{z_i}}{Z_i} V_i - \sum_m T_{mi} I_m \end{aligned} \tag{3.66}$$

where $k_{z_i} = \sqrt{k^2 - k_{\perp i}^2}$ is the uncoupled propagation constant for the *i*th mode, k is the propagation constant in free space, *m* denotes all other modes in the waveguide, and Z_i is the mode wave impedance:

$$Z_i = \sqrt{\frac{\mu}{\varepsilon}} \frac{k}{k_{z_i}} \tag{3.67}$$

The mode coupling coefficients are defined as

$$\begin{aligned} T_{im} &= \int_S \vec{e}_i \cdot \frac{\partial \vec{e}_m}{\partial z} dS = \int_S \nabla_\perp \psi_i \cdot \frac{\partial \psi_m}{\partial z} dS \\ T_{mi} &= \int_S \vec{e}_m \cdot \frac{\partial \vec{e}_i}{\partial z} dS = \int_S \nabla_\perp \psi_m \cdot \frac{\partial \psi_i}{\partial z} dS \end{aligned} \tag{3.68}$$

From Green's theorem of two dimensions,

$$\int_{S(z)} \left(\psi_m \cdot \nabla_\perp^2 \frac{\partial \psi_i}{\partial z} + \nabla_\perp \psi_m \cdot \nabla_\perp \frac{\partial \psi_i}{\partial z} \right) dS = \oint \psi_m \frac{\partial}{\partial n} \left(\frac{\partial \psi_i}{\partial z} \right) dl \tag{3.69}$$

$$\int_{S(z)} \left(\nabla_\perp^2 \psi_m \cdot \frac{\partial \psi_i}{\partial z} + \nabla_\perp \psi_m \cdot \nabla_\perp \frac{\partial \psi_i}{\partial z} \right) dS = \oint \frac{\partial \psi_i}{\partial z} \frac{\partial \psi_m}{\partial n} dl \tag{3.70}$$

Applying the relation $\nabla_\perp^2 \psi_i + k_{\perp i}^2 \psi_i = 0$ in (3.69), we have

$$\int_{S(z)} \nabla_\perp \psi_m \cdot \nabla_\perp \frac{\partial \psi_i}{\partial z} dS = \int_{S(z)} \psi_m \cdot k_{\perp i}^2 \frac{\partial \psi_i}{\partial z} dS + \oint \psi_m \frac{\partial}{\partial n} \left(\frac{\partial \psi_i}{\partial z} \right) dl \tag{3.71}$$

Applying the boundary condition at the waveguide wall $\partial \psi_m / \partial n = 0$, and the relation $\nabla_\perp^2 \psi_i + k_{\perp i}^2 \psi_i = 0$ in (3.70),

$$\int_{S(z)} \nabla_\perp \psi_m \cdot \nabla_\perp \frac{\partial \psi_i}{\partial z} dS = \int_{S(z)} k_{\perp i}^2 \psi_m \cdot \frac{\partial \psi_i}{\partial z} dS \tag{3.72}$$

T_{mi} can be solved from (3.68), (3.71) and (3.72), and similarly we can get T_{im}:

$$\begin{aligned} T_{mi} &= \frac{k_{\perp m}^2}{k_{\perp m}^2 - k_{\perp i}^2} \oint \psi_m \frac{\partial}{\partial n} \left(\frac{\partial \psi_i}{\partial z} \right) dl \\ T_{im} &= \frac{k_{\perp i}^2}{k_{\perp i}^2 - k_{\perp m}^2} \oint \psi_i \frac{\partial}{\partial n} \left(\frac{\partial \psi_m}{\partial z} \right) dl \end{aligned} \tag{3.73}$$

Assuming that the modes considered are above cutoff, the mode voltage and current may be express in terms of forward and backward wave amplitudes, A_i^+ and A_i^-:

$$\begin{aligned} V_i &= Z_i^{1/2} \left(A_i^+ + A_i^- \right) \\ I_i &= Z_i^{-1/2} \left(A_i^+ - A_i^- \right) \end{aligned} \tag{3.74}$$

Assuming that there is no reflection, the amplitude of the *i*th mode due to the coupling with the *m*th mode is

$$\frac{dA_i^+}{dz} + jk_{z_i} A_i^+ = S_{im}^+ A_m^+ \tag{3.75}$$

S_{im}^+ is the transfer coefficient between the two modes,

$$S_{im}^+ = \frac{1}{2}\left[\sqrt{\frac{k_{z_i}}{k_{z_m}}} T_{mi} - \sqrt{\frac{k_{z_m}}{k_{z_i}}} T_{im}\right] \tag{3.76}$$

With the eigenmodes found from (3.65), the mode coupling between the two ports of the mode converter can be found from the differential equation (3.75) for given geometric parameters. We have optimized the geometric parameters of the converter at 11.424GHz. The circular waveguide port has a radius of $a = 1.905\text{cm}$ or 1.5 inch diameter. The dimension of the rectangular waveguide port is given as $c = 1.52\text{cm}$ and $d = 1.82\text{cm}$. The lengths of the three taper sections are optimized so that the amplitude of mode M_2 is the minimum at the end of the converter at a given ε_{oval}. The value of ε_{oval} is scanned to find the shortest length of the mode converter. The result is given as

length of taper1	$L_1 = 2.43\text{cm}$
length of the oval waveguide	$L_2 - L_1 = 1.975\text{cm}$
length of taper2	$L - L_2 = 3.0\text{cm}$
	$\varepsilon_{oval} = 0.1132$

In the final design of the mode converter, the HFSS solver was used to optimize the geometric parameters numerically. The details of the design are given in Ref [24]. The parts 3, 4 and 5 of the mode converter described in Ref [24] are equivalent to the mode converter discussed in this section. The parts 1 and 2 are extra tapers which fit into a rectangular waveguide with different dimensions.

SUMMARY

In this chapter, we have described the design of an active switching element composed of a Tee junction with an active window and a movable short plane connected to the 3rd port. The S-matrix of this element before and after switching can be adjusted by the coupling in the 3rd port of the Tee, as well as the locations of the window and the short plane. If the *on* state loss of the module is given, the power handling capacity is basically determined by both the maximum allowable field in the window and the total number of carriers which can be generated in the window. We have also discussed the design of the circular waveguide Tee, which is composed of a rectangular waveguide Tee and 3 circular-to-rectangular mode converters.

CHAPTER 4: DESIGN OF THE MULTI-ELEMENT HIGH POWER MICROWAVE SWITCHES

A high power switch is, in general, composed of one or more active elements and an RF network to match the elements between the RF source and the load. Although a lot of research effort has been done to improve the power handling capacity of the active elements like semiconductor switches, the power level needed for some applications, such as high gradient accelerator structures, still exceeds the capacity of a single active element. Several switching schemes have been suggested [16, 22], so that the RF power can be distributed to the active elements, reducing the load on each element.

In this chapter, the discussion will be focused on switchable irises, which can be used in the active resonant delay line systems. The SPDT (Single Pole Double Throw) switches, which could be part of the active DLDS, will also be discussed.

4.1 SYNTHESIS OF THE SWITCHABLE IRIS

A high power switchable iris can be constructed using several schemes. One of the schemes is the parallel switch array. In this scheme, the input power is split and fed into an array of active elements; the transmitted and reflected power is then recombined, as shown in Figure 19. The coupling coefficients of the active element are the same as the whole system for both the *on* and *off* states.

The other two schemes employ a cascaded phase shifter. Figure 20 shows the synthesis of a cascaded phase shifter, which contains several serially connected active elements. When the active windows are turned on, each element provides a small phase change and the phase change adds up in the whole module. Each element may or may not be matched, but the whole module must be matched. Since the phase change in each element is small, the active window can be placed close to the standing wave nodes with

relatively low electric field, so the load on each window is much lower than the power flowing through the module.

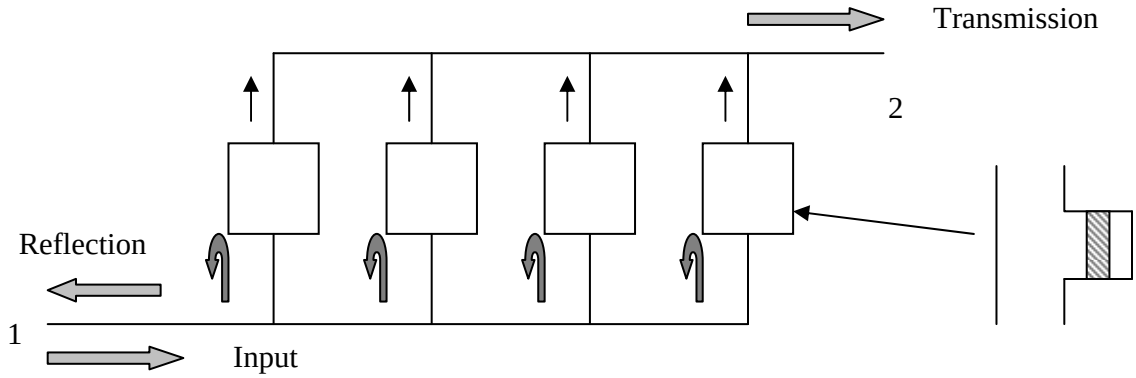


Figure 19. Parallel switch array

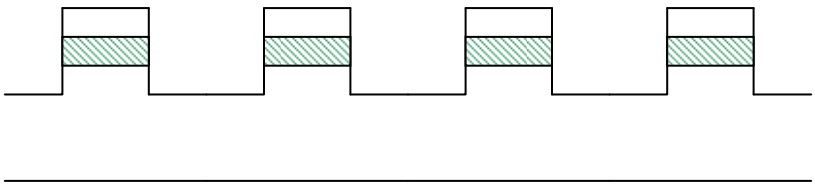
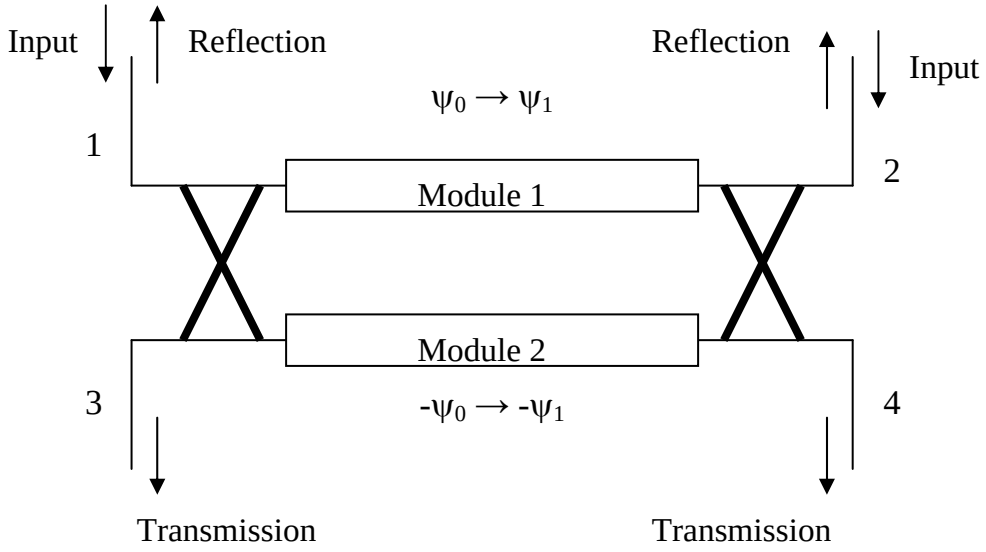


Figure 20. Active module for the cascaded phase shifter



When active window is *off*, modules have phase shift $\pm\psi_0$;
When active window is *on*, modules have phase shift $\pm\psi_1$.

Figure 21. Operation principle of the switchable irises with cascaded phase shifters and hybrids

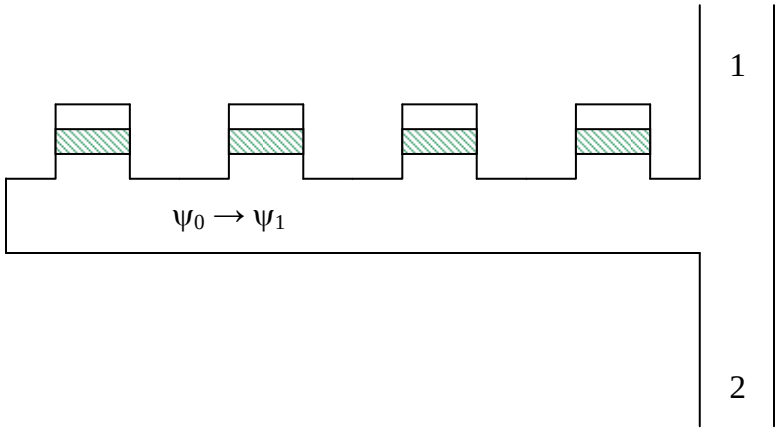


Figure 22. Switchable iris using a cascaded phase shifter as the third arm of a symmetric Tee

One scheme using the cascaded phase shifter is shown in Figure 21. The RF from the ports on the left side is coupled into the modules by a 3dB 90º hybrid, and then coupled

into the right side ports with another 3dB 90º hybrid. When module 1 has phase shift ψ and module 2 has phase shift -ψ, we can easily have:

$$\begin{aligned} V_2^- &= (V_1^+ e^{j\psi} - V_1^+ e^{-j\psi})/2 + j(V_3^+ e^{j\psi} + V_3^+ e^{-j\psi})/2 \\ &= V_1^+ j\sin\psi + V_3^+ j\cos\psi \\ V_4^- &= j(V_1^+ e^{j\psi} + V_1^+ e^{-j\psi})/2 + (V_3^+ e^{-j\psi} - V_3^+ e^{j\psi})/2 \\ &= V_1^+ j\cos\psi - V_3^+ j\sin\psi \end{aligned} \tag{4.1}$$

If the system is symmetric, i.e., port 1 and 2 are connected to two identical sources, port 3 and 4 are connected to two identical loads such as resonant delay lines,

$$\begin{aligned} V_1^+ &= V_2^+ \\ V_3^+ &= V_4^+ \end{aligned} \tag{4.2}$$

then

$$\begin{aligned} V_1^- &= V_1^+ j\sin\psi + V_3^+ j\cos\psi \\ V_3^- &= V_1^+ j\cos\psi - V_3^+ j\sin\psi \end{aligned} \tag{4.3}$$

the whole system is then equivalent to 2 identical irises with S-matrix

$$S = j\begin{pmatrix} \sin\psi & \cos\psi \\ \cos\psi & -\sin\psi \end{pmatrix} \tag{4.4}$$

When the phase shift ψ is changed by switching the active window, the S-matrix of the irises is switched. The equivalent RF power in one module is

$$\begin{aligned} P_{m1} &= P_{m1}^+ + P_{m1}^- \\ &= (P_1^+ + P_3^+)/2 + (P_2^+ + P_4^+)/2 \\ &= P_1^+ + P_3^+ \end{aligned} \tag{4.5}$$

which is equal to the equivalent input power for one iris. The total handling capacity of the two pair of iris ports is equal to the total power handling capacity of the two modules.

Another possible scheme to construct the switchable iris with a cascaded phase shifter is shown in Figure 22. The phase shifter is connected to the 3rd port of a Tee and shorted at the other end. The Tee is similar to the one used in the active element, as described in the previous chapter, but may have different parameters. If the cascaded phase shifter module has the total phase shift $\hat{\psi}$, the S-matrix of the system can be given by (3.11):

$$\hat{S} = \begin{pmatrix} \cos\dfrac{\hat{\zeta}-\hat{\phi}}{2} e^{j(\frac{\hat{\zeta}+\hat{\phi}}{2}+\hat{\alpha})} & j\sin\dfrac{\hat{\zeta}-\hat{\phi}}{2} e^{j(\frac{\hat{\zeta}+\hat{\phi}}{2}+\hat{\alpha})} \\ j\sin\dfrac{\hat{\zeta}-\hat{\phi}}{2} e^{j(\frac{\hat{\zeta}+\hat{\phi}}{2}+\hat{\alpha})} & \cos\dfrac{\hat{\zeta}-\hat{\phi}}{2} e^{j(\frac{\hat{\zeta}+\hat{\phi}}{2}+\hat{\alpha})} \end{pmatrix} \tag{3.11}$$

where

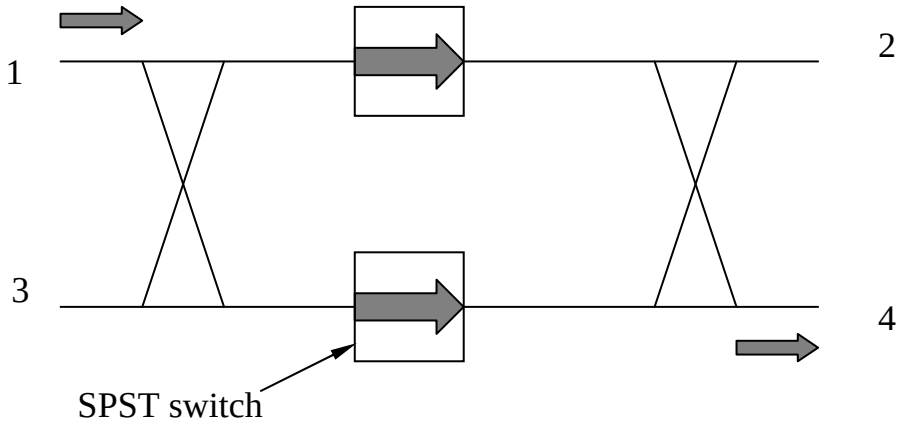
$$e^{j\hat{\zeta}} = \frac{-\cos\hat{\theta} - e^{j2\hat{\psi}}}{1 + e^{j2\hat{\psi}}\cos\hat{\theta}}$$

$\hat{\alpha}$, $\hat{\phi}$ and $\hat{\theta}$ are parameters of the Tee connected to the cascaded phase shifter, similar to those parameters given in (3.1). When the phase $\hat{\psi}$ changes, the scattering coefficients of the system will be switched.

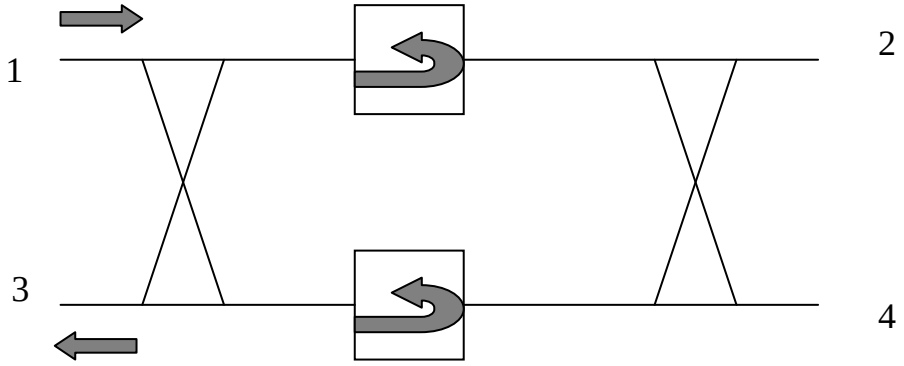
If $\cos\hat{\theta} = 0$, the S-matrix of the system will be

$$S = \begin{pmatrix} \cos\psi & j\sin\psi \\ j\sin\psi & \cos\psi \end{pmatrix} \tag{4.6}$$

The power handling capacity of the system will be the same as the power handling capacity of the module.



SPST switch full transmission



SPST switch full reflection

Figure 23. SPDT switch using SPST switches

4.2 SPDT SWITCH FOR ACTIVE DLDS

The SPDT switch can be constructed with SPST (Single Pole Single Throw) switches or cascaded phase shifters.

Figure 23 shows the operation principal of the SPDT switch using SPST switches. The input is fed from port 1 into two arrays of active elements through a 3dB hybrid. When the SPST switches are fully transmissive, the RF will go through the SPST switches and

be combined into port 4. When the RF is fully reflected back from the active elements, it will be combined into port 3.

The SPST switch can be just one active element if the element satisfies the power handling capacity. When higher power is required, a parallel active element array (as shown in Figure 19) can be used as one SPST switch. The total input power P_1 is equal to the sum of the power in the two SPST switches.

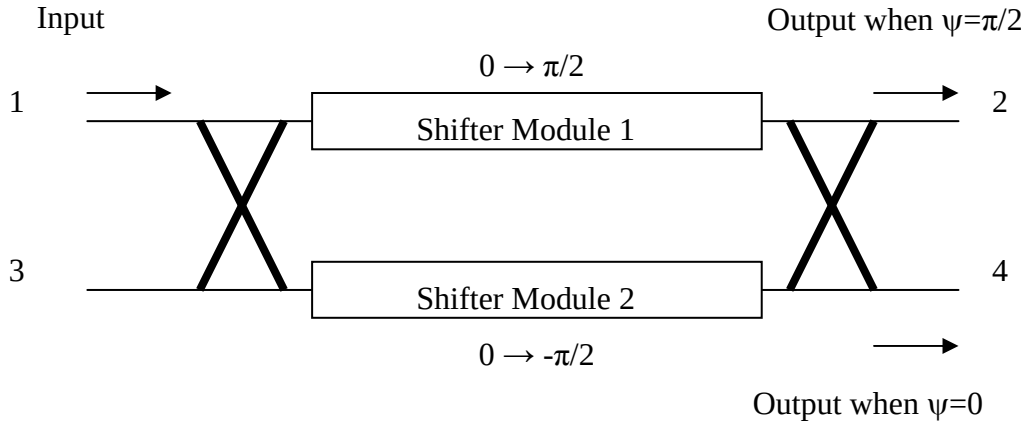


Figure 24. SPDT switch using cascaded phase shifters

The SPDT switch using cascaded phase shifters has the same construction as the switchable iris with hybrids; however, the input power is only fed into port 1. As a result of (4.1), when the modules have same phase shift ($\psi=0$), RF power will come out from port 4; when the modules have opposite phase shift ($\psi=\pi/2$), RF power will come out from port 2. Figure 24 shows the operation principal of the SPDT switch using cascaded phase shifters. The total input power P_1 is equal to the sum of the power in the two cascaded phase shifter modules.

4.3 THE CASCADED PHASE SHIFTER

As shown in Figure 20, the cascaded phase shifter module is composed of several active elements connected in serial. The active elements have two states. In one of the states, each active element is set to be matched by itself, and the total phase shift ψ is determined by the phase advance of each element. In the other state, each element is not matched, but the whole module is. In this case, the total phase shift of the module needs to be π (this will be shown later). If a certain total phase shift is desired, it can be adjusted with an additional length of waveguide.

In the case that the phase shift needs to be changed from ψ_0 to ψ_1, the module can have a phase shift π in the unmatched state, and phase shift $\pi + \Delta\psi$ in the matched state, where $\Delta\psi = \psi_1 - \psi_0$. The additional phase shift $\psi_0 - \pi$ can be provided by additional waveguides at the both ends of the module. Another possibility is to choose the unmatched state module phase shift 0, and $\Delta\psi$ in the matched state, with additional phase shift provided by waveguides. The range for ψ_0 and ψ_1 is $0 \le \psi_0, \psi_1 \le \pi/2$, and the range for $\Delta\psi$ is $-\pi/2 \le \Delta\psi \le \pi/2$.

The S-matrix of each element in the active module is

$$\hat{S} = \begin{pmatrix} \cos\dfrac{\zeta-\phi}{2} e^{j(\frac{\zeta+\phi}{2}+\alpha)} & j\sin\dfrac{\zeta-\phi}{2} e^{j(\frac{\zeta+\phi}{2}+\alpha)} \\ j\sin\dfrac{\zeta-\phi}{2} e^{j(\frac{\zeta+\phi}{2}+\alpha)} & \cos\dfrac{\zeta-\phi}{2} e^{j(\frac{\zeta+\phi}{2}+\alpha)} \end{pmatrix} \tag{3.11}$$

and

$$e^{j\zeta} = \frac{-\cos\theta - e^{j\Psi}}{1+\cos\theta e^{j\Psi}} = -\cos\theta + \frac{\sin^2\theta}{1+\cos\theta e^{j\Psi}} \tag{3.9}$$

In the state that each active element is matched, the matching condition is:

$$\zeta_1 = \phi + \pi \tag{4.7}$$

The phase advance in each element is $\phi + \alpha + \pi$. The total phase shift of *n* elements is

$$n(\phi + \alpha + \pi) = N\pi + \Delta\psi \tag{4.8}$$

N is an even integer when the unmatched state phase is 0, and odd if the unmatched state phase is π.

The solution of the equation will be

$$\alpha = (N\pi + \Delta\psi)/n - \phi - \pi \tag{4.9}$$

This condition can be satisfied by choosing an appropriate reference plane of the port 1 and 2 for the active element.

When the active element is not matched, the matching condition is given by the following.

We may introduce the transfer matrix A of a two-port network [35], which is defined as:

$$\begin{pmatrix} V_1^+ \\ V_1^- \end{pmatrix} = A \begin{pmatrix} V_2^- \\ V_2^+ \end{pmatrix} \tag{4.10}$$

On the other hand, the S-matrix of the two-port network satisfies:

$$\begin{pmatrix} V_1^- \\ V_2^- \end{pmatrix} = S \begin{pmatrix} V_1^+ \\ V_2^+ \end{pmatrix} \tag{4.11}$$

Solving the two equations, the transfer matrix A can be expressed using the elements of the S-matrix:

$$A = \begin{pmatrix} 1/S_{12} & -S_{22}/S_{12} \\ S_{11}/S_{12} & (S_{12}^2 - S_{11}S_{12})/S_{12} \end{pmatrix} \tag{4.12}$$

For a lossless two-port network like the one described by (3.11), the S-matrix is symmetric with determinant equals to 1. We can define $r = S_{11} = S_{22}$ and $t = S_{12} = S_{21}$. The transfer matrix can be also expressed as

$$A = \begin{pmatrix} 1/t & -r/t \\ r/t & (t^2 - r^2)/t \end{pmatrix} \tag{4.13}$$

The determinant of the transfer matrix is 1. For one cascaded phase shifter module containing *n* active elements, the transfer matrix is A^n, and the voltages of the two port network satisfies:

$$\begin{pmatrix} V_1^+ \\ V_1^- \end{pmatrix} = A^n \begin{pmatrix} V_2^- \\ V_2^+ \end{pmatrix} \tag{4.14}$$

If the whole module is required to be matched with phase shift χ, the transfer matrix needs to be:

$$A^n = \begin{pmatrix} e^{-j\chi} & 0 \\ 0 & e^{j\chi} \end{pmatrix} \tag{4.15}$$

The transfer matrix can be diagonalized as

$$A = U \begin{pmatrix} \lambda_1 & 0 \\ 0 & \lambda_2 \end{pmatrix} U^{-1} \tag{4.16}$$

where U is a unitary matrix, while λ_1 and λ_2 are the eigenvalues of A. So

$$A^n = U \begin{pmatrix} \lambda_1^n & 0 \\ 0 & \lambda_2^n \end{pmatrix} U^{-1} = \begin{pmatrix} e^{-j\chi} & 0 \\ 0 & e^{j\chi} \end{pmatrix} \tag{4.17}$$

When the element is not matched, A and U are not diagonal, then (4.17) can be satisfied only if χ=0 or π. If χ=0, (4.17) becomes

$$A^n = U \begin{pmatrix} \lambda_1^n & 0 \\ 0 & \lambda_2^n \end{pmatrix} U^{-1} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \tag{4.18}$$

The eigenvalues of the transfer matrix satisfies:

$$\begin{aligned} (\lambda_{1,2})^n &= 1 \\ \lambda_1 \lambda_2 &= 1 \end{aligned} \tag{4.19}$$

Solving the equations, we have

$$\lambda_{1,2} = e^{\pm j\frac{2m}{n}\pi} \tag{4.20}$$

where *m* is an integer and *n* is the total number of active elements in a module. However, *m* should not be an integer multiple of *n*, otherwise *A* will be a unit matrix and the element is matched.

Similarly, when the phase shift of the module is π, the eigenvalues are

$$\lambda_{1,2} = e^{\pm j\frac{2m+1}{n}\pi} \tag{4.21}$$

The trace of the transfer matrix conserves after diagonalization:

$$Tr(A) = \frac{t^2 - r^2 + 1}{t} = 2\cos\frac{M}{n}\pi \tag{4.22}$$

M is an even integer when the total phase shift is 0 and odd when the total phase shift is π; *M* should not be an integer multiple of 2*n*.

Now we can derive ζ_1 as a function of ψ. Substituting *r* and *t* with the values in (3.11) and (4.9), we can solve (4.22) for ζ_0 as:

$$\zeta_0 = \phi + \pi + 2\arctan\left(\frac{\cos\frac{N\pi + \Delta\psi}{n} - \cos\frac{M\pi}{n}}{\sin\frac{N\pi + \Delta\psi}{n}}\right) \tag{4.23}$$

$$\zeta_1 - \zeta_0 = 2\arctan\left(\frac{\cos\frac{M\pi}{n} - \cos\frac{N\pi + \Delta\psi}{n}}{\sin\frac{N\pi + \Delta\psi}{n}}\right) \tag{4.24}$$

To reduce the field in the active window, $|\zeta_1 - \zeta_0|$ needs to be minimized. For $0 \le \Delta\psi \le \pi/2$, $|\zeta_1 - \zeta_0|$ will be minimal when $M = N = 1$. If *n* is a large number, (4.24) is approximately

$$\zeta_1 - \zeta_0 = \frac{\Delta\psi}{n}(1 + \frac{\pi}{\pi + \Delta\psi}) \tag{4.25}$$

Similarly, when $-\pi/2 \le \Delta\psi \le 0$, $|\zeta_1 - \zeta_0|$ will be minimized when $M = N = -1$. In both cases, the module phase shift of the unmatched state needs to be π.

4.4 DERIVATION OF THE SCALING LAW

In this section, we will discuss the scaling law which determines the properties of the multiple-element switch systems such as the power handling capacity and the *off* state loss, especially concerning the dependence on the number of active elements.

The discussion in the previous chapter already gave the properties of the single active element. When the parameters of the active element are properly chosen, the power handling capacity of the active element is given by

$$P_{in} = \frac{AGL}{4R_s \sin^2(\frac{\zeta_1 - \zeta_0}{2})} E_{\max}^2 \tag{4.26}$$

Where ζ is the phase defined by (3.9), and E_{max} is the maximum electric field occurring at one surface of the window.

Under various switch setups which were discussed in section 4.1 and 4.2, the system power handling capacity will be the sum of the capacity in the switch modules, either the cascaded phase shifter module or the parallel switch array. The *off* state loss will also be the same as in one module. So in this section, we only need to compare the properties of one cascaded phase shifter module or that of the parallel switch array.

1. PARALLEL ACTIVE ELEMENT ARRAY

For a parallel array consisting *n* active elements, the S-matrix of the array is given by (3.11). The required change in phase ζ is half of the change in ψ, where $\cos\psi$ is the desired reflection coefficient of the system.

$$\frac{\zeta_1 - \zeta_0}{2} = \psi_1 - \psi_0 \tag{4.27}$$

The *on* and *off* state losses of the system will be the same as that of the single active element. Defining the *on* state loss for the system as L_0, we have

$$L_0 = \frac{P_{lon}}{P_{in}} = L \tag{4.28}$$

The *off* state loss using the thin window approximation will be

$$\frac{P_{loff}}{P_{in}} = \frac{4\sigma l R_s \sin^2(\psi_1 - \psi_0)}{L_0} \tag{4.29}$$

The power handling capacity will be the sum of the capacity from all the elements

$$P_{in} = \frac{nAGL_0}{4R_s \sin^2(\psi_1 - \psi_0)} E_{\max}^2 \tag{4.30}$$

2. CASCADED PHASE SHIFTER

For a cascaded phase shift module consisting *n* active elements, the change of phase ζ is given by (4.25) when $0 \le \psi_1 - \psi_0 \le \pi / 2$:

$$\zeta_1 - \zeta_0 = \frac{\psi_1 - \psi_0}{n}\left(1 + \frac{\pi}{\pi + \psi_1 - \psi_0}\right) \tag{4.31}$$

The *on* and *off* state losses from each active element in the module *L* will add up to the module's losses. The *on* state loss of the phase shifter module L_0 will be

$$L_0 = \frac{P_{lon}}{P_{in}} = nL \tag{4.32}$$

So the power handling capacity of one module is

$$\begin{aligned} P_{in} &= \frac{AGL_0}{4nR_s \sin^2(\frac{\zeta_1 - \zeta_0}{2})} E_{\max}^2 \\ &\approx \frac{nAGL_0}{R_s(\psi_1 - \psi_0)^2(1 + \frac{\pi}{\pi + \psi_1 - \psi_0})^2} E_{\max}^2 \end{aligned} \tag{4.33}$$

The *off* state loss will be

$$\frac{P_{loff}}{P_{in}} = n\sigma l \frac{2\sin^2\theta}{(1 + 2\cos\theta\cos\zeta_0 + \cos^2\theta)} Z_g \sin^2(\frac{\zeta_1 - \zeta_0}{2}) \tag{4.34}$$

or

$$\begin{aligned} \frac{P_{loff}}{P_{in}} &= \frac{4\sigma l R_s n^2 \sin^2(\frac{\zeta_1 - \zeta_0}{2})}{L_0} \\ &\approx \frac{\sigma l R_s s(\psi_1 - \psi_0)^2(1 + \frac{\pi}{\pi + \psi_1 - \psi_0})^2}{L_0} \end{aligned} \tag{4.35}$$

3. COMPARISON

The power handling capacities of the *n* element parallel array and cascaded phase shifter are given by (4.30) and (4.33). The ratio between (4.30) and (4.33) is shown in Figure 25.

$$P_{par} \Big/ P_{cas} = \frac{4(\psi_1 - \psi_0)^2(1 + \frac{\pi}{\pi + \psi_1 - \psi_0})^2}{\sin^2(\psi_1 - \psi_0)} \tag{4.36}$$

When $0 \le \psi_1 - \psi_0 \le \pi/4$, the cascaded phase shifter with *n* active elements will have slightly higher power handling capacity, as well as a lower *off* state loss. However, the

parallel array will be better than the cascaded phase shifter when $\pi/4 \le \psi_1 - \psi_0 \le \pi/2$. The ratio of the *off* state losses is the inverse of the ratio for the power handling capacity, and the parallel array will be also better when $\pi/4 \le \psi_1 - \psi_0 \le \pi/2$. Nonetheless, the cascaded phase shifter has other disadvantages. For example, the losses in the metal parts of one active element were not considered in the previous discussion. These losses will not scale as the losses on the active window, part of them will be constant numbers. The losses will add up for the *n* elements in the cascaded phase shifter, but not in the parallel array. The cascaded phase shifter is also more sensitive to disturbances in parameters, which results in a strict tolerance requirement. Given these drawbacks, the parallel active element array should be a better choice, even when $0 \le \psi_1 - \psi_0 \le \pi/4$.

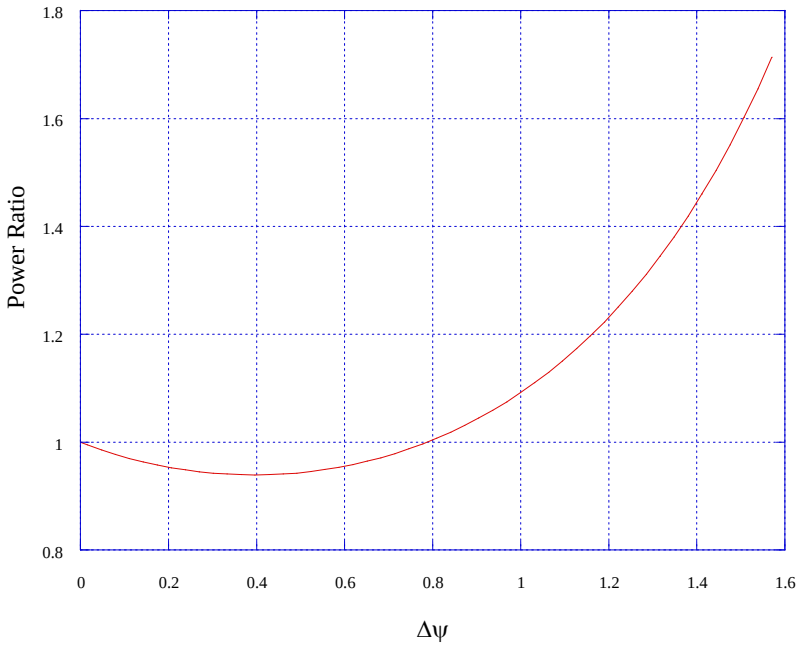


Figure 25. Ratio of power capacity between parallel array and cascaded phase shifter

Inverting (4.30), we can get the number of elements required for a parallel switch array:

$$n = \frac{4R_s \sin^2(\psi_1 - \psi_0)}{AGL_0 E_{\max}^2} P_{in} \tag{4.37}$$

If the thickness of the conducting layer is optimized as one skin depth, combining with eq. (3.48), the power handling capacity can be written as

$$P_{in} = \frac{GL_0 nNe\mu_{eff}}{2\sin^2(\psi_1 - \psi_0)} E_{\max}^2 \tag{4.38}$$

where N is the number of carrier pairs in one active element. The total number of carrier pairs in all the active elements required for the *on* state is

$$nN = \frac{2\sin^2(\psi_1 - \psi_0)}{GL_0 e\mu_{eff} E_{\max}^2} P_{in} \tag{4.39}$$

4.5 SUMMARY OF THE SCALING LAW

The scaling laws can be summarized as the following:

- In general, the parallel switch array configuration is preferred compared to the cascaded phase shifter. In some cases, the parallel switch array needs less active elements and has less loss during the *off* state; in the other cases, the parallel switch array needs slightly more active elements and a little bit higher losses from the windows, but it may have lower losses from the Tees and waveguides.

- The power handling capacity of the parallel switch array is the sum of the capacities of all the active elements in the array. The power handling capacity of the parallel array is proportional to the total number of carrier pairs generated in the multiple active elements.

- For a given target of power handling capacity and acceptable *on* state loss, the number of elements is proportional to the surface resistance, and inversely proportional to the square of the limit of the peak E-field.

- The total number of carrier pairs required for the *on* state is inversely proportional to the square of the limit of the peak E-field. It's necessary to choose a material and design which can sustain high electric field, as the active window.

- Once the material and the peak E-field is chosen, the capability of carrier generation will determine the power handling capacity of the system. This will be the major challenge of the active window design.

- The number of elements or the required number of carrier pairs is independent of the waveguide impedance Z_g.

CHAPTER 5: DESIGN AND IMPLEMENTATION OF THE ACTIVE WINDOW

5.1 INTRODUCTION

In this chapter, we will discuss the physics and implementation of the active waveguide window, which is the key component of the active element discussed in previous chapters. The window performs switching based on the bulk effects in the semiconductor. The performance of the active element is basically determined by the change in the number of carriers during the switching. The switching time needs to be a fraction of the desired output pulse width, which is a few hundreds nanoseconds.

In Chapter 1, we have introduced two types of semiconductor switches. One is the optically controlled switch by Tantawi [13], and the other is the electrically controlled switch by Tamura and Tantawi [22]. The optical switch in [13] has a fast switching time of several nanoseconds, but requires a 100mJ laser, which would be very expensive.

Tamura's switch window operates under the TE_{01} mode in a circular waveguide. This mode has no radial electric field and no azimuthal magnetic field; hence, a small gap in the waveguide will not lead to RF leakage without the choke structure. The switch was able to handle multi-megawatts of RF power. The power handling capacity is mainly limited by the maximum electric field the switch can sustain in the waveguide. Ref [22] also details the scaling laws for combining a set of these switches. However, the device described in [22] only demonstrated the possibility of using such technology with ultra-high power microwave systems. This device was too slow for a pulse compression application and had high losses.

We have developed a new switch based on injecting the carrier at the surface of a silicon wafer using an array of PIN surface diodes. The switch is designed to work at X-band, but is possible to scale into other frequencies. This switch is fast enough and its losses are

low enough for pulse compression applications. The fabrication process for the PIN diodes is compatible with the popular CMOS IC process, so the unit cost should be moderate if it's produced in volume. The requirements on the driver for the solid state silicon switch are also looser than other options. A typical setup uses a 1kV 1kA pulsed power driver, which is cheaper and less complicated compared to the high voltage driver for the plasma switch or the high power laser for the optical semiconductor switch.

Our active switch window works in a circular waveguide under the TE_{01} mode, which is in common with the older Tamura design. However, we have chosen to use the planar structure PIN diodes, with both P and N doping on the front surface of the silicon window. The planar structure makes a shorter intrinsic region length possible, so the switching speed can be enhanced. When the planar diodes turn on, the injected carriers concentrate near the top surface of the silicon wafer, which can help to reduce the RF losses in certain cases.

In our design, the switching bias stays off during the charging phase of the pulse compression system and turns on to discharge the pulse, which is opposite to the older Tantawi and Tamura design. This choice has several advantages:

1. The charging phase is usually longer than the discharging phase, Turning the bias on at discharging phase will reduce the required current integral and the heat load.

2. The charging phase has more stringent requirement on losses compared to the discharging state, because the losses will be compounded with multiple reflections. The *off* state RF loss of the switch window is easier to be reduced to a satisfying level. In contrast, it needs more carriers and higher current integral to reduce the *on* state losses.

3. The Tamura design tried to apply a reverse bias to sweep off the carriers in the bulk silicon to perform the switching. When the carriers are extracted out, a space charge field will be generated due to the separation of carrier pairs. To achieve fast switching, a strong reverse biasing voltage is needed to offset the space charge field. However, when

the field is strong enough, impact ionization will generate more carriers in the silicon and make the switching impossible. This limits the maximum speed of the switching. Tamura's switch has only achieved a switching time of about 1 millisecond, which is far from the requirement of the pulse compression systems.

In the rest part of this chapter, we will discuss the physics, design and fabrication of this electrically controlled RF switch. We will also discuss the physics of the optically controlled switch.

5.2 CARRIER GENERATION IN SEMICONDUCTORS

In an intrinsic semiconductor without doping, carriers can be generated in several ways: contact injection, impact ionization, photogeneration, and thermal generation. For an electrically controlled switch, contact injection and/or impact ionization are dominant. For an optically controlled switch, carriers are excited through photogeneration with a laser. Thermal generation is not an option to generate carriers in a fast and controllable manner; however, its reverse process thermal recombination determines the carrier lifetime, which is important for the switch design.

5.2.1 PHOTOGENERATION

When a semiconductor is illuminated by light, the photons can excite electron-hole pairs from the lattice if their energy is higher than the band gap. For monochromatic light, the carrier generation rate is proportional to the intensity of the light, as $G_L = I\alpha$, where α is called absorption coefficient and is strongly dependent on photon wavelength.

The absorption of each photon will generate one electron-hole pair. As the light travels through the semiconductor, $dI/dx = -G_L$. So the light intensity and carrier generation rate drop exponentially: $I = I_0 e^{-\alpha x}$, $G_L = G_{L0} e^{-\alpha x}$. $1/\alpha$ is the average penetration depth of light and the thickness of the generated carrier layer. When the wavelength is long and

the photon energy is close to the band gap, the absorption is weak and the value $1/\alpha$ is large.

Photogeneration can be very efficient if the carrier lifetime is long enough. The energy needed to generate one electron-hole pair is only a little more than the band gap energy, which is 1.12eV for silicon. If we need to build a switch as described in section 3.6, the total number of required carrier pairs will be $N = 3.4 \times 10^{15}$, which requires about 0.6mJ of energy. Conservatively considering several factors, such as the exponential distribution of carriers, slightly higher energy needed for the photon, and the reflection at the interface, the required energy should still be less than 10mJ. To generate a 300μm layer of carriers, the wavelength of the laser can be chosen at around 1040nm, so that the penetration depth of the laser and the thickness of the generated carrier layer will be close to the skin depth. Such a laser pulse is not hard to achieve. However, since the availability of laser wavelengths is limited, sometimes it's hard to find a matching wavelength for a certain desired penetration length. In such cases, a more intense laser pulse is needed.

In the proof of principle experiment made by Tantawi et al [13], a 100 mJ 532nm laser was used. The requirement of the strong pulse was due to the choice of wavelength. At 532nm, the penetration depth is close to 1.5μm. According to the discussion in Chapter 3, the required carrier density is inversely proportional to the square of the thickness of carrier layer, or the penetration depth; the total number of carriers is inversely proportional to the penetration depth. Nonetheless, the *on* state loss at the window can be smaller for such a strong pulse at a short wavelength; and the power handling capacity of the module can be higher if the module is optimized.

5.2.2 CONTACT INJECTION

Contact injection creates carriers in an intrinsic semiconductor with an externally applied electric field. This is the dominant carrier generation mechanism for PIN diodes with

forward bias. With the bias, the electrons and holes are separately injected into the heavily doped P/N regions through the metal-semiconductor contacts, then drift and diffuse into the intrinsic region under the biasing electric field.

A short intrinsic region is essential for fast injection since the carriers need to drift a shorter distance to reach the center and the other side of the diode. Also, the bias field can be higher in shorter diodes with the same bias voltage, which will result in a higher drift velocity. We have compared two diodes with the same volume. One is 60μm long, 50μm deep and 2mm wide, with contacts covering both of the 50μm□2mm surface, assuming infinite carrier lifetime; the other one is 200μm long, 50μm deep and 0.6mm wide. Simulation with a 2-D semiconductor device simulation tool Medici [30, 31] shows that after 150ns of 1A injection current, the carrier density at the center of a 60μm long diode reaches $6\square 10^{16}/cm^3$; in the 200μm diode, the carrier density can only reach $1.7\square 10^{16}/cm^3$ at the center, but is much higher at the both ends of the diode.

Another factor to be considered is the carrier diffusion length, which is the average distance carriers can diffuse into a sea of opposite carriers before been recombined. To avoid significant loss of carriers during the injection, the length of the diode must be less than the diffusion length. This is essential for fast switching and maintaining a relatively uniform carrier distribution at equilibrium. The diffusion length is closely related to the carrier lifetime: $L_D = \sqrt{\tau D}$, where D is the diffusion coefficient. For silicon under room temperature and low carrier density, $D_n \approx 35 cm^2/s$ for electrons and $D_p \approx 12 cm^2/s$ for holes. To achieve a diffusion length of 100μm for holes, the required carrier lifetime is about 8μs, which can be easily satisfied by the available silicon materials. The diffusion coefficient for Gallium Arsenide is approximately 10 times higher. However, usually the GaAs carrier lifetime is as short as 10ns, which is shorter than the desired output pulse width of the compression system, making GaAs not a suitable material for this switch. Such a short carrier lifetime also requires a shorter diode intrinsic region of several

microns, causing difficulties in our design of the active window (for example, the carrier layer will be too thin).

The carrier injection generates one electron-hole pair with each electron injected from the circuit. The current integral needed from the circuit is equal to the total charges of one kind of the injected carriers. For the switch as described in section 3.6 with the number of carrier pairs $N = 3.4 \times 10^{15}$, the switching needs to inject 0.6mC of charges. Given the non-uniformity of carrier density and the limited carrier lifetime, the actual required current integral will be several times higher. To achieve 1μs switching time, several kilo-ampere of current is needed. Given the serial resistance in the circuit, a bias voltage of more than 1 KV is needed.

5.2.3 IMPACT IONIZATION

When the electric field in a semiconductor is above a certain value, the carriers can gain enough energy so that electron-hole pairs will be excited when the carriers collide with the semiconductor lattice. This phenomenon is called impact ionization. The electron impact ionization rate α_n is defined as the numbers of electron-hole pairs which can be generated by one electron traveling one unit length, while α_p is similarly defined for holes.

The ionization rates are strongly dependant on the electric field. When the field is high enough and one carrier can excite more than one electron-hole pair before it annihilates or is extracted by the circuit, the carrier density and the current in the semiconductor can increase exponentially, which can lead to avalanche breakdown.

The impact ionization makes it possible to generate carriers more efficiently. Each carrier injected from the contact is able to generate a lot of carriers. This reduces the current needed, as well as the voltage drop on the serial resistance.

Impact ionization can happen in both the forward and reverse biased PIN diodes during switching. For the forward biased diode, the impact ionization from the biasing field is minimal, since the majority of the bias voltage is dropped on the serial resistance and the space charge field. However, when strong RF power is applied, the field can be strong enough to cause, or assist the impact ionization. When the diode is reversely biased, ionization can happen when the bias voltage is high enough to breakdown the diode. The breakdown voltage for a PIN diode is about proportional to the length of the intrinsic region. For a diode with 60μm length, the breakdown voltage is approximately 2KV.

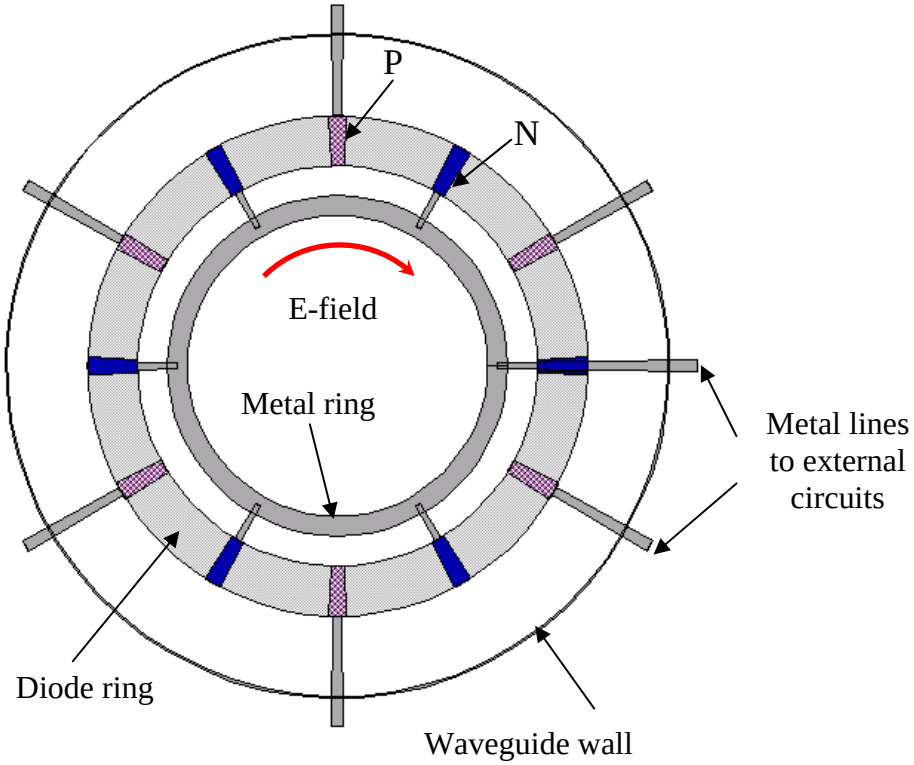


Figure 26. Schematic top view of the active window

The actual number of the PIN diodes is much larger.

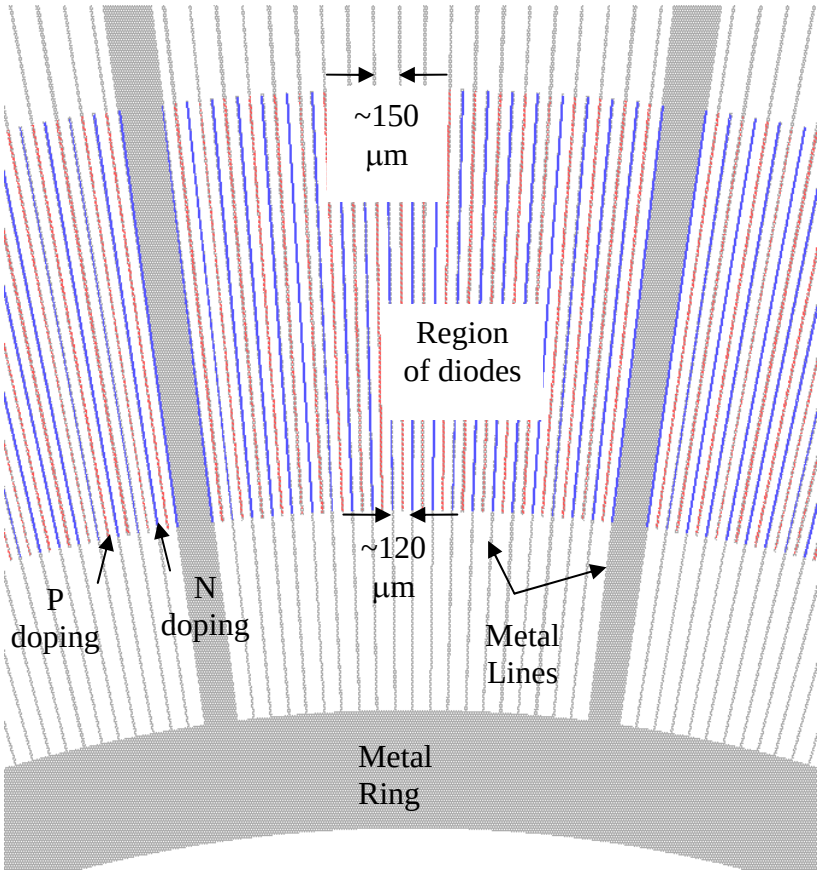


Figure 27. Detail top view of the diode region on the active window

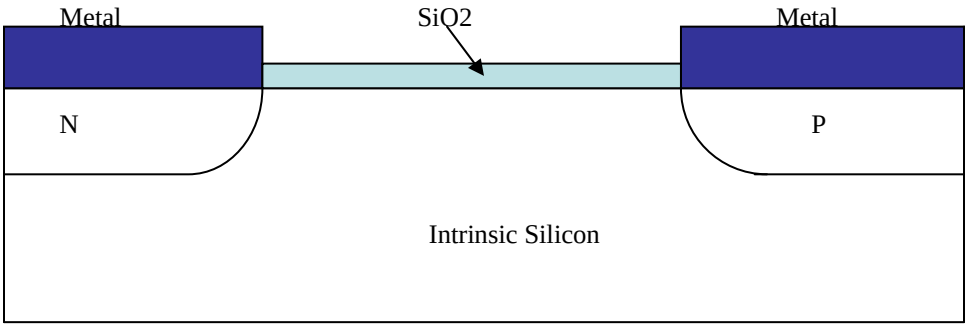


Figure 28. Schematic view of the cross-section in the PIN diode

5.3 DETAIL OF THE DESIGN AND SIMULATION OF THE ELECTRICAL CONTROLLED ACTIVE WINDOW

5.3.1 OVERVIEW OF THE WINDOW DESIGN

In this section, we will discuss the design and the properties of the electrically controlled active window we have actually fabricated. As noted in the previous discussion, this window was fabricated from a high purity silicon wafer, with very high resistivity for low loss and very long carrier lifetime. The carriers are generated by forward biased PIN diodes, mainly through contact injection. The diodes are integrated on the silicon wafer, as illustrated in Figure 26 and Figure 27. The thickness of the available wafers is 525μm, which is much larger than the desired length for a fast switching PIN diode. To make the diodes shorter, the diodes were built with a planar structure, with both P and N doping regions on the same side of the active window, which is shown in Figure 28.

To reduce the number of carriers required for switching, the diodes only cover a small ring shape region on the window, at the peak E-field radius. There is a small metal ring inside the diode ring, which can help to reduce the required number of carriers. The metal ring also matches the window during the *off* state, and serves as a feed for the biasing of the diodes.

The wafer - or the active window - is inserted into a circular waveguide under the TE_{01} mode. As mentioned before, the field direction under this mode allows a gap in the waveguide without serious leakage, so the wafer can be inserted the gap. Several holders were also designed to accommodate the active window, with different inner diameters.

5.3.2 ELECTRICAL DESIGN

The active window is controlled by the injection of carriers from the forward biased PIN diodes. The length of the diode (the distance between the P and N regions) is chosen at about 60-75μm. The length is variable because the two sides of the diode are not parallel.

We have also made a version of switch with about 100μm diode length, which has been experimentally proved to be slower. Although a shorter diode length is desired for fast switching, the improvement is less significant when the length is short enough. The length of the diode is also proportional to the depth of the diode, which needs to be optimized so that the number of carriers required for switching is minimized. The minimum length of the diode is also limited by other factors such as the minimum metal line width determined by both the process technology and the current in the line.

The P and N regions of the diodes are lines in the radial direction, which is parallel to the magnetic field in the TE_{01} mode, so the lines will not cut the magnetic field and have little effect on the RF properties. The diode region forms a ring on the wafer instead of covering the whole wafer, so the length of the diodes can be kept close to constant, and the current density along the radial direction does not vary a lot. The inner and outer radii of the diode ring are 10mm and 12.5mm respectively, which are determined from the RF simulation to minimize the required number of carriers. The numbers of the diodes and bias lines are very large. For the 60-75μm design, the number of diodes is 960, with each diode covering 0.345° in total; the length of the diode is 60μm on the inner side and 75μm on the outer side. The metal lines covering the P region are extended out to a group of metal pads which can be connected to the bias circuit, while the P lines are extended to a metal ring inside the ring of diodes. Each of those metal lines covers 0.06°. There are 24 more radial lines connecting the metal ring to the edge and back of the wafer. These lines cover 1.2° each. The details of the diode ring are shown in Figure 27. This biasing layout avoids the crossing of bias lines, which is quite difficult with high operating voltage and current. The metal ring will have some effect on the RF property, which will be discussed later.

The electrical property of the diode is simulated with Medici, while the device profile is simulated with 2-D process simulation program TSuprem-4 [32]. The final version of the process used to build the device as well as in the simulation is listed Table 4. Figure 29

shows the simulated carrier distribution at different time after the current is injected. In the simulation, the diode has a 2.4m total length, which is the sum of the 960 diodes. A 1 kilo-ampere current source with 10ns rise time is used for biasing.

From the results, a carrier layer of 2-30μm with $1\square 10^{17}$ carrier density can be generated in 200ns, and it will grow to 3-40μm in 300ns.

5.3.3 HOLDERS FOR THE ACTIVE WINDOW

Several holders are designed to provide support and bias to the active window, with different inner diameter of 1.299 inch, 1.5 inch and 1.6 inch. Since the 1.5 inch circular waveguide is the most widely used in the lab, the 1.299 inch holder has a taper section to adapt to 1.5 inch waveguide. The drawing of the 1.299 inch holder is shown in Figure 31. The major parts of the holders are similar, except for the diameters. The holders were designed by Gordon Bowden, and the drawing was accomplished by Robert Reed.

The bias voltage is applied between the two parts of the holder. The upper part of the holder (part 4 in the drawing) has 24 gold plated contact springs, which will provide electrical connection to the P regions through the 24 pads on the active window. The contacts for the N regions are on the back and edge of the active window. The two parts of the holder are isolated by a ceramic spacer. Two O-ring seals on both sides of the spacer can provide vacuum sealing. The bolts securing the two parts of the holder are insulated with delrin bushings.

Due to the concern of a possible breakdown caused by the high voltage bias, the initial design left a gap of approximately 5mm between the upper and lower parts of the holder. Reflection has been measured from such a holder. In a revised design, the gap between the holders is minimized to about 2mm to reduce possible RF reflection and leakage.

5.3.4 RF PROPERTIES

In chapter 3, we have discussed the RF properties of the active window with a uniform carrier density. The properties of our actual window is different from the uniform window, since the carriers only cover a ring on the window, and there is a metal ring cutting the magnetic field of the TE_{01} mode. The carrier layer in the diode ring is about 50μm deep, which is also much thinner than the wafer, due to the planar diode structure.

Simulation has been done with HFSS to optimize the parameters, especially the locations of the metal ring and the diode ring. The target of the optimization is to use the minimum number of carriers to perform the switching, without significantly increasing the field or losses during the *off* state under comparable conditions. The metal ring can increase the reflection during the *on* state and reduce the required number of carriers, while matching the active window during the *off* state. The matching of the active window will not help to significantly improve the loss or power handling capacity. However, with a matched window, the relationship between the 3rd arm phase change ΔΨ of the switch and the location of the short plane in the back is linear, so the tuning of the system can be easier. This matching also opens the possibility to use the switch window without the three port network in certain applications that need full transmission in the *off* state. In the optimization, an inner diameter of 1.299 inch was used, since it requires fewer carriers and makes the proof of principal experiment easier, at the cost of the lower power handling capacity. Some of the results and comparisons are given below.

First, the window is simulated in an ideal case without a gap in the waveguide, and the window is inserted in a waveguide with both sides open to excitation. The wafer is 525μm thick, with a resistivity of 5KΩcm. The diode ring is 2.5mm wide and 50μm in depth, filled with carrier pairs at $1\square 10^{17}/cm^3$ (the corresponding conductivity is 1610 Siemens/m) during the *on* state. The total required number of carrier pairs is $8.8\square 10^{14}$. During the *off* state, the window is matched with the metal ring having an inner radius of 8.1mm and an outer radius of 8.8mm; the reflection coefficient S_{11} is close to 0.1. The

loss is 1.8% if the metal ring is lossless; if the metal ring is made of aluminum, it will add 0.6% to the loss. When the switch is *on*, S_{11}=0.953 and S_{12}=0.150, with 6.8% loss. If the window has a maximum E-field of 1×10^7V/m, the equivalent power handling capacity is about 12MW; if the maximum field is the DC breakdown field of 3×10^7V/m, the window can handle about 100MW of equivalent power.

We then simulated the case that one side of the waveguide is terminated with a short plane. The short is at the position so that the phase change is $\Delta\Psi = \pi$ after switching. The field at the window is twice of the traveling wave. For the window with the metal ring and the diode ring, the simulated *on* state has a loss of around 7%, while the *off* state comes with a loss of 8.2% if the metal ring is lossless. If the metal ring is aluminum, the *off* state loss will increase to 10.6%, approximately 4 times of the one-pass case. In the case that the ring is made of copper, the *off* state loss will be reduced slightly. Waveguide wall losses are not considered in the simulation.

As a comparison, we have simulated the case for a window with uniform carrier density and no metal ring. When both ends of the waveguide are waveports, the window has a very strong *off* state reflection, with S_{11}=0.94 and very little loss. When the short plane is added to provide the 3rd arm phase change of $\Delta\Psi = \pi$, the *off* state loss in the window is 6.1%, slightly better than the window with the metal ring. The maximum field is about 7% less than the case with the metal ring, which means approximately 14% more power handling capacity. When the window is turned *on* with carrier pair density at 3×10^{15}/cm^3 (conductivity is 82S/m) in the whole wafer, the loss is 6.5%. The required number of carrier pairs is 1.35×10^{15}.

We have also simulated the active window in the actual holder with a 2mm gap. The difference is negligible compared to the simulation without a gap. For the holder with a 5mm gap in the one-pass setup, the *off* state reflection is significant. The *on* state loss is also larger, which will be 7.6% excluding wall losses. If the wall losses are included, it

will be even higher. To match the window, the location of the metal ring needs to be adjusted again.

To reduce the *off* state loss further, wafers with a higher resistivity of 100KΩcm can be used. In the one-pass case, the *off* state loss is only 0.1% when the metal ring is lossless. With an aluminum metal ring, the loss will be 0.7%. In the case that a short plane is attached to achieve a phase switching of $\Delta\Psi = \pi$, the *off* state loss is only 0.4% when the metal ring is lossless. With an aluminum metal ring, the loss will be 2.8%.

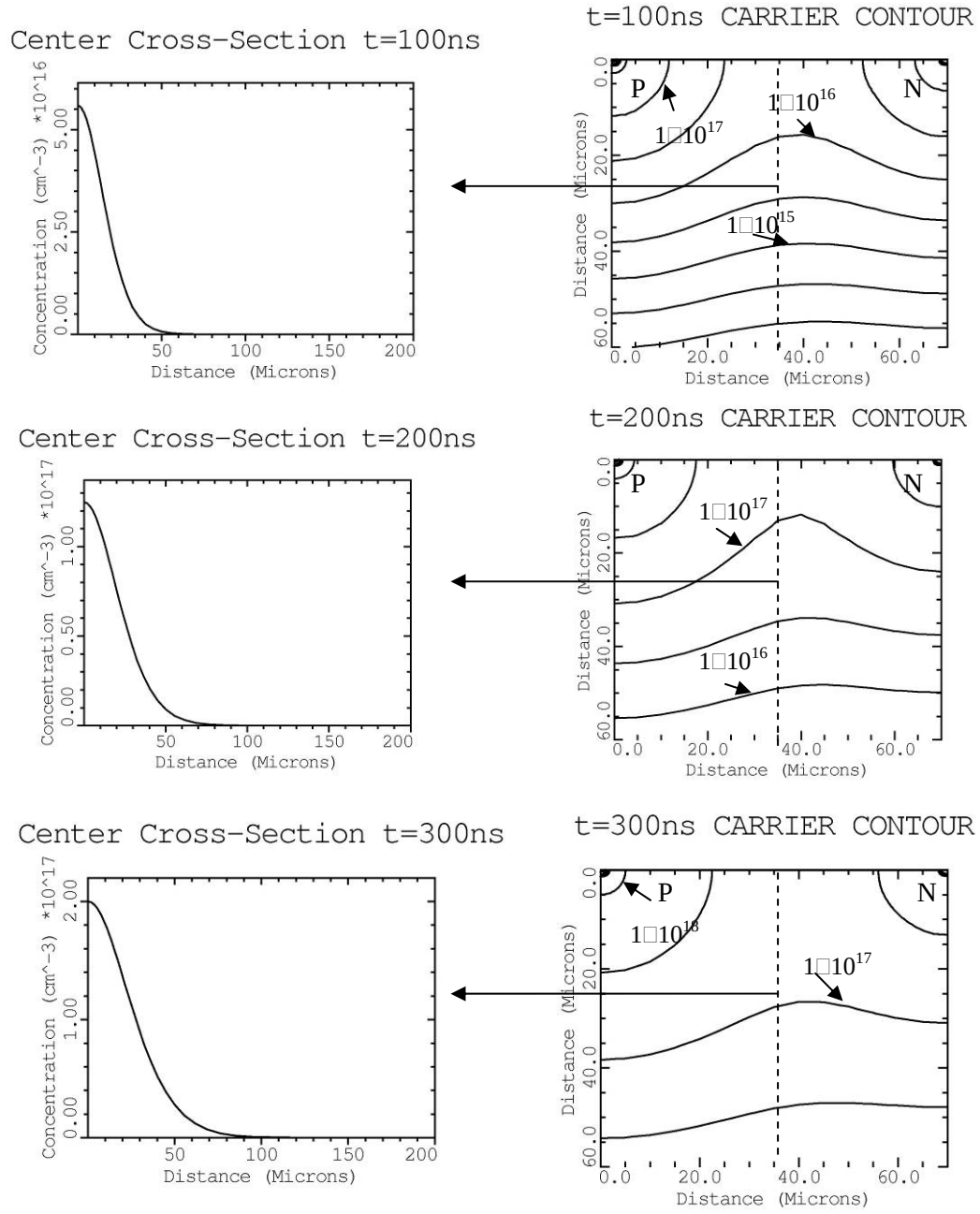


Figure 29. Simulation results of the carrier distribution in the diode at different times

The right side is the 2-D carrier distribution contour in the cross-section.

The left side is the distribution in the center cross-section of diode

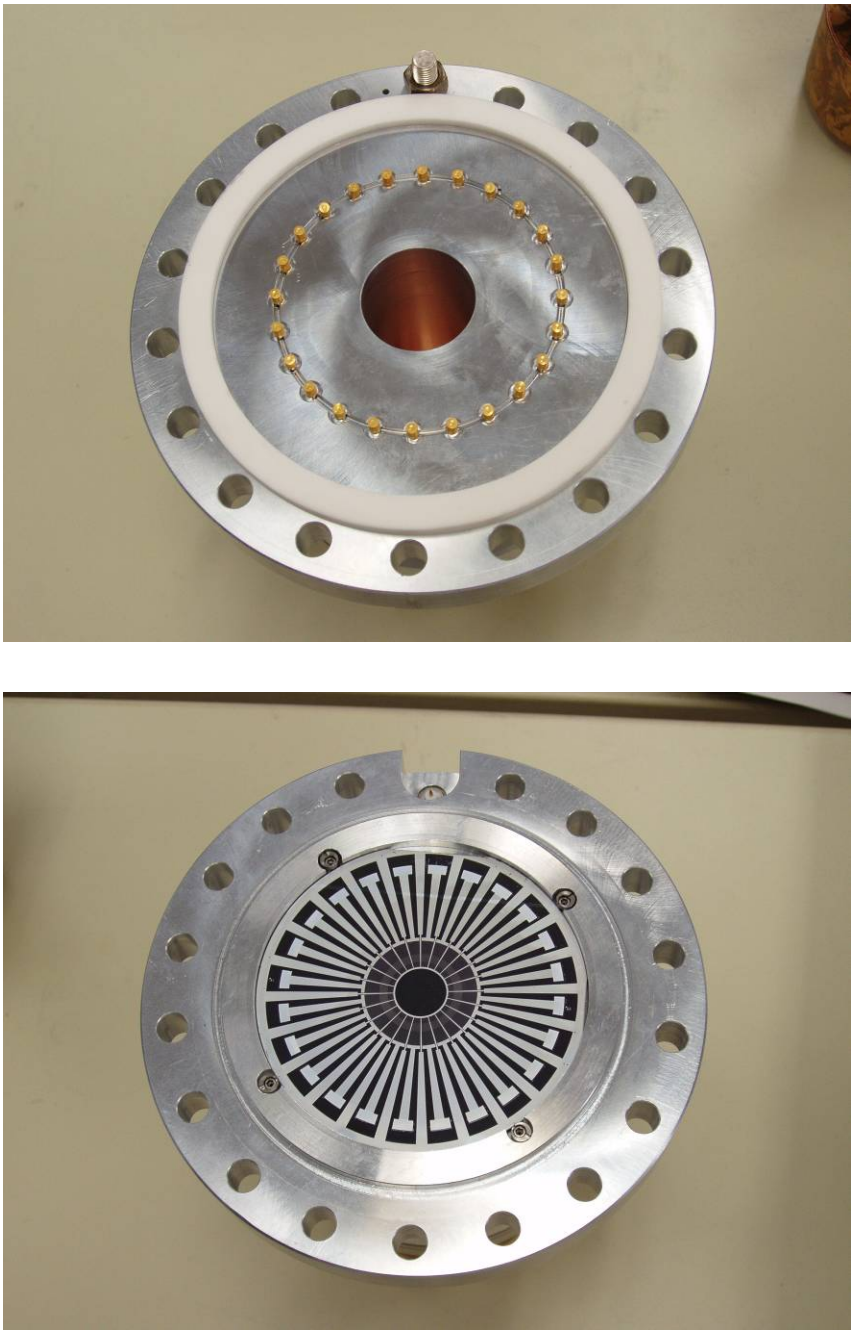


Figure 30. Photos of the two halves of the window holder with an active window

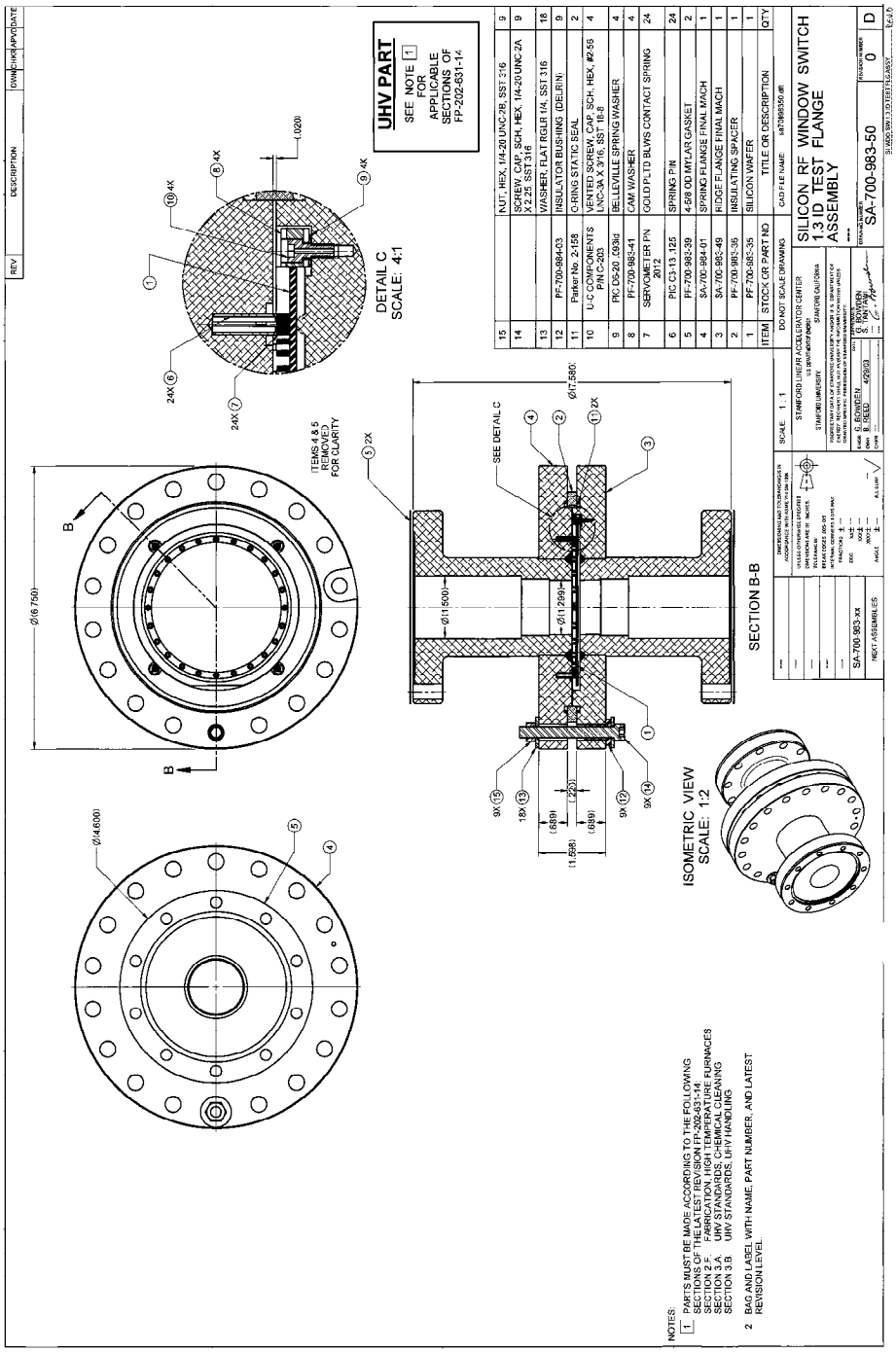


Figure 31. The wafer holder with 1.299 inch diameter and the taper

5.4 DEVICE PROCESS FLOW

The fabrication process for the switch window structure is quite similar to the standard CMOS process used for IC production. This ensures a moderate unit cost if it will be fabricated in volume. The fabrication is mostly completed at the Stanford Nanofabrication Facility (SNF) by the author. Several cycles have been completed in the past few years, and revisions were made after each cycle according to test results. The latest version of the process flow is provided in Table 4. Details such as wafer cleaning and photoresist coating/exposure/developing are not listed.

The fabrication starts with a high resistivity silicon floatzone wafer. We have used several different batches of wafers from different vendors, with resistivity higher than 5000Ωcm. For most of the wafers, the thickness is around 500μm and the wafer is polished on both sides. The latest batch of wafers is produced by Cemat Silicon S.A., with the ingot from Tianjin Huan Ou Semiconductor Material Co. The wafers have >90KΩcm resistivity and >5000μs carrier lifetime. The thickness of the wafer ranges from 513μm to 526μm, and the wafer is single-side polished.

A thermal oxide layer is generated first on the silicon surface in steam ambience. The target thickness is 0.6 micron. Then mask 1 is defined on 1μm photoresist with photolithography. The photolithography uses Karlsuss MA-6 contact aligner for exposure, with up to 0.75 micron resolution. The exposed oxide is then etched away with Applied Material P5000 plasma etcher. We have chosen plasma etching because of the better resolution resulting from the better directivity. After etching the oxide layer in the N region, phosphor ions are implanted at 40keV. The implantation job can be done either at SNF by an SNF staff, or at an outside vendor. If necessary, the implantation can be done with the photoresist stripped, since the oxide layer is thick enough to stop the ions. Thereafter, similar photolithography and etching processes are applied with mask 2 to form the P region, followed by boron implantation. An anneal process is required after

implantation, so the dopants can be activated by occupying the substitutional sites in the lattice, and the bonds broken by the high energy ions can be repaired.

Mask	Process Steps
	Wet oxidation at 1100 ºC for 50 minutes plus ramp time, generates ~6000Å thermal oxide
Mask 1	Definition of the N region and alignment marks with photolithography
	Dry etch oxide at the N region
	$5\square 10^{14}/cm^2$ Phosphor implantation at 40keV
Mask 2	Definition of the P region with photolithography
	Dry etch oxide at the P region
	$5\square 10^{14}/cm^2$ Boron implantation at 40keV
	Anneal at 950ºC for 1 hour
	Backside metallization: sputter 2μm Al
Mask 3	Definition of backside metallization
	Wet etch of backside metal
	Frontside metallization: sputter 0.1μm of Ti and 1.5μm of Al
Mask 4	Definition of frontside metallization
	Dry etch of frontside metal
	Deposit 3μm of SiO_2 passivation layer
Mask 5	Definition of contact pads
	Wet etch SiO_2 to form contacts

Table 4. Brief process flow of the active window

The energy of the ion implantation is chosen at a minimum level for the implanter, so the dopant density near the contact surface will be high enough without a long diffusion process. The dose has to be high enough to form the Ohmic contacts, but low enough so

that the anneal process can be done with a short time and at a low temperature. A long anneal process will diffuse the dopant deep into the silicon, causing significant RF losses. Higher loss has been observed in earlier versions of switches with $5\square10^{15}/cm^2$ dose and 1 hour anneal at 1100ºC. Currently the doses for both Boron and Phosphor implantation are chosen at $5\square10^{14}/cm^2$, followed by 1 hour anneal at 950ºC, which reduces the RF insertion loss significantly. Doses as low as $1\square10^{14}/cm^2$ also works according to our simulation.

After the anneal process, the wafer is metallized. The backside of the wafer is metallized first, which will provide a negative bias from the backside of the switch holder, connecting to the front side with the metal on the edge of the wafer. 2μm of aluminum is sputtered on the backside of the wafer, then defined with mask 3 and wet etched. The front side metallization is accomplished after the backside. At first 0.1μm of Titanium is deposited, then 1.5μm of Aluminum. The Titanium can form a uniform layer of alloy with silicon, which will prevent the formation of an Al spike into Si. The Al spike is harmful because it will cause a non-uniform current density at the contacts, and therefore the current capacity of the diodes will be reduced. After mask 4 is applied to define the metal lines, the unwanted metal is etched away with plasma etching. Although we prefer thicker Al for better current conductivity, the thickness is limited by the plasma etcher we use. In the future, it could be possible to replace the aluminum with copper, which would reduce the RF loss.

A SiO_2 layer is deposited with Plasma Enhanced Physical Chemical Deposition (PECVD) to protect the metallization. Compared to other methods at similar temperature, PECVD provides the densest SiO_2. Finally, the contacts are defined with mask 5. After the SiO_2 over the contacts is wet etched away, the fabrication is completed, as shown in Figure 32.

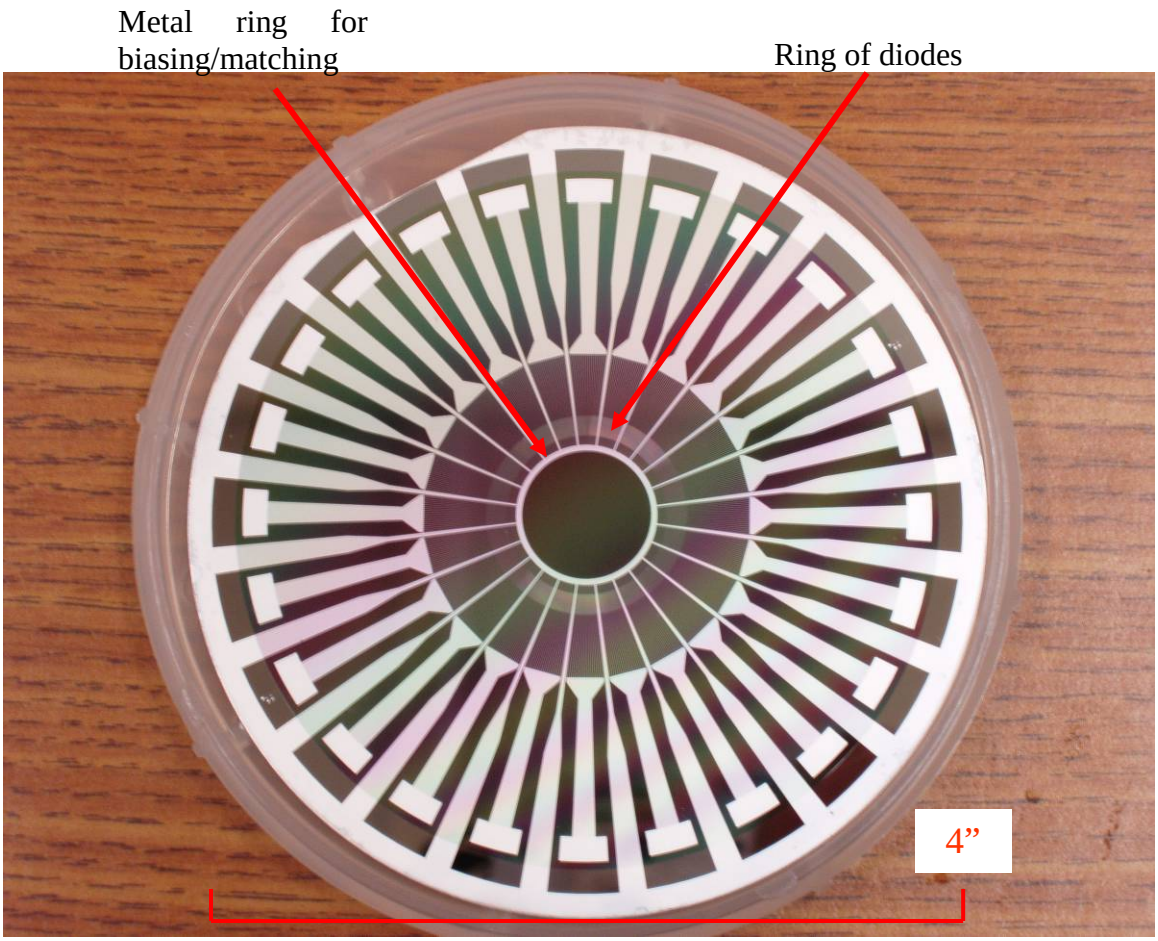


Figure 32. The active window fabricated on a 4” wafer

5.5 CIRCUIT DRIVING THE ACTIVE WINDOW

We have built an IGBT pulsed current circuit to power the window. The circuit diagram is shown in Figure 33. IGBT transistors are driven by an IGBT driver. When the driver turns on the IGBT, the cathodes of the PIN diodes are virtually grounded, so the high voltage drop will apply on the diodes quickly, until the current picks up. Inductance in the circuit is tightly controlled to reduce the current rise time. IXYS EVDD408 or EVDD414 evaluation boards are used as the driver for IRGPS60B120KD IGBT transistors. The EVDD408 can drive 2 IGBTs and EVDD414 can drive 4. The current output of this circuit is monitored by one 0.17Ω low inductance resistor on each board.

With 1KV over the IGBT and the load, each IGBT can provide a current of around 250A, with rise time of 3-40ns. Usually 2 boards are used to provide 1-1.5KA, but more boards can be used for faster switching, as long as the window can sustain the current. The current monitor resistors can be also removed to reduce unnecessary voltage drop.

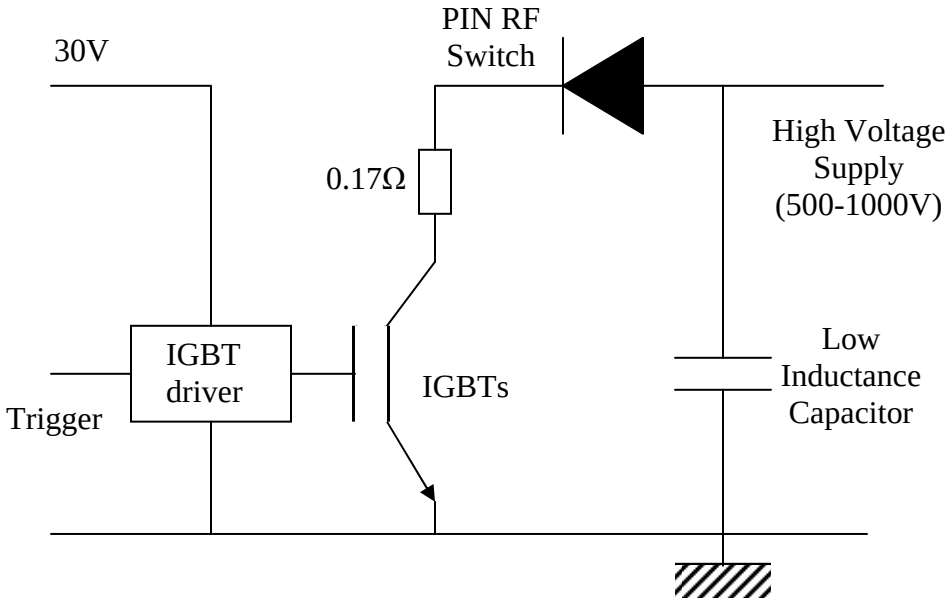


Figure 33. The circuit driving the active window

SUMMARY

In this chapter, we have discussed the physics of carrier generation and the design of the electrically controlled active window based on a PIN diode array.

- The active window is built on a silicon wafer with 525μm thickness. The resistivity of the wafer is up to 90KΩcm. The diameter of the window is 1.299 inch.

- There is a metal ring on the window. It matches the window when the diodes are off; during the *on* state, it provides bias to the diodes and helps reflection. The

number of carriers required for switching is reduced with the help of the metal ring. The metal ring will contribute to about 0.6% of single trip RF loss, and lower the power handling capacity by 14%.

- The window consists of 960 PIN diodes, covering a ring on the window. The diodes are located on one side of the window, with a length of 60-75μm.

- The diodes are forward biased when the switch turns *on*, resulting in the full reflection of the window. The simulated turn on time is about 2-300ns with 1000A driving current, depending on the requirement of *on* state loss.

- The active windows were built by the author at the Stanford Nanofabrication Facility (SNF). The process of the windows is based on the CMOS compatible technology, which is commonly used in the IC industry.

- The RF supporting structure was designed and built. The structure provides support and bias to the active window.

- The pulsed biasing circuit was built with the IGBT. The circuit can provide at least 500A with 3-40ns rise time. Several of such circuits can be used in parallel, providing a pulsed current of more than 1KA.

CHAPTER 6: LOW POWER EXPERIMENTS

In this chapter, we will present the low power testing results of the active window. First, the low power characterization of the active window switches will be presented. The characterization of the circular waveguide Tee will also be discussed. The characterization includes two types of tests, network analyzer measurements and low power active switching tests. The network analyzer (NWA) measurements will give the passive characteristics of the switches during the *off* state. The active switching test will examine the switching performance of the switches. Each type of the test uses two different setups, the one-pass setup and the switch module setup. The one-pass setup is used for characterizing the switch in the supporting RF structure. The switch module setup attaches the circular waveguide Tee to one end of the window switch holder and a movable short plane to the other end, so the reflection coefficient of the module can be tuned. In the active pulse compression test which will be discussed in the next chapter, such a module setup is used. The characterization of the circular waveguide Tee uses only the NWA measurement. This characterization includes the measurement of the S-matrix of the 3-port network, and the measurement of the setup with the symmetric port terminated at different positions.

After the characterization tests, the active resonant delay line pulse compression experiment was carried out with the switch module. This experiment will prove the principle of active pulse compression, using the switch module described in this thesis. In this experiment, one port of the switch module is connected to a 375ns dual-moded resonant delay line, and the other port is connected to a low power RF pulse input. Two experiments were carried out. In one experiment, the window is switched before the last time bin of the input pulse (375ns before the input pulse ends) and the phase of input flips at the same time. In the other experiment, the phase of the input pulse does not flip and the window is switched at the end of the input pulse.

In the early stages of the tests, we used an old version holder with a 5mm gap designed in 2003. After a newer version holder with the gap reduced to 2mm was completed later, some tests have been repeated with better results. However, we did not have the chance to repeat any active switching or pulse compression tests with the new holder. Instead, a metal spacer was used to reduce the 5mm gap in some of those tests. The silicon window also has experienced several design revisions, and used different materials. The active switching experiments used older version of windows with 5KΩcm resistivity, and we did not have chances to repeat these experiments with the latest 90KΩcm windows. In the following discussion, unless specifically mentioned, the experiments use the latest 90KΩcm windows and the old version of holder. All the measurements are made at 11.424GHz.

6.1 THE ACTIVE WINDOW WITH ONE-PASS TEST SETUP

The one-pass test setup is shown in Figure 34. The silicon window is held in the supporting structure with a 1.299 inch ID, and two wrap-around mode converters are attached, which can convert the TE_{10} mode in a WR90 rectangular waveguide into the TE_{01} mode in a 1.5 inch circular waveguide.

6.1.1 NETWORK ANALYZER MEASUREMENT OF THE ONE-PASS SETUP

The network analyzer measurement will provide the transmission and reflection coefficients, or S-Matrix of the components. By comparing the experimental results with simulation/theoretical calculation results, our design of the structure and the silicon window is examined and improved. Such examination is especially important for some simplified models in the simulation.

Network analyzer HP8510 is used in the experiments. All the measurements are made at 11.424GHz, which is the designed operation frequency of the switch.

In this test, we first measured the empty holder to check the design and fabrication of the window holder, and then the whole switch assembly with a silicon window in the holder was characterized.

The 2003 version of the holder has the reflection coefficient S_{11}=0.267 (-11.47dB) from the frontside and transmission coefficient S_{12}=0.951 (-0.437dB). The backside reflection is S_{22}=0.260, slightly different from the frontside. The insertion loss is approximately 2.4%, including 1.8% from the mode converters. The most part of the reflection comes from the 5mm gap in the holder where the silicon window sits. Before the new holder with smaller gap had been fabricated, we added a metal spacer on the backside of the silicon wafer and reduced the gap to about 3.5mm. With the latest version of the silicon window and a metal spacer in the holder, the S-parameters are measured at S_{11}=0.367 (-8.71dB) and S_{12}=0.901 (-0.906dB). The backside reflection is S_{22}=0.356. The loss is 5.4%, with approximately 3.0% caused by the window.

The 2006 version of the window holder reduces the gap for the window from about 5mm to about 2mm. The 2mm gap, including the thickness of the wafer, is necessary for the insulation between the upper half holder and the negative bias lines on the silicon wafer. Without the silicon window in the holder, the S-parameters are measured at S_{11}=0.105 (-19.58dB) and S_{12}=0.982 (-0.158dB), and the loss is approximately 2.4%. With the silicon window in the holder, the reflection coefficient S_{11}=0.267 (-11.47dB) from the frontside and transmission coefficient S_{12}=0.939 (-0.547dB). The loss is 4.7%, with about 2.3% caused by the window.

For the switches using the latest revision of process and 5000Ωcm wafers, the loss is about 2% higher with comparable reflection, which agrees with the simulation. For switches using the earlier revision of process with higher implantation dose to form the junctions and higher temperature/longer time in the annealing process, the total loss can as high as 10%. As mentioned in the previous chapter, this loss mainly comes from the dopants in the junctions, which can be reduced with lower implantation dose and shorter

anneal time. For the latest test results with the 90KΩcm wafers and new holder, the loss over the window is 2.3%. That loss is still 1.6% higher than the simulation results, mostly due to the dopants.

6.1.2 ACTIVE SWITCHING TEST FOR THE ONE-PASS SETUP

The active switching test will provide the time response and the *on* state properties of the switch. The schematic diagram of the active switching test with one-pass setup is shown in Figure 35.

Peak RF power analyzer was used to measure the input and the transmitted/reflected power through directional couplers. A pulsed current source will drive the switch. The high voltage parts are enclosed in a wood box.

Figure 36 shows the time response of the active window, with the reflection and transmission power normalized to the input. In this experiment, the older version of holder with 5mm gap was used; the tested window is made of the 5000Ωcm wafer. The position of the metal ring in this wafer is slightly different, yielding the larger *off* state reflection. The driver circuit operated at 900V with 4 IGBTs, providing a pulse with about 1000A and 200ns duration. The switching time is 2-300ns. The *on* state losses are measured at about 12%, and the transmission is about 3%. Excluding the losses from the mode converters etc, the loss is about 10%.

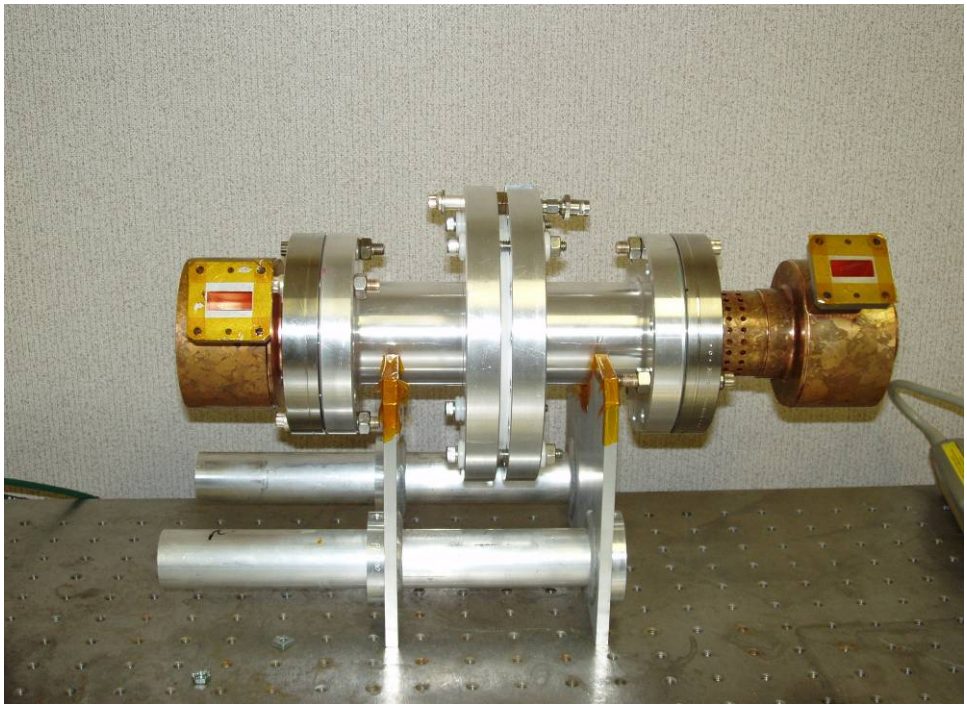


Figure 34. Photo of the one-pass setup

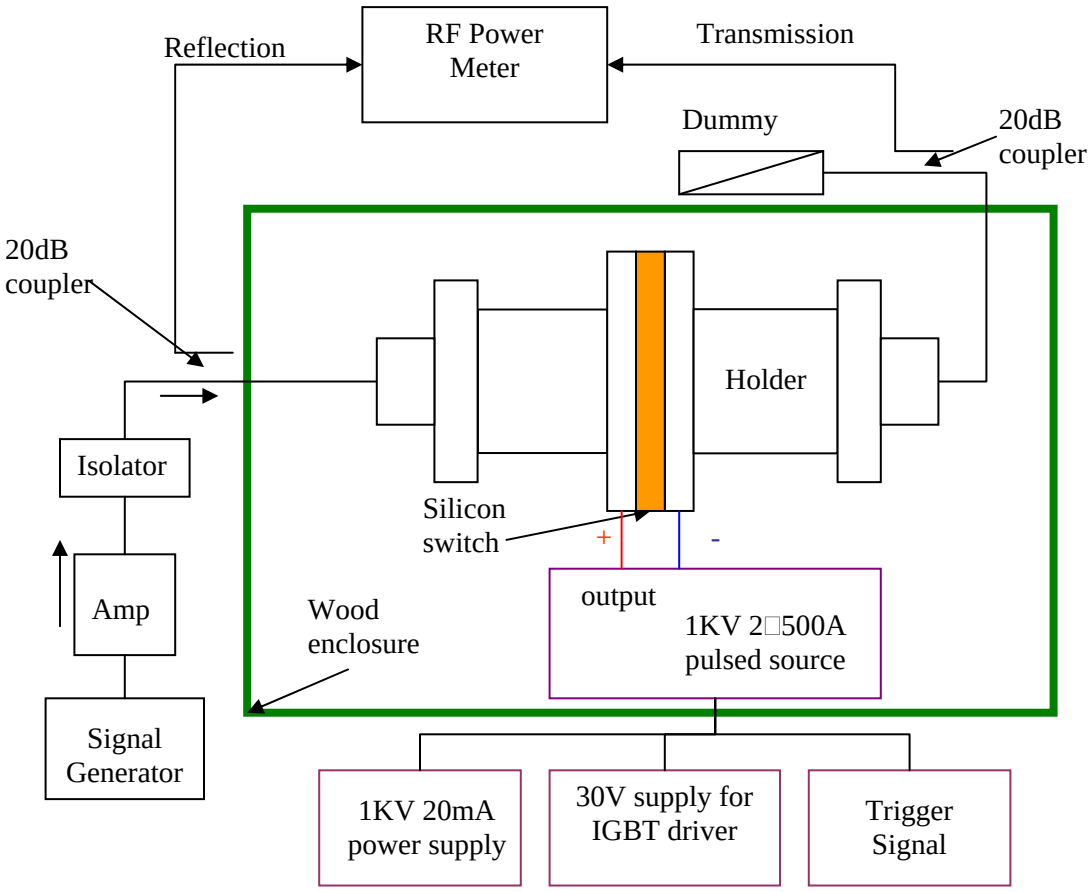


Figure 35. Schematic view of the one-pass active switching test setup

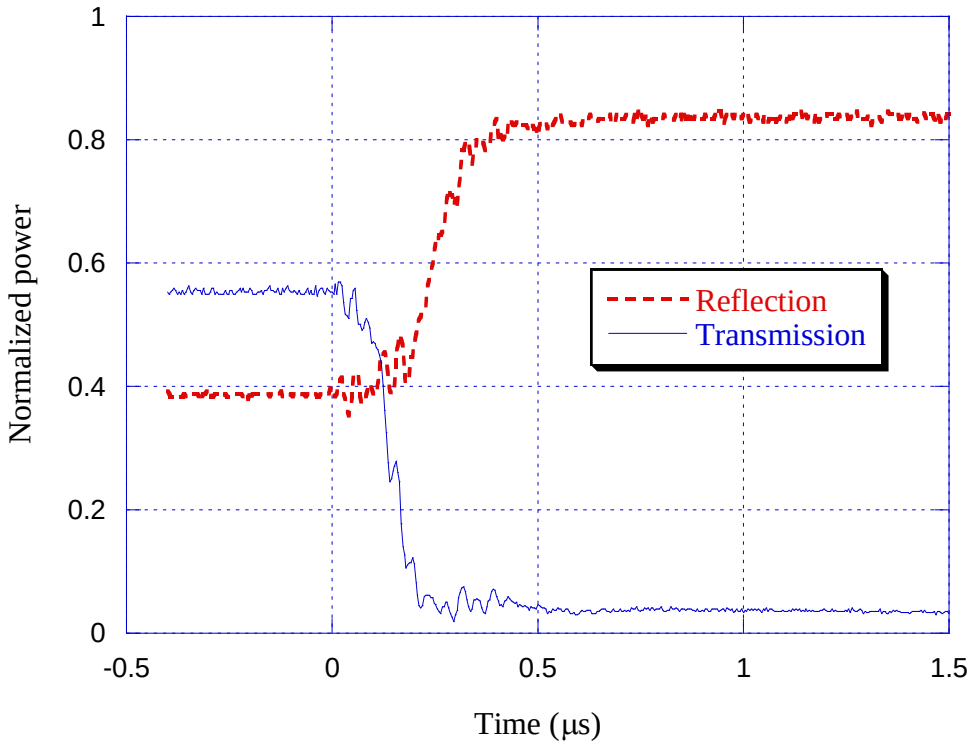


Figure 36. Time response of the active window with one-pass setup

6.2 THE CIRCULAR WAVEGUIDE TEE

The characterization of the circular waveguide Tee includes two parts. First, the Tee is tested as a 3-port device and the S-parameters are measured with the network analyzer. This test will examine the design and machining of the Tee. The S-parameters of the Tee as a 3-port network is shown in Figure 37. At 11.424GHz, the result is quite close to the desired S-matrix shown in (3.51).

In the second test, the symmetric port is terminated with the movable short plane, and then the S-parameters between the other two ports are measured as the short plane moves to different positions. The second test will prove the principal that a two port network

with tunable S-parameters can be constructed with such a setup. The test results are illustrated in Figure 38. The results have shown that the Tee with a short in the symmetric port can provide tunable S-parameters ranging from 0 to 1 with very low losses.

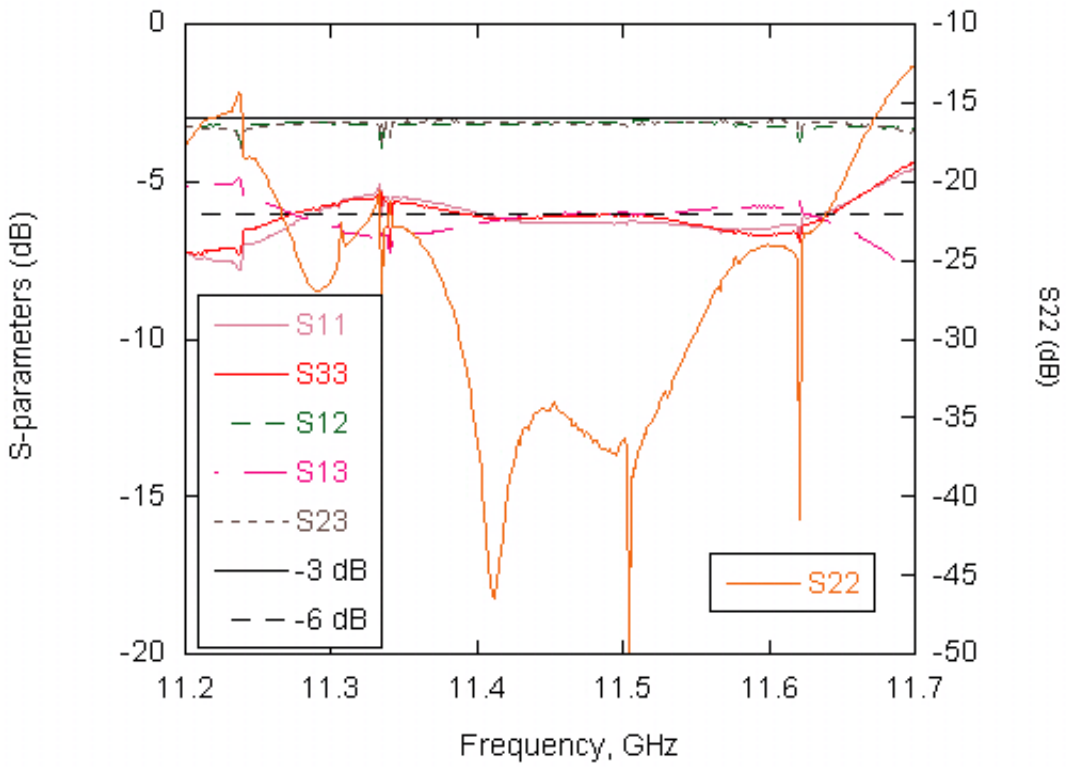


Figure 37. The S-parameters of the circular waveguide Tee

Port 2 is the symmetric port, which is different as noted elsewhere of this dissertation

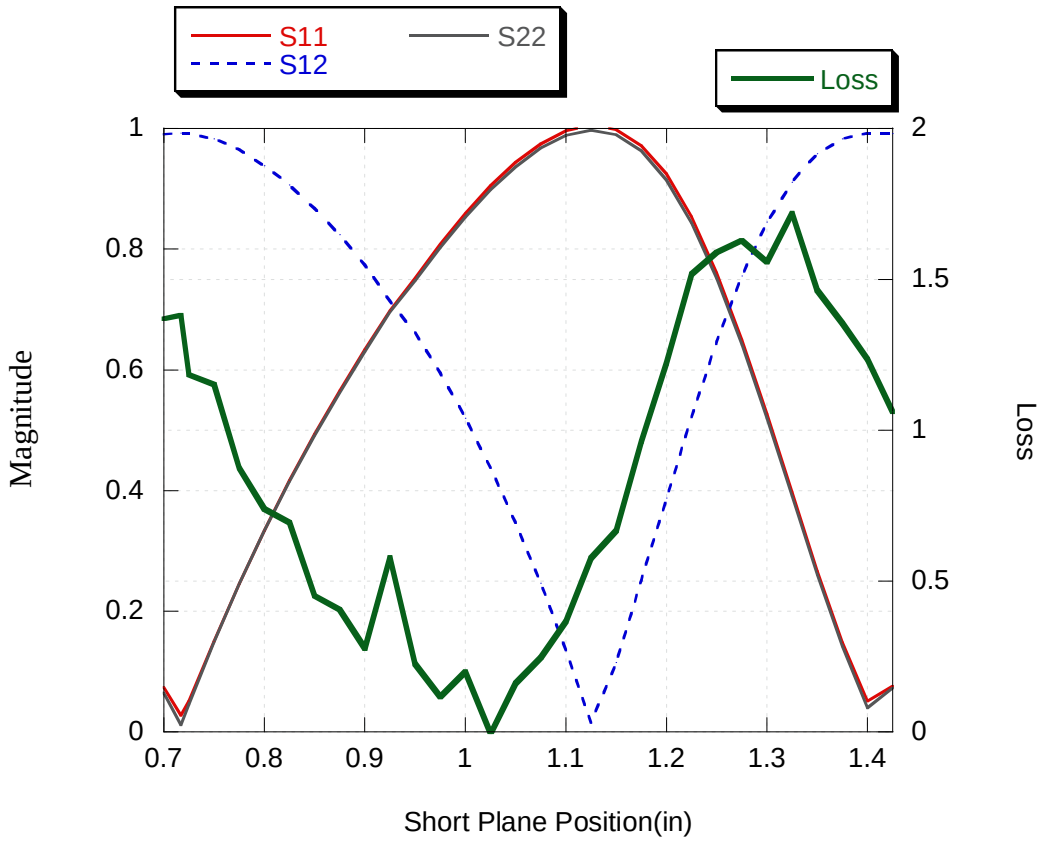


Figure 38. The S-parameters and the losses of the Circular Tee with the symmetric port terminated at different positions, measured at 11.424GHz

6.3 THE ACTIVE WINDOW WITH SWITCH MODULE SETUP

The active switch module consists of a circular waveguide Tee junction with an active window and a movable short plane connected to the 3rd port, as illustrated in Figure 11. Circular to WR90 mode converters are used to connect the ports to the low power RF source and the measurement instruments. The schematic diagram for the active switch experiment is shown in Figure 39, and Figure 40 shows the photo of the actual module.

The active module provides two flexibilities compared to the one-pass setup. It can adjust the S-parameters of the module before and after the switching, according to the requirement of the system. To adjust the reflection coefficient after the switching, the length of the waveguide between the switch and the 3rd port of the Tee needs to be changed, which can be realized by adding spacer waveguides. The reflection coefficient before the switching is adjusted by changing the location of the movable short. The module can also provide a tradeoff between the *on* state loss and the power handling capacity, by adding a variable iris between the Tee and the active window. However, our experiments only utilized the function of adjusting the reflection coefficients.

6.3.1 Network Analyzer Measurement

The NWA measurements are accomplished in groups. In each group of measurement, the movable short will sweep for a round trip phase change of π, and the S-parameters are recorded at different positions.

Figure 41 is the result of the measurement with the 5000Ωcm active window. The old version holder with 5mm gap was used.

Figure 42 is the result of the measurement with the latest batch of active window with 90KΩcm resistivity. The old version holder is used, with a spacer to reduce the gap to 3.5mm. The distance between the window and the Tee is close to the optimized value which was used in the active compression experiment. The loss is significantly improved using lower loss material. The sharp change of S-parameters is also improved with better matching of the window. In the optimized state for active compression, the loss in the module is about 4%, including at least 2% from the mode converters and the Tee.

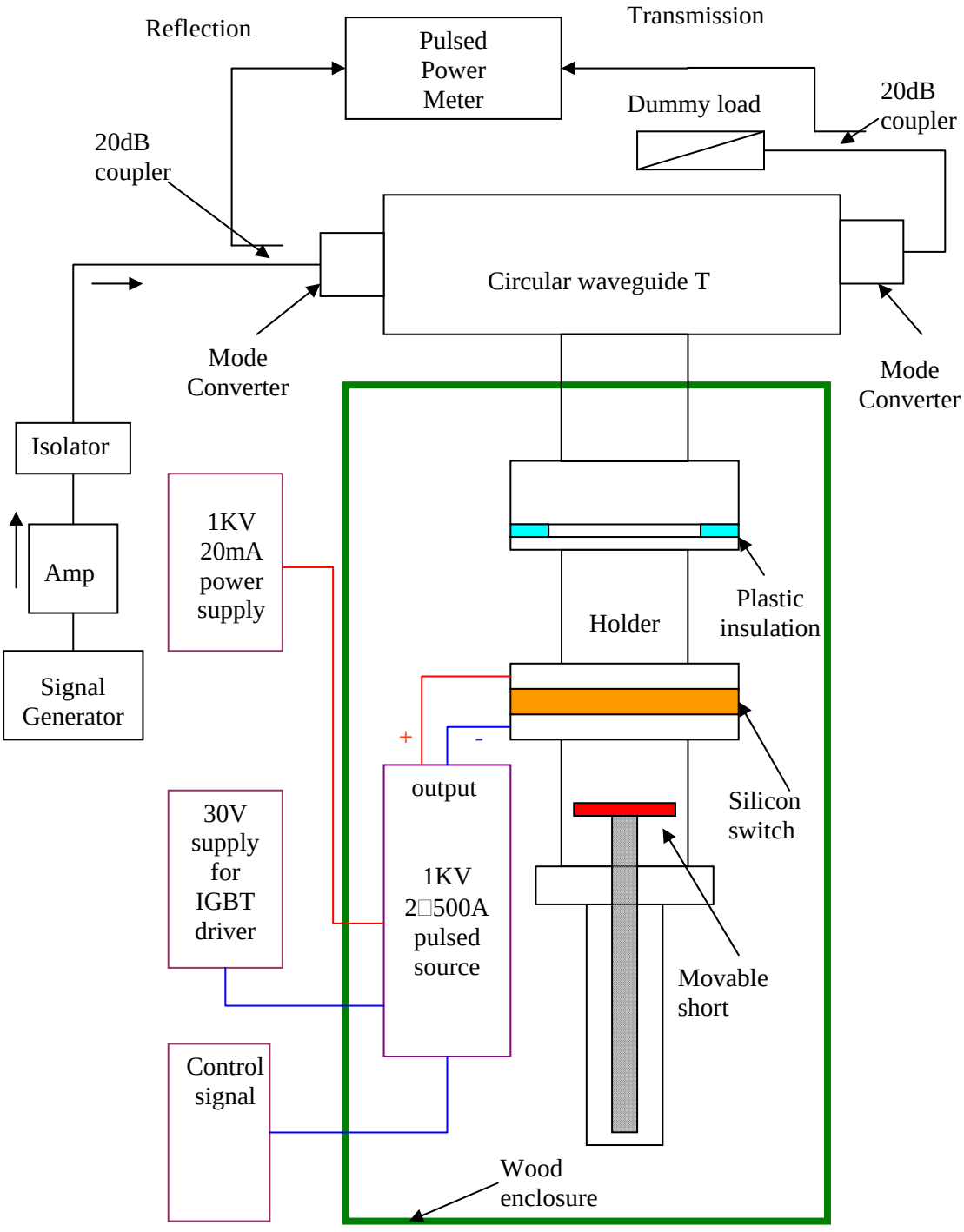


Figure 39. Schematic diagram of the module active switching test setup

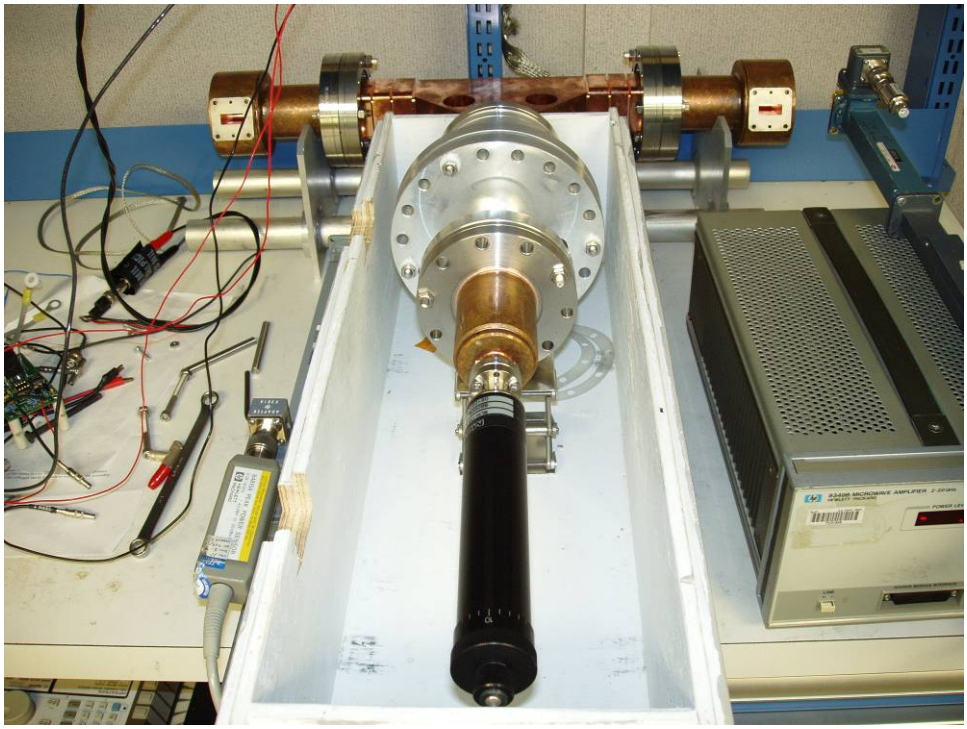


Figure 40. Photo of the switch module

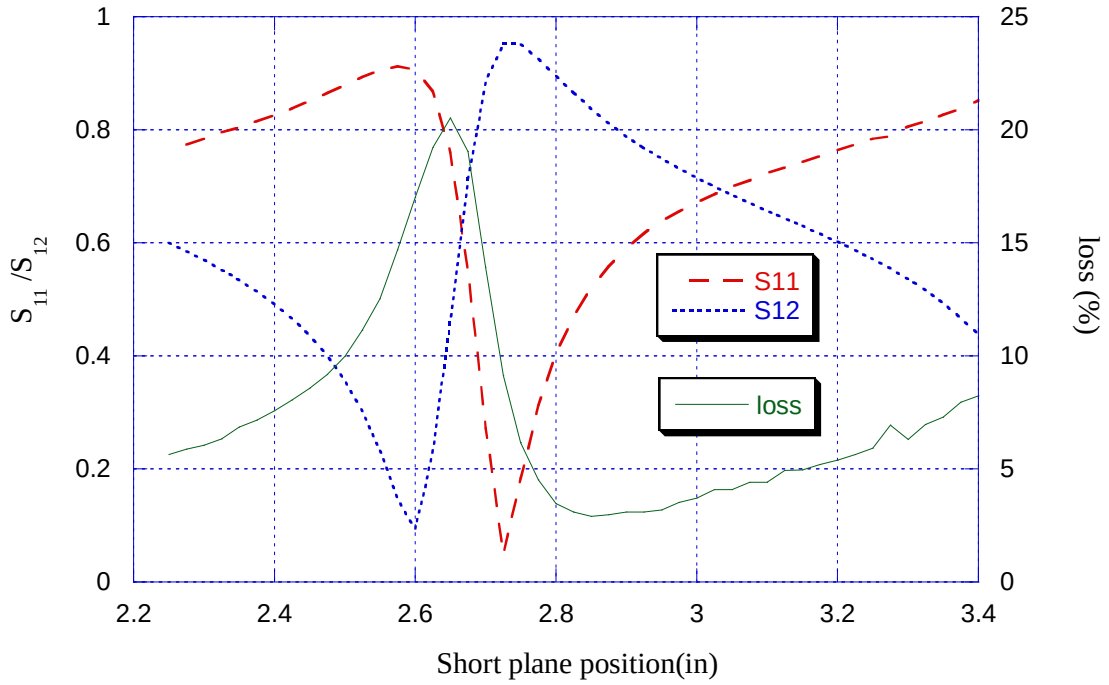


Figure 41. The S-parameters and the losses of the switch module, with the 5000Ωcm window and a 5mm gap in the holder

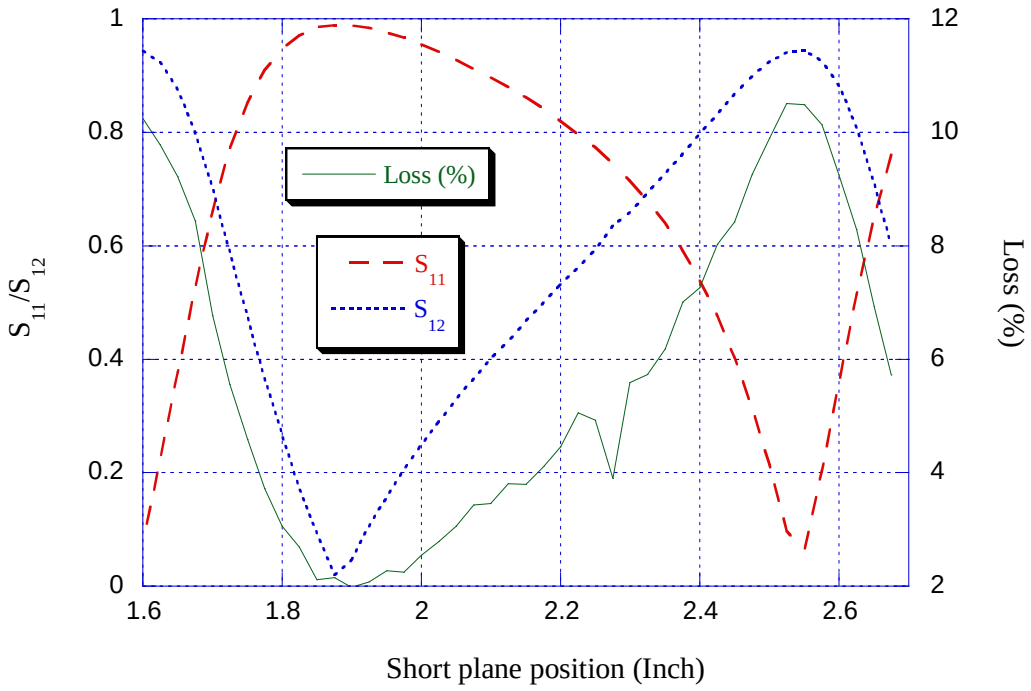


Figure 42. The S-parameters and the losses of the switch module, with the 90KΩcm window and a 3.5mm gap in the holder

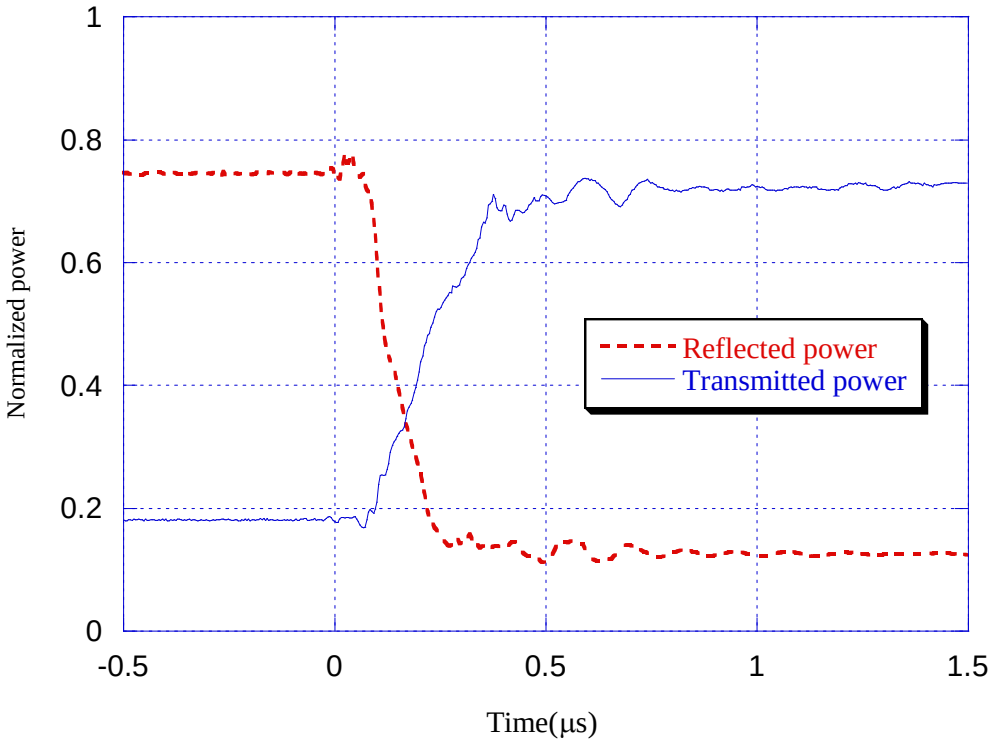


Figure 43. Time response of the active window with the switch module

6.3.2 ACTIVE SWITCHING TEST

The schematic diagram of the active switching test with the switch module setup is shown in Figure 39.

One of the test results is shown in Figure 43. In this test, the older version of holder with 5mm gap was used; the tested window is made of the 5000Ωcm wafer. The result shows that the module successfully tuned the S-parameters for both the off and *on* state. The *on* state loss is approximately 15%.

6.4. LOW POWER ACTIVE PULSE COMPRESSION EXPERIMENTS

6.4.1 EXPERIMENT SETUP

The input and compressed output pulses are monitored by the power meter through directional couplers. The schematic diagram of the setup is illustrated in Figure 44, and Figure 45 shows the photo of the setup.

In the experiments, the older version of window holder was used, with a metal spacer reducing the gap in the holder to 3.5mm. The latest batch of windows was used, with 90KΩcm resistivity.

In each of the experiments, the S-parameters of the switch module before and after switching were tuned carefully to maximize the compression gain. The *on* state S-parameters are tuned by changing the length of waveguide between the holder and the Tee. The *off* state S-parameters are tuned by changing the position of the movable short. The compression ratio is 20, which means the length of the input is 20 times that of the delay time in the resonant delay line.

The driver used in the experiments has a current of about 1400A and duration of 250ns.

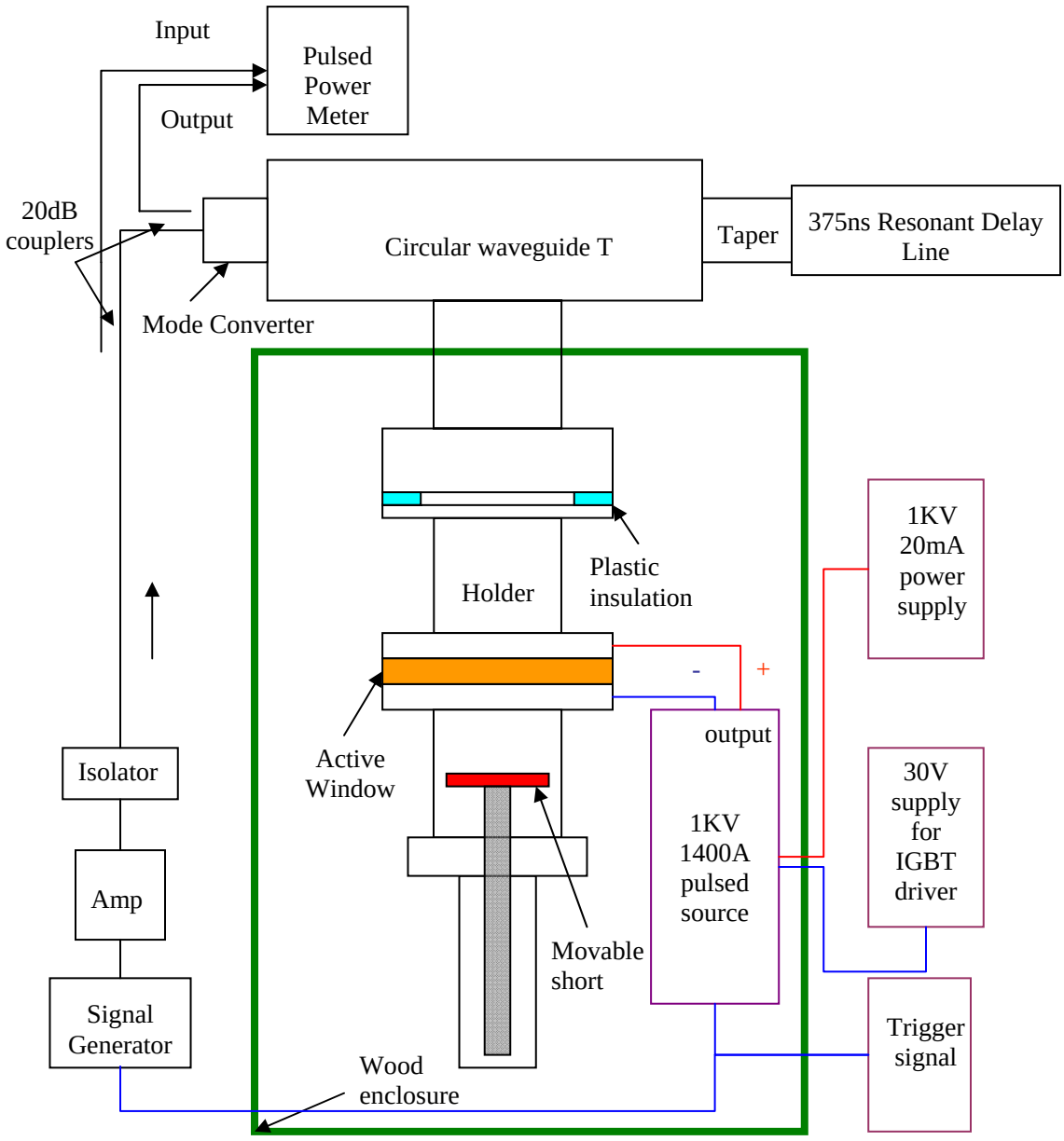


Figure 44. The active pulse compression experiment setup

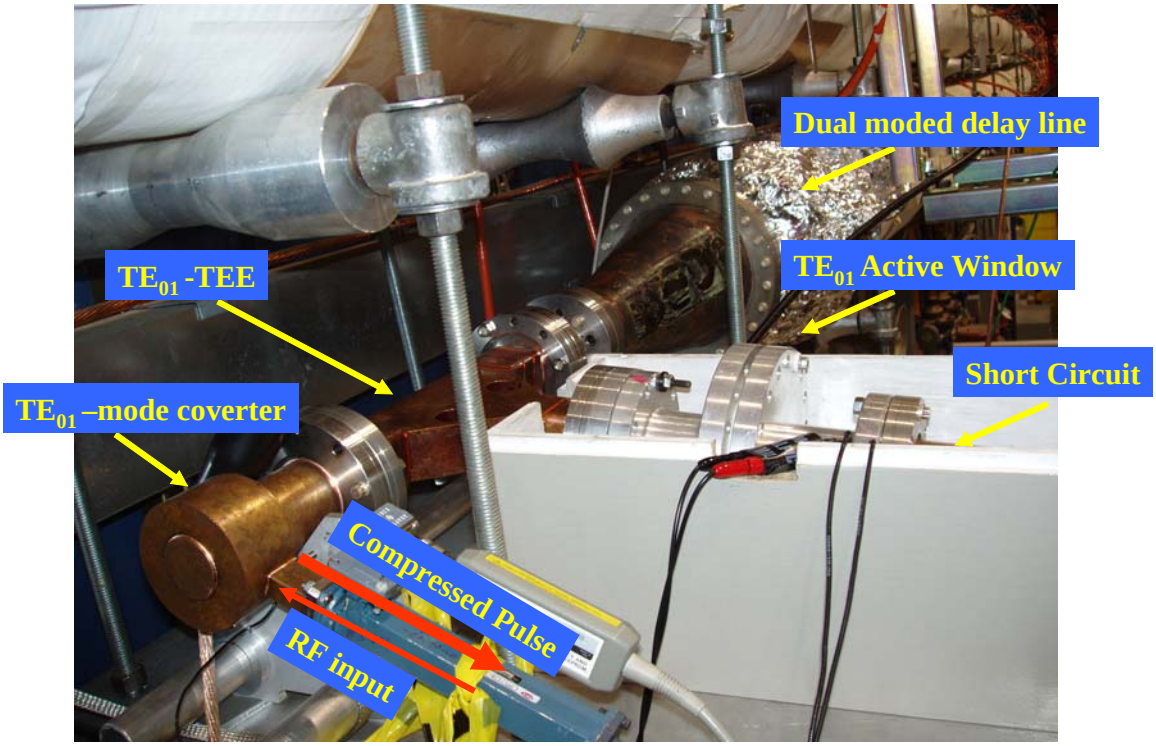


Figure 45. Photo of the active pulse compression experiment setup

6.4.2 Results of the Experiments

The results of the experiments are illustrated in Figure 46 and Figure 47. These results exhibit the advantage over the passive pulse compression system.

In the experiment with input phase flipped before the last time bin, the compression gain of the active compression (with switching) is close to 8, while the passive system (without switching) is only about 5.5 and the theoretical maximum is 9.

In the experiment without input phase flipping, the compression gain of the active compression is about 6, while the theoretical maximum for the passive system is only about 4 (in an actual system with losses, the compression gain is usually 2).

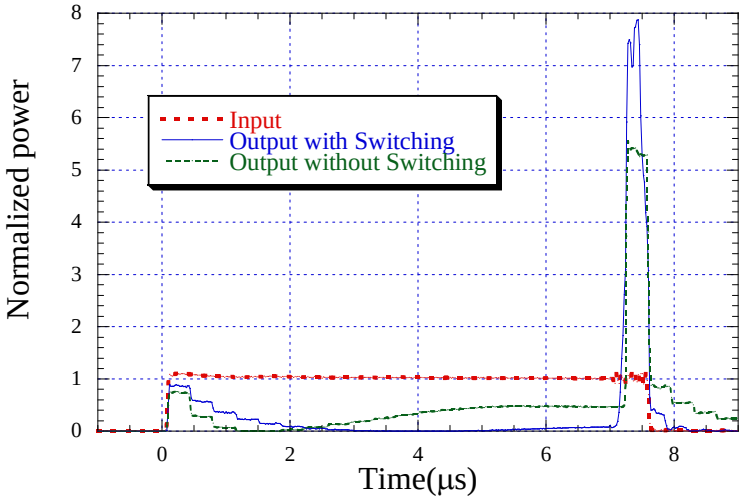


Figure 46. Active pulse compression test with input phase flip

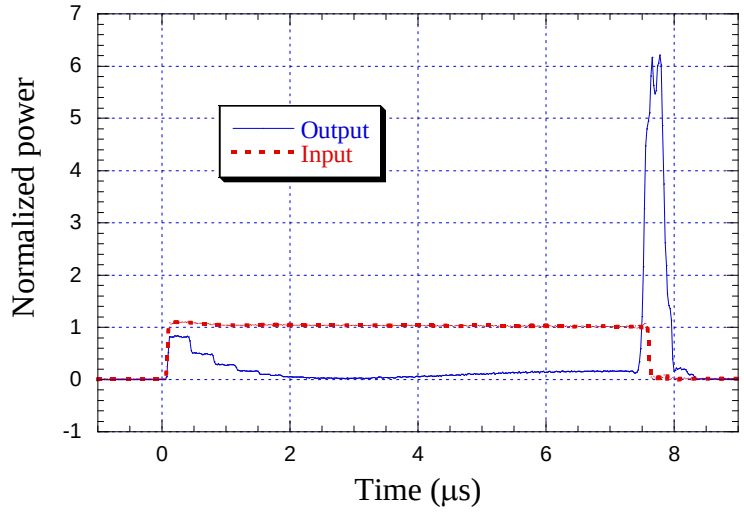


Figure 47. Active pulse compression test without input phase flip

SUMMARY

The results of the low power characterization experiments can be summarized here.

- For the NWA test of the one pass setup, the result shows that the RF structure with 2mm gap was designed correctly. The S-parameters of the window in the structure from the frontside were measured at S_{11}=0.267 (-11.47dB) and S_{12}=0.939 (-0.547dB). The reflection is considerably small. The loss is 4.7%, with about 2.3% from the window, which is still 1.6% higher than the simulation. The additional loss mainly comes from the dopant in the diodes. This loss has already been reduced compared to the earlier version of windows by improvements in the fabrication process.

- The circular waveguide Tee has been characterized with the NWA. The results show that the S-parameters of the Tee satisfy the design requirements. With the symmetric port terminated with a movable short plane, the S-matrix between the other two ports can be tuned with acceptable losses.

- In the active switching test of the one pass setup, 2-300ns switch time was achieved with 12% loss, using the older version of window and the holder with 5mm gap. This result fits the simulation.

- For the tests of the switch module setup, the results showed that the module could successfully match the S-parameters during the on and *off* states, with reasonable losses. The circular waveguide Tee was designed and built correctly.

- The active pulse compression experiments showed improved compression gain over passive systems. The improvement is significant, especially for the case that the input phase cannot be flipped. This demonstrates the possibility of making a pulse compression system with an oscillator like source, which is not possible for any passive systems. Oscillator sources such as the magnetron cannot control the

phase and frequency of the output, but usually they will have lower cost and higher efficiency compared to klystrons.

- The results of optimized compression gain are quite close to the calculated value listed in Table 2, assuming 10% *on* state losses and 4% *off* state losses in the switch module, and 4% losses in the delay line.

CHAPTER 7: CONCLUSION AND FUTURE WORK

7.1 CONCLUSION

In this dissertation, we have reviewed the theory of an active resonant delay line pulse compression system and compared it to other pulse compression systems. We also reviewed the theoretical foundations for the implementation of an ultra-high-power RF switch, the key component for the pulse compression system.

We showed an implementation for such a switch using a novel overmoded circular TE_{01} mode three-port network and an active window based on bulk effects in the semiconductor. The switch module can provide tunable transmission coefficients at both the *on* and *off* states of the switch. The module is also able to match the *on* state loss of the module to the system requirement, while maximizing the power handling capacity. With the given system requirements, the power handling capacity is proportional to the number of carrier pairs in the active window during the *on* state. The key component of the three-port network is a circular waveguide Tee composed of a rectangular waveguide Tee and 3 circular-to-rectangular mode-converters. We exhibited the analytical design of the compact circular-to-rectangular mode-converter. To provide higher power handling capacity, we also presented several schemes of the multi-element switches and the scaling laws of those switches.

We presented the design and implementation of an array of PIN diodes spatially combined into the TE_{01} mode circular waveguide. The active window which comprises the array of PIN diodes has two fundamental novel features that enable it to be fast and reduce its losses. First, the diodes are contained on the surface of the silicon wafers and confined to a small ring-shaped region at the peak of the electric field radius. This reduces the total amount of charge needed to switch the reflectivity of the window, and

makes it possible to reduce the length of the diodes. Second, the matching of the window at the *off* state is done by a metallization ring, which serves also as a parallel feed for the biasing of the diodes. We demonstrated the use of such a device in a pulse compression system with substantially improved gain over the passive system. We showed also for the first time, the possibility of using such a system to compress the output of an oscillator like source. This was not possible before.

The switching time of our active window was measured at 200-300ns, driven by a 1KA current. Although this active window is much faster than its predecessors, it still needs improvement for applications in a real active pulse compression system with a few hundred nanosecond output width. The switching speed is limited by the large number of carriers required for the switch with a satisfying power handling capacity.

7.2 HIGH POWER TEST

A high power experiment needs to be completed in the future, which will determine the power handling capacity of this switch and the time response under a high power RF field. The equivalent power handling capacity is basically determined by the maximum electric field that the active window can sustain.

From the known range of breakdown field for silicon, the capacity in the range of tens of megawatts is expected. With the assistance of a high power RF field, the switching speed is also expected to be faster than the low power test results.

7.3 IMPROVING THE CURRENT SWITCH DESIGN

There are several possibilities to improve the performance of the current window.

The current low loss windows used in the active compression experiments are made of single side polished silicon wafers. The unpolished side of the wafer has a lower

breakdown field, which may reduce the power handling capacity significantly. The backside of the wafer can be polished before the fabrication of the switch.

To enhance the switching speed of the window, higher injection current can be attempted. The maximum current is limited by the maximum current allowed by the diodes, as well as the serial impedance in the circuit. It is possible to achieve a switching time under 100ns, which would make this switch more suitable for a real active RF pulse compression system.

To reduce the loss of the module further, copper can be used to replace the aluminum lines on the window.

7.4 OPTICAL SWITCH

In the design of this forward biased electrical switch with a metal ring, we have found that the required number of carrier pairs is only $3.5\square 10^{14}$. Generating this number of carriers only requires energy of 0.06mJ. Generating this number of carrier pairs through laser is not very hard if the wavelength is properly chosen. It is possible to design such an optical switch. A metal ring can be also used to match the window during the *off* state, and help the reflection of *on* state. The laser can be projected onto a ring shape region. Even if it's not possible to project the laser onto the ring shape region, and the metal ring is not used, the required energy in the laser pulse will still be acceptable, as the cost of high power laser decreasing.

The optical switch can also have lower *off* state losses by removing the dopant and metal in the PIN diodes. It's even possible to use a very thin wafer such as 100μm to reduce the loss further. Of course, the switching speed of the optical switch is very fast, which could be less than 1ns. Such a switch could be ideal for the active RF pulse compression systems.

7.5 REVERSE BIASED SWITCH TRIGGERED BY LASER

To enhance the power handling capacity of the window, the required number of carrier pairs for switching can be much larger than the switch of current design. When the number is large enough, the laser power required by the optical switch might be too high.

A possible alternative is to build an electrically controlled switch using reverse biased PIN diodes. The diodes can be triggered by a low power laser. With the initial carriers generated by the laser, the breakdown of the PIN diodes is more controllable and requires much lower voltage. The impact ionization can generate carriers more efficiently than the forward biased diode. It is possible to use a low power laser and a 1-2KV driver circuit to achieve a switching time under 100ns and a higher power handling capacity. It is possible to use such a switch for a pulse compression system with the output of hundreds megawatt in power and several hundred nanosecond in pulse width.

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