

**High-Speed, High-Resolution Analog Waveform Sampling
in VLSI Technology**

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**HIGH-SPEED, HIGH-RESOLUTION
ANALOG WAVEFORM SAMPLING
IN VLSI TECHNOLOGY**

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL
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IN PARTIAL FULFILLMENT OF THE REQUIREMENT
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DOCTOR OF PHILOSOPHY

Gunther Martin Haller

March 1994

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I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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Abstract

Switched-capacitor analog memories are well-suited to a number of applications where a continuous digitization of analog signals is not needed. In data acquisition systems based on the use of an analog memory, the input waveforms are sampled and stored at a high rate for a limited period of time, and the analog samples are then retrieved at a lower rate and digitized with a slow ADC before new waveforms are acquired. The advantages of using an analog memory are lower overall power dissipation and cost, higher density and reliability, and potentially superior performance. The analog memory essentially exploits the fact that the sampling and storage of samples in a bank of analog memory cells can be accomplished at a higher rate and with a greater precision than direct digital conversion.

This dissertation examines the important components of an analog memory in detail and investigates their use in a number of architectures. The research has led to the design of an analog memory that can acquire analog waveforms at sampling rates of several hundred MHz with a dynamic range and linearity of more than 12 bits, without the need for elaborate calibration and correction procedures. This is accomplished by means of a new memory architecture that results in memory cell pedestals and sampling times that are independent of the signal level, as well as cell gains that are insensitive to component sizes. The write address control for this memory has been realized with an inverter delay chain that provides substantially higher performance with respect to sampling rate and timing accuracy than other published approaches.

Based upon the concepts developed in this work, an experimental analog memory was designed and integrated in a 2- μm CMOS process. Extensive measurements of this prototype at sampling rates up to 700 MHz are presented and demonstrate a dynamic range, linearity, offset, and gain accuracy corresponding to a precision of more than 12 bits after a

simple dc baseline subtraction. One 32-cell channel in the experimental circuit dissipates only 2 mW from a single 5-V supply.

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Chapter 1

Introduction

1.1 Motivation

Many modern data acquisition systems require the recording of analog signals as a function of time over a wide dynamic range. Most commonly, the analog information is digitized at the required acquisition rate using an analog-to-digital converter (ADC). However, in a number of applications analog waveforms need only be captured as snapshots; continuous digitization is not necessary. Examples of such applications include pulse echo phenomena (RADAR, LIDAR, ultrasonics, non-destructive material or medical testing), pulse shape recording (high energy physics experiments, accelerator diagnostics), and laboratory instrumentation (oscilloscopes, transient digitizers). In such cases an input waveform can be sampled at a high rate for a limited period of time, and the samples stored in an analog memory. The analog samples are then retrieved at a lower rate and digitized with a slow ADC before a new waveform is acquired. Advantages of using an analog memory include low overall power dissipation and cost, high density, and potentially superior dynamic range at high sampling rates.

Two main technologies are available for realization of an integrated analog memory: charge-coupled devices (CCD's) and switched-capacitor circuits. Integrated circuits based on switched capacitor techniques are inherently capable of higher accuracy and sampling

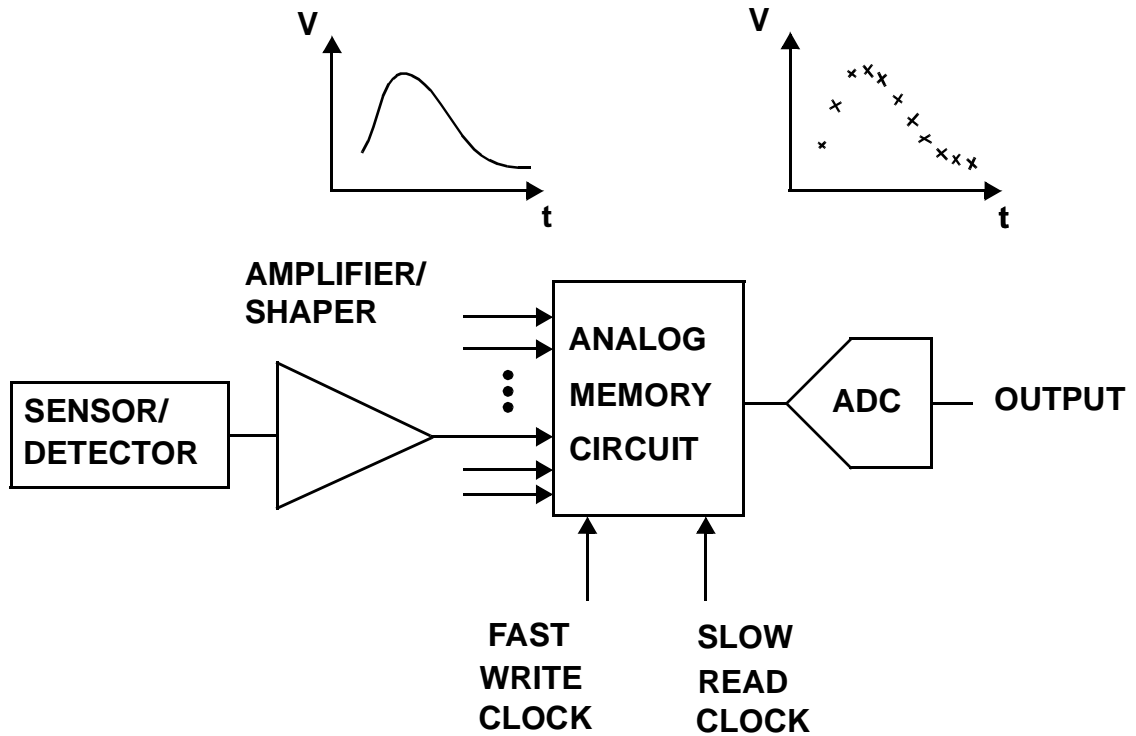


Figure 1.1: Signal acquisition with an analog memory circuit.

rates than CCD devices. Furthermore, CCD's require elaborate clocking circuitry that generally dissipates considerable power.

The objective of this research is an in-depth investigation of using switched-capacitor analog memories for analog waveform sampling at rates exceeding 100 MHz. Strong cost and performance incentives especially encourage the use of analog memories in high energy physics experiments. Fast analog waveform capture for tens of thousands of channels must be provided at low cost and with a minimum of power dissipation, prohibiting the use of high performance real-time digitizers. Low power dissipation is a particularly important prerequisite for collider detectors [1, 2], where the electronics is integrated in a confined area and heat extraction is extremely difficult.

A block diagram of a typical waveform acquisition system is shown in Figure 1.1. The electrical signal generated in the detector or sensor is amplified and shaped, and the conditioned waveform is then sampled and stored at a high rate in the analog memory. The

stored information is subsequently retrieved at a relatively low rate for conversion into digital form. The use of an analog memory eases the speed required of the ADC considerably and therefore significantly reduces cost and power dissipation. In addition, many signal channels can be multiplexed onto one A/D converter when readout speed and latency are not crucial. As an additional benefit, large dynamic range signals can be recorded at higher rates with an analog memory than can be achieved with monolithic real-time converters.

Specific applications for the memory proposed in this work appear in high energy physics accelerators and colliders, where bunches of particles are transported at close to the speed of light inside structures several kilometers long. For example, in the Stanford Linear Collider (SLC) bunches of electrons and positrons are accelerated in a three-kilometer long disk-loaded waveguide [3, 4]. In the proposed Next Linear Collider (NLC) particles will be accelerated in two linear ten-kilometer long machines for head-on collisions [5]. In order to control the operation of a particle beam with sufficient accuracy, its transverse position must be measured at as many as a thousand locations with a precision of better than $1\ \mu\text{m}$ across a range of 5 mm. The complexity and cost of such a measurement system can be significantly reduced through use of high-speed, high-dynamic range analog memories, while also improving performance.

In this thesis the basic characteristics of integrated transistor switches and capacitors are reviewed and an architecture for waveform sampling at rates as high as several hundred MHz is introduced. A circuit implementation of this architecture is investigated in detail in respect to its theoretical dc and ac performance. In order to confirm the results of this study, an experimental version of the circuit has been fabricated in a 2- μm CMOS technology and tested. Sampling rates up to 700 MHz have been achieved while sustaining a dynamic range of more than 12 bits. The proposed analog memory is a viable alternative to real-time analog-to-digital converters in applications where continuous acquisition is not required. The power dissipation of the device is orders of magnitude below that typical of commercial monolithic converters, which are presently limited to a dynamic range of 8 bits for rates exceeding 100 MHz.

1.2 Organization

The implementation of analog sampling and storage functions using switched capacitor circuits is described in Chapter 2. Several analog memory architectures that have already been implemented are examined and their operation is explained. The performance limitations of these circuits are studied with particular attention given to the impact of variations in component sizes on the memory cell transfer function. Calibration and correction procedures that can be used for high-precision data acquisition are reviewed. The chapter then describes circuits employed for the write control in analog memories and closes with a definition of terms commonly used to describe sampling systems.

In Chapter 3 the MOS transistor is explored with respect to its use as a voltage switch. Impedance levels and error voltages are evaluated for several memory cell configurations wherein the switch is inserted in the signal or signal-return paths. The limiting factors governing the matching of the signal responses among individual memory cells are identified.

Chapter 4 introduces a new analog memory architecture. The operation of this memory and its expected performance are discussed. The memory circuit's transfer function is derived, illustrating the effect of component mismatch within a memory channel on the memory response. The memory is addressed by means of shift registers for sampling speeds below 100 MHz. For higher speeds, a write control circuit comprising starved inverters with feedback control is proposed.

The folded-cascode operational amplifier is the subject of Chapter 5. Performance parameters such as gain, bandwidth, and noise are investigated, and simulation results are compared to experimental data that was obtained from integrated prototypes.

The design of a two-channel analog memory with 32 cells in each channel is described in Chapter 6. This circuit was integrated in a 2- μm CMOS technology with poly-to-poly capacitors. The test setup used for the characterization of the memory is explained and experimental results are presented. A dynamic range of more than 12 bits has been achieved at sampling rates up to 700 MHz while dissipating only 2 mW of power in each channel.

Chapter 7 summarizes the contributions of this research and identifies areas of future study.

Chapter 2

Analog Memory Concepts

2.1 Overview

The design of analog memory circuits is influenced not only by the issues involved in their realization in a given technology, but also by the intended application. The choice of an architecture depends strongly on whether the circuit serves as an analog storage and multiplexing device, as an analog waveform recorder, or as an analog delay line.

In this chapter the basic concepts underlying analog memory design are explained, and architectures that have been realized in switched-capacitor technologies are reviewed. The study focuses on waveform sampling architectures wherein one of the important performance criteria is the matching of transfer characteristics of the individual memory cells. The degree of matching needed and the desired overall performance determine the complexity of the required calibration and correction procedures for such circuits. These procedures are formulated, and the requisite cell-to-cell matching is studied. The advantages and limitations of existing memory structures are also addressed.

The individual cells in a bank of analog memory cells are addressed on-chip by dedicated write and read control circuits. Implementations of such addressing circuits are reviewed and their operation described. The chapter closes with a definition of terms used throughout the thesis.

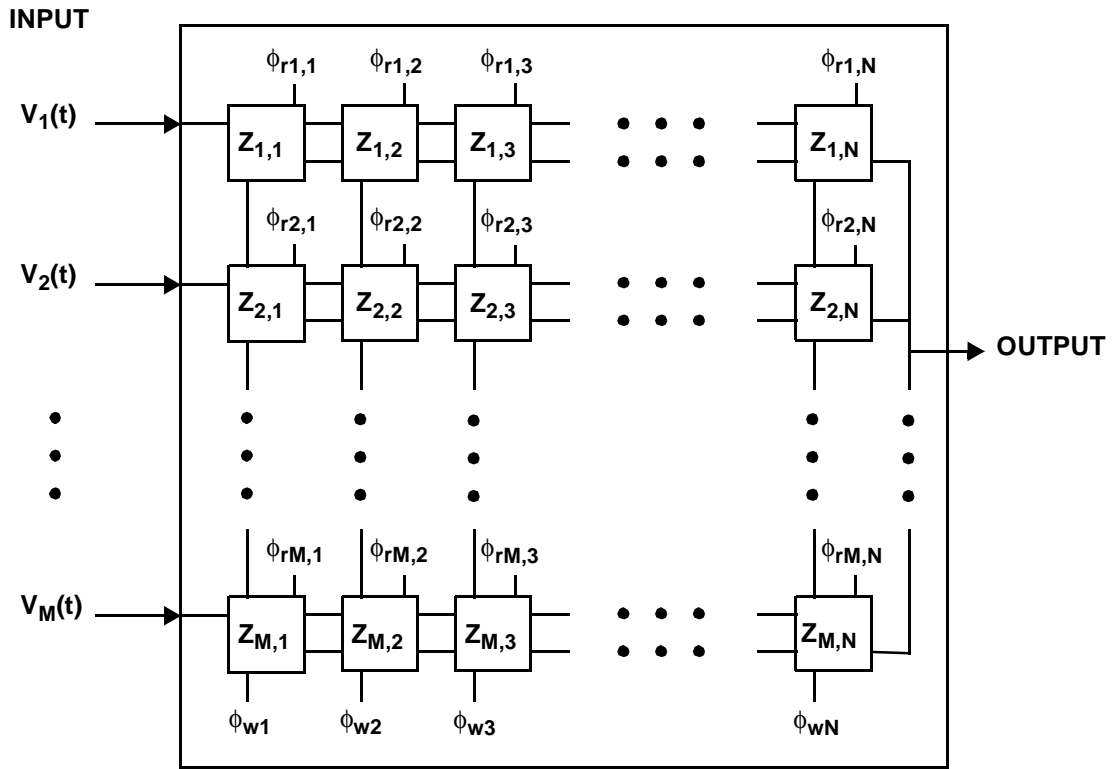


Figure 2.1: Generalized representation of an analog sampling and multiplexing memory.

2.2 Analog Storage

Figure 2.1 illustrates the concept of an analog memory circuit comprising M signal channels with N generic storage cells in each channel. The location of a cell in a channel is indicated by the column address i ($1 \leq i \leq N$), and the channel number by the row address j ($1 \leq j \leq M$). An analog input signal $V_j(t)$ is connected to all N memory cells in channel j . Control signals ϕ_{w1} through ϕ_{wN} and $\phi_{r1,1}$ through $\phi_{rM,N}$ are the memory write and read address signals, respectively. Waveforms can be stored in the analog memory at N timing instances by sequentially addressing the memory cells within a channel via write control signals ϕ_{w1} through ϕ_{wN} . The input voltages at time t_1 are stored in memory cells $Z_{j,1}$, at time t_2 in cells $Z_{j,2}$, and so forth until the input levels at time t_N are recorded in cells $Z_{j,N}$. After the write phase is finished, the readout commences by applying read address

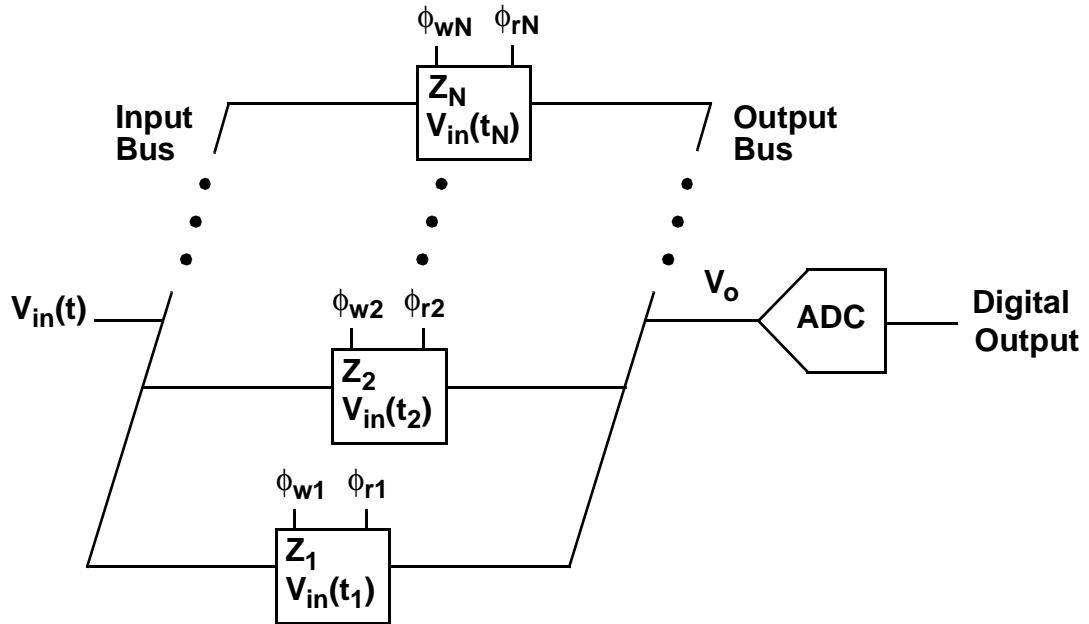


Figure 2.2: Block diagram of one signal channel of an analog waveform memory.

$\phi_{r,1}$ which connects the first memory cell of the first row to the output bus. After the output has settled it can be digitized by an on or off-chip converter. Likewise the remaining memory cells are serially read out and digitized.

The maximum number of analog values that can be stored in an array such as that depicted in Figure 2.1 is the number of rows, M , times the number of columns, N , and is generally bounded by the physical chip size. The intended application dictates the relationship between M and N . In circuits dedicated for analog storage and multiplexing, for instance, the number of channels is large compared with the number of cells in one channel ($M \gg N$). The primary purpose of such an architecture is the optimization of required space, power dissipation, and cost for large data acquisition systems by reducing the number of interconnections and analog-to-digital converters [6, 7, 8]. In such applications, the minimum time between the acquisition of two consecutive input waveforms must be long enough so as to permit a sequential read out of the data.

The focus of this thesis is on analog waveform sampling applications, where the number of cells in a channel is large compared to the number of channels on one chip

($N \gg M$). Figure 2.2 shows a single channel version ($M = 1$) of an analog memory with the input connected to all N memory cells. During the write phase, the analog input waveform is sequentially stored in the N memory cells Z_1 through Z_N . After the entire waveform is acquired, the signals stored in the memory cells are sequentially read out and digitized during the read phase.

The voltage read out from a given memory cell i during the read phase, V_{oi} , corresponds to the input voltage $V_{in}(t_i)$ sampled and stored at time t_i . Generally, the time between readout of two adjacent memory cells can be much larger than the time between the acquisition of consecutive input samples during the write phase, $t_i - t_{i-1}$. This relaxes the speed requirement on the following high-resolution ADC considerably. A single low-cost, low-power converter is generally sufficient for digitization of the analog information read out from many memory cells.

2.3 Memory Calibration and Correction Procedures

The challenge in analog memory design is to produce a uniform and linear response in a large number of memory cells at a level of performance comparable to the inherent accuracy of the technology. Principal performance issues are cell-to-cell offset and gain variations within a memory channel, which are governed by the circuit architecture and its sensitivity to the matching properties of its constituent components. The voltage V_{oi} read out from a given memory cell i can be expressed as a function of the input voltage V_{in} ,

$$V_{oi} = H_i(V_{in}), \quad (2.1)$$

where H_i is referred to as the transfer function of memory cell i . Ideally, the transfer functions of all cells are identical and equal to one. In reality this will not be the case because of gain, nonlinearity, and offset variations among cells. The origin of these variations can be inaccuracies in the fabrication process or control signal feed-through while the circuit is being operated.

In high-precision applications, the lowest achievable cell nonuniformities may not be adequate and must therefore be cancelled by correcting the data. In large systems, it is essential that the computational effort and the number of components required to store the

Non-Ideal Parameter	Correction Procedure	Number of Calibration Voltage Levels	Number of Constants per Memory Cell
Offset	Subtraction	1	1
Gain and Offset	Multiplication and Addition	2	2
Linearity	Piece-Wise Linear Approximation	Number of Segments + 1	2 x Number of Segments

Table 2.1: Calibration and Correction Parameters.

correction constants be minimized. Calibration is commonly performed by applying known sets of signals at the analog input and storing the resulting output values. The transfer function H_i is then calculated, and the inverse function of H_i is used to correct the acquired data. Cell-specific correction values are commonly expressed in the form of calibration constants. The time needed to determine these constants during the calibration procedure is generally not crucial, whereas a premium is placed on the minimization of processing effort needed for the real-time, on-line correction of the signal data. The goal, therefore, is to minimize the number of calibration constants and the time required to correct the signal data.

The performance of an analog memory and the desired overall accuracy determine the complexity of the inverse function of H_i , and therefore the number of calibration voltage levels to be applied during calibration. Table 2.1 lists the operations that must be performed to correct for offset, gain, and linearity errors, along with the number of reference voltage levels and constants needed for these operations. The cancellation of memory cell offset voltages, for instance, requires a subtraction procedure with one calibration constant for each cell. These constants are obtained by applying a single reference voltage, V_{cal} , to the circuit during calibration. The corresponding output voltage of cell i , V_{oci} , is

$$V_{oci} = V_{cal} + V_{offi} = K_i, \quad (2.2)$$

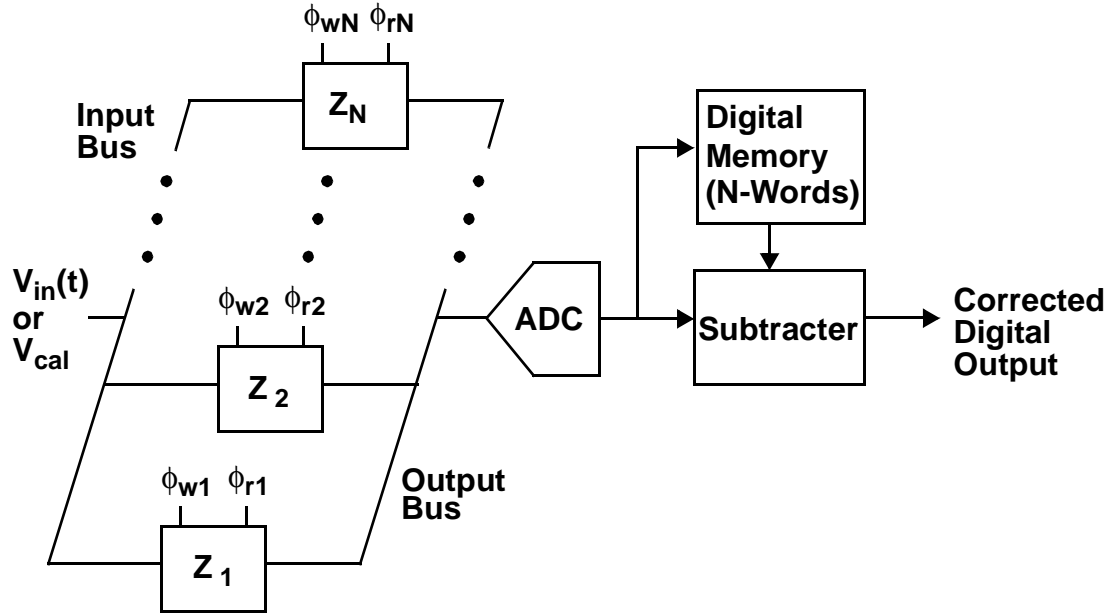


Figure 2.3: On-chip digital correction.

where V_{offi} is the memory cell offset voltage and K_i is the calibration constant to be stored for cell i . During data acquisition, the difference between the input signal voltage V_{sig} and the reference calibration voltage V_{cal} can then be calculated by subtracting K_i from the output response V_{oi} ,

$$V_{sig} - V_{cal} = V_{oi} - K_i. \quad (2.3)$$

The cell dependency is thus removed because the known reference voltage V_{cal} is identical for the entire acquisition system.

The subtraction procedure can be implemented with a digital circuit as illustrated in Figure 2.3. During calibration the voltage V_{cal} is applied at the input, and the digitized output voltage levels are transferred directly into the static digital memory. These stored calibration constants are then subtracted from the data output during signal acquisition time, thereby cancelling all cell specific, as well as common, offset voltages. Note that the cancellation of offset voltages does not require any circuitry to calculate calibration constants since the constants are identical to the output levels digitized during calibration.

Correction of both cell-to-cell gain and offset voltage errors requires the recording of the circuit response to at least two separate reference voltages

$$V_{oci1} = A_i V_{cal1} + V_{offi} \quad (2.4)$$

and

$$V_{oci2} = A_i V_{cal2} + V_{offi} , \quad (2.5)$$

where A_i is the voltage gain of cell i . V_{oci1} and V_{oci2} are the responses of the circuit to reference voltages V_{cal1} and V_{cal2} , respectively. The two calibration constants, K_{1i} and K_{2i} , for each cell are then computed as

$$K_{1i} = \frac{1}{A_i} = \frac{V_{cal2} - V_{cal1}}{V_{oci2} - V_{oci1}} \quad (2.6)$$

$$K_{2i} = -\frac{V_{offi}}{A_i} = V_{cal1} - K_{1i} V_{oci1} . \quad (2.7)$$

During signal acquisition, the voltage level V_{oi} read out from cell i is corrected by means of a multiplication and an addition,

$$V_{sig} = K_{1i} V_{oi} + K_{2i} . \quad (2.8)$$

An analog memory channel with N cells therefore requires $2 \times N$ constants, as indicated in Table 2.1. The number of constants required can be reduced when the responses of the individual memory cells within a channel are uniform enough to satisfy the accuracy specifications after a common correction. For example, when the gain matching among cells is satisfactory, (2.8) reduces to

$$V_{sig} = K_1 V_{oi} + K_{2i} , \quad (2.9)$$

and only $(N + 1)$ constants need to be stored.

As indicated in Table 2.1, nonlinearities in the circuit response can be corrected using a piece-wise linear approximation to the memory cell transfer curve. The number of cali-

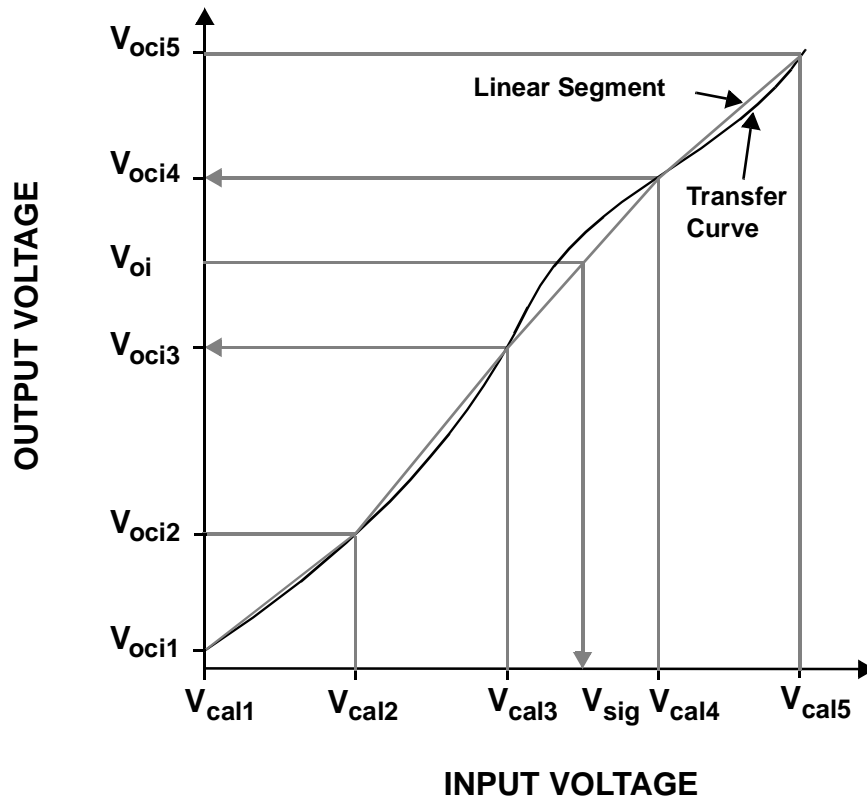


Figure 2.4: Calibration with linear approximation method.

Calibration voltage levels is determined by the number of linear segments needed to obtain the desired accuracy, as illustrated in Figure 2.4. In this figure a nonlinear transfer curve is approximated by four linear segments. The five calibration voltages are V_{cal1} through V_{cal5} , and the corresponding memory responses are V_{oci1} through V_{oci5} . During data acquisition, the input signal voltage, V_{sig} , can be approximated from the measured output voltage V_{oi} by a linear interpolation between the nearest calibration output values.

The procedures listed in Table 2.1 are sufficient to cancel cell offset, gain, and nonlinearity errors for dc input signals. The analog memory must be carefully designed and evaluated to maintain the needed performance across the desired input signal frequency range. A variation in the sampling time interval from cell to cell manifests itself as an amplitude error, as is illustrated in Figure 2.5. In this example, a ramp input signal is sampled at four distinct times, t_1 through t_4 , on the trailing edges of clocks ϕ_{w1} through ϕ_{w4} and stored in

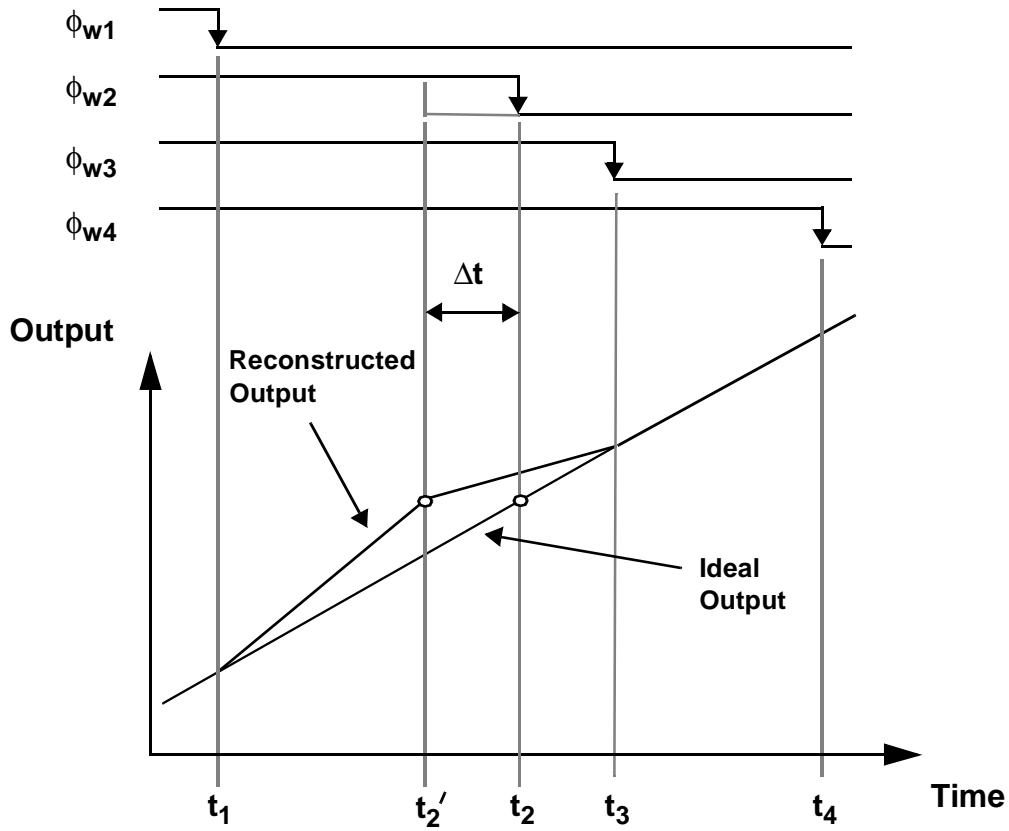


Figure 2.5: Effect of sample time error on the reconstructed waveform.

four consecutive analog memory cells. The time t_2' is the nominal sample time, and t_2 is the actual time when the second sample is stored. A deviation $\Delta t = t_2 - t_2'$ results in an amplitude error

$$\Delta V_o = \frac{dV_{in}}{dt} \Delta t, \quad (2.10)$$

where dV_{in}/dt is the slope of the input voltage signal.

The correction of errors due to sampling interval variations is straight-forward, provided that the time deviations are stable and independent of the input signal level. The sample time t_i associated with a given memory cell location i is simply adjusted by a correction factor Δt_i that is obtained from a single ac input waveform during calibration.

These correction factors can be determined from a ramp or sine wave input signal and are applicable to all input signal shapes and frequencies.

Input voltage level dependent sampling times, however, entail substantial measurement errors for high frequency input signals, as is investigated in Chapter 3. Complex ac calibration and data correction procedures may be required if the memory does not satisfy the performance objectives.

2.4 Analog Memory Circuit Architectures

Details of the structure and operation of several analog waveform memory circuit architectures are reviewed in this section. The memory cells in these architectures are composed of transistor voltage switches and capacitors for charge storage. The circuits can, in principle, be classified into two categories: those with an amplifier or buffer dedicated to each storage cell [9, 10] and those with a single amplifier common to an entire memory channel [11]-[19].

Shown in Figure 2.6 is the architecture of an analog waveform storage circuit utilizing a traditional sample-and-hold structure. Each sampling cell consists of a write (sampling) switch, S_w , a memory cell capacitor, C , a readout buffer, B , and a read switch, S_r . Acquisition of a signal typically proceeds as follows. While switches S_{w1} through S_{wN} are conducting, the voltages on the capacitors C_1 to C_N track the signal applied to the input bus. As the switches S_{w1} through S_{wN} are turned off sequentially, the input waveform is sampled and held at N discrete times on the cell capacitors. The stored analog information can then be read out onto the output bus by consecutively closing and opening switches S_{r1} through S_{rN} . The uniformity of the memory cell responses in this architecture is governed by the matching of the write switches, the storage capacitors, and the gains, nonlinearities, and offset voltages of the cell buffer amplifiers. The power dissipation scales with the number of memory cells.

The architecture depicted in Figure 2.6 has been implemented as a circuit called the AMU [9, 20]. The AMU chip contains 256 memory cells and has a maximum sampling frequency of 150 MHz with a power dissipation of 200 mW. A simple MOS source follower was used as a buffer in order to meet power and size requirements. The

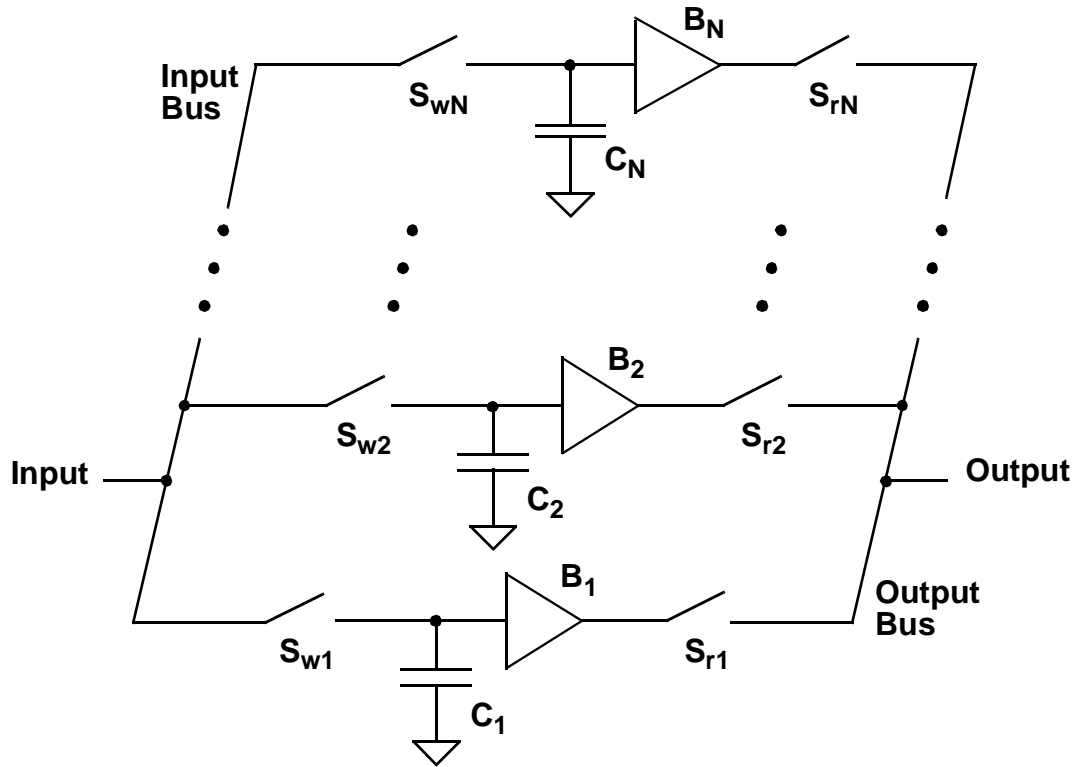


Figure 2.6: Analog memory architecture with an amplifier in each memory cell.

drawbacks of using such a simple buffer circuit are large cell-to-cell gain variations and a nonlinear cell response. One of the applications for the AMU is a 10,000 channel high energy physics detector system with 512 sampling cells (two chips) for each channel [1, 21, 22]. The calibration and correction procedure needed to eliminate variations of the cell offsets, gains, and nonlinearities employed a piece-wise linear approximation with eight segments for each memory cell.

A bus-oriented architecture with considerably less power dissipation than the architecture of Figure 2.6, as well as improved memory cell response matching, is shown in Figure 2.7. In this approach the input waveform is sampled and stored on capacitors that are switched sequentially across a readout amplifier. Only one readout amplifier is needed for each channel, which dramatically reduces the power dissipation of the memory. During the write phase, switches S_1 , S_2 , and S_5 are closed, while S_3 and S_4 are open. The input

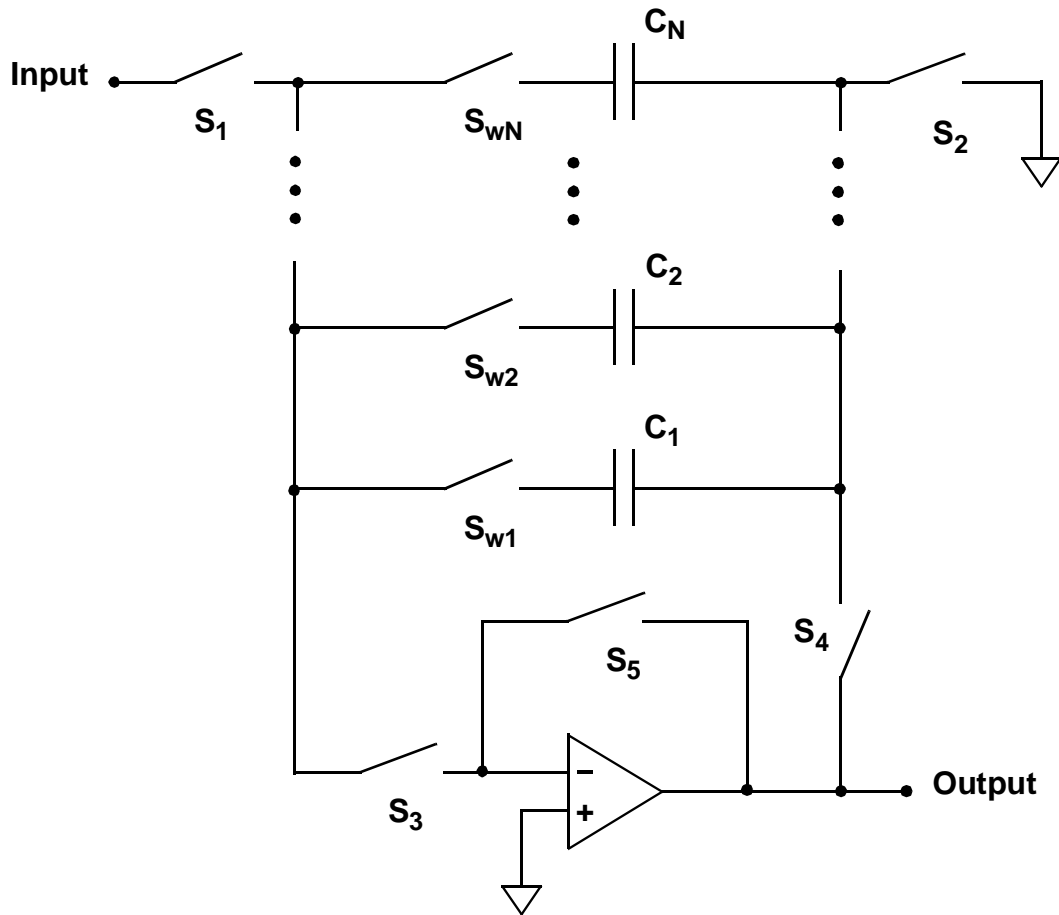


Figure 2.7: Bus-oriented architecture with one amplifier per channel. The voltage on the sampling capacitors is sensed during readout by switching the capacitors across the output amplifier.

waveform is then sampled and stored on the capacitors by sequentially closing and opening sampling switches S_{w1} through S_{wN} . After the input waveform has been recorded, switches S_1 and S_2 are opened and S_3 and S_4 are closed. Individual cells are then read out by sequentially closing and opening S_{w1} through S_{wN} so as to consecutively connect the cell capacitors across the readout amplifier. In order to reduce charge sharing effects, the reset switch S_5 is closed and opened in between readout of individual memory cells. Memory cell-to-cell gain and offset variations are dominated by sampling switch mismatch and are a function of the input signal level. The exact time when the signal is sampled is also dependent on the input level, which is a serious drawback for high-speed

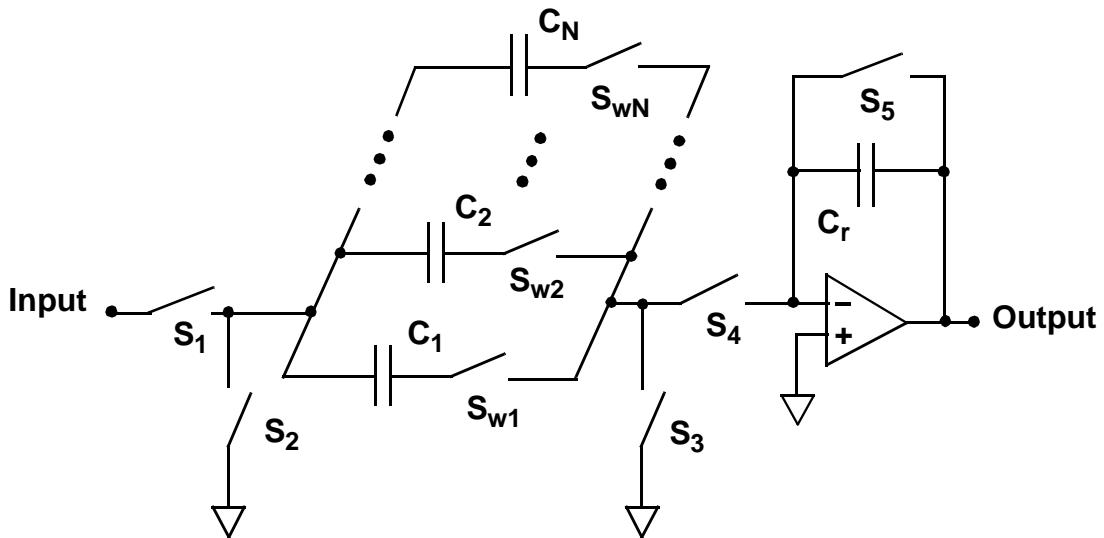


Figure 2.8: Bus-oriented architecture with one amplifier per channel. The charge stored on the sampling capacitors is transferred to capacitor C_r during readout.

applications. As discussed in Chapter 3, these memory cell response errors are a function of the input voltage because the cell sampling switches are inserted in the signal path, which also introduces nonlinearities. A circuit based on this architecture has been implemented, and a sampling rate of 50 MHz was achieved with a power dissipation of 10 mW [16, 17].

In the architecture depicted in Figure 2.7 the voltage across the sampling capacitors C_i is sensed during readout by switching the sampling capacitors across the output amplifier. In Figure 2.8 an alternative architecture is shown in which the charge stored on the sampling capacitors C_i is transferred during readout to a common capacitor, C_r , that is connected across the amplifier. In this architecture the analog input waveform is recorded by sequentially closing and opening switches S_{w1} through S_{wN} , while switches S_1 , S_3 , and S_5 are closed and S_2 and S_4 are open. During readout, S_1 and S_3 are opened and switches S_2 and S_4 are closed. The waveform is then read out by sequentially closing and opening switches S_{w1} through S_{wN} . In between the readout of two memory cells, the charge on C_r is reset by closing switch S_5 to avoid charge sharing. The cell-to-cell offset variations are

dominated by switch parameter mismatch. Gain deviations are governed by mismatch among the sampling capacitances since the output voltage of cell i , V_{oi} , is given by

$$V_{oi} = \left(\frac{C_i}{C_r} \right) V_{in}(t_i) + V_{offi} . \quad (2.11)$$

A circuit based on this concept has been realized, and a sampling frequency of 10 MHz was achieved with a measured gain nonuniformity of 0.5%, limited by capacitor size mismatch [18, 19].

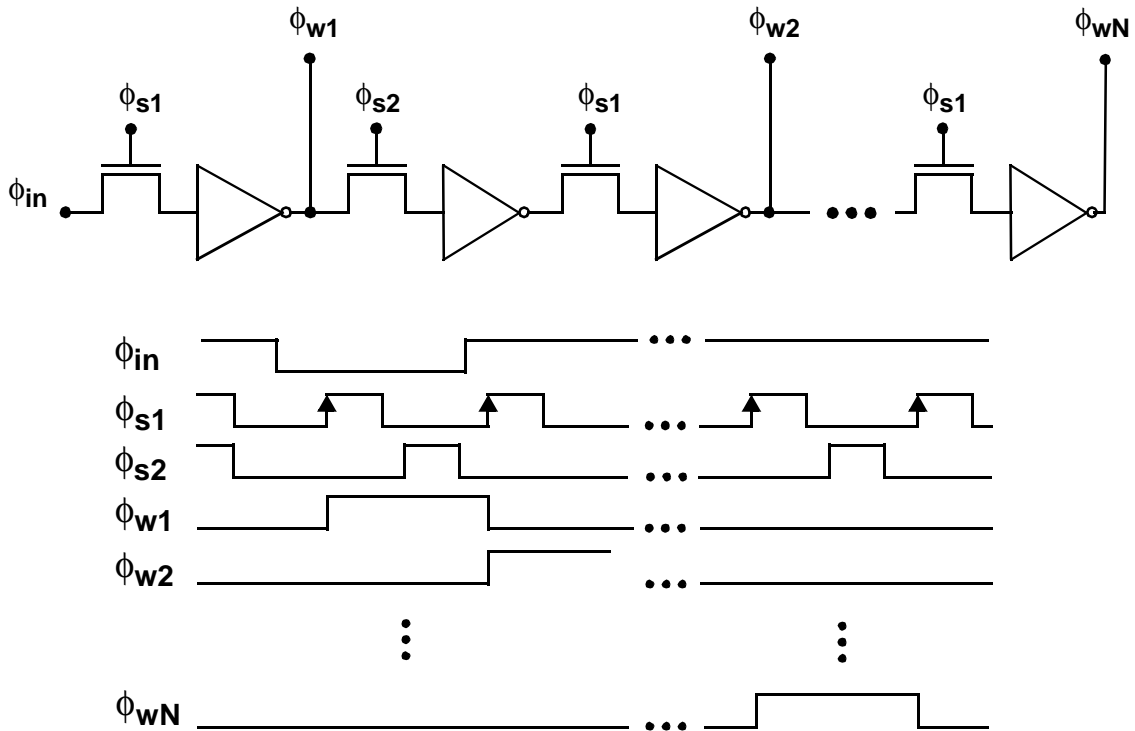


Figure 2.9: Dynamic two-phase shift register with timing diagram.

2.5 Analog Memory Write Control

The sampling rate at which an input signal can be recorded in an analog memory is, in practice, often limited by the speed of the write control circuit. The write address function for analog memory circuits is typically provided by an on-chip static or dynamic shift register. Figure 2.9 illustrates one of the simplest shift register configurations, a two-phase dynamic shift register [24], along with the timing diagram. In this figure, ϕ_{s1} and ϕ_{s2} are the two nonoverlapping clocks controlling the shift register, and ϕ_{in} is the serial input to the register. Signals ϕ_{w1} through ϕ_{wN} are the write address control signals for the analog storage section, as introduced in Figure 2.1.

The shift register is initialized by raising both of the clocks, ϕ_{s1} and ϕ_{s2} , and the serial input ϕ_{in} high, as shown in Figure 2.9. This sets the write address signals ϕ_{w1} through ϕ_{wN} to their low state. The write control proceeds as follows. The serial input ϕ_{in} is set low, and with a raising edge of clock ϕ_{s1} , the first write address ϕ_{w1} becomes high. After clock ϕ_{s1} is returned to low, a ϕ_{s2} pulse advances the logic level of ϕ_{in} to the second inverter in the register. The serial input ϕ_{in} is then raised to the high state and, after another ϕ_{s1} pulse, the first address signal, ϕ_{w1} , goes low, while the second address signal, ϕ_{w2} , goes high. Consecutive clock pairs, ϕ_{s1} and ϕ_{s2} , advance the logic levels within the shift register until the last write address control signal, ϕ_{wN} , rises and falls, as illustrated in Figure 2.9. It is important to note that the shortest period the nonoverlapping shift-register clocks must stay high is determined by the time required to adequately charge or discharge the inverter input gate capacitances through the pass transistors. The minimum time between two successive write clocks is therefore simply two inverter delays plus the timing overhead required to ensure that the shift-register clocks are nonoverlapping.

Shown in Figure 2.10 is one stage of a typical static shift register. In this register, the serial input, ϕ_{in} , is advanced through the shift register by nonoverlapping clocks ϕ_{s1} and ϕ_{s2} . The circuit is static because the state of the register is held via the feedback pass transistors across two successive inverter stages. For both dynamic and static shift registers, acquisition speeds exceeding 150 MHz are difficult to realize in MOS technology.

In order to circumvent the speed limitations of an on-chip shift register, a write control circuit wherein the write address signals, ϕ_{w1} through ϕ_{wN} , are driven by off-chip, high-speed drivers has been used [20, 23]. However, such an approach requires elaborate auxiliary circuitry, and sampling rates greater than 200 MHz are not practical for CMOS logic swings. To achieve waveform sampling rates of several hundred MHz, some alternative on-chip approach for write control must be devised; such a circuit is described in Chapter 4.

2.6 Comparison with Direct Digital Conversion

The nature of an analog waveform memory dictates its use in applications where a continuous digitization is not mandatory and the analog information need only be recorded over

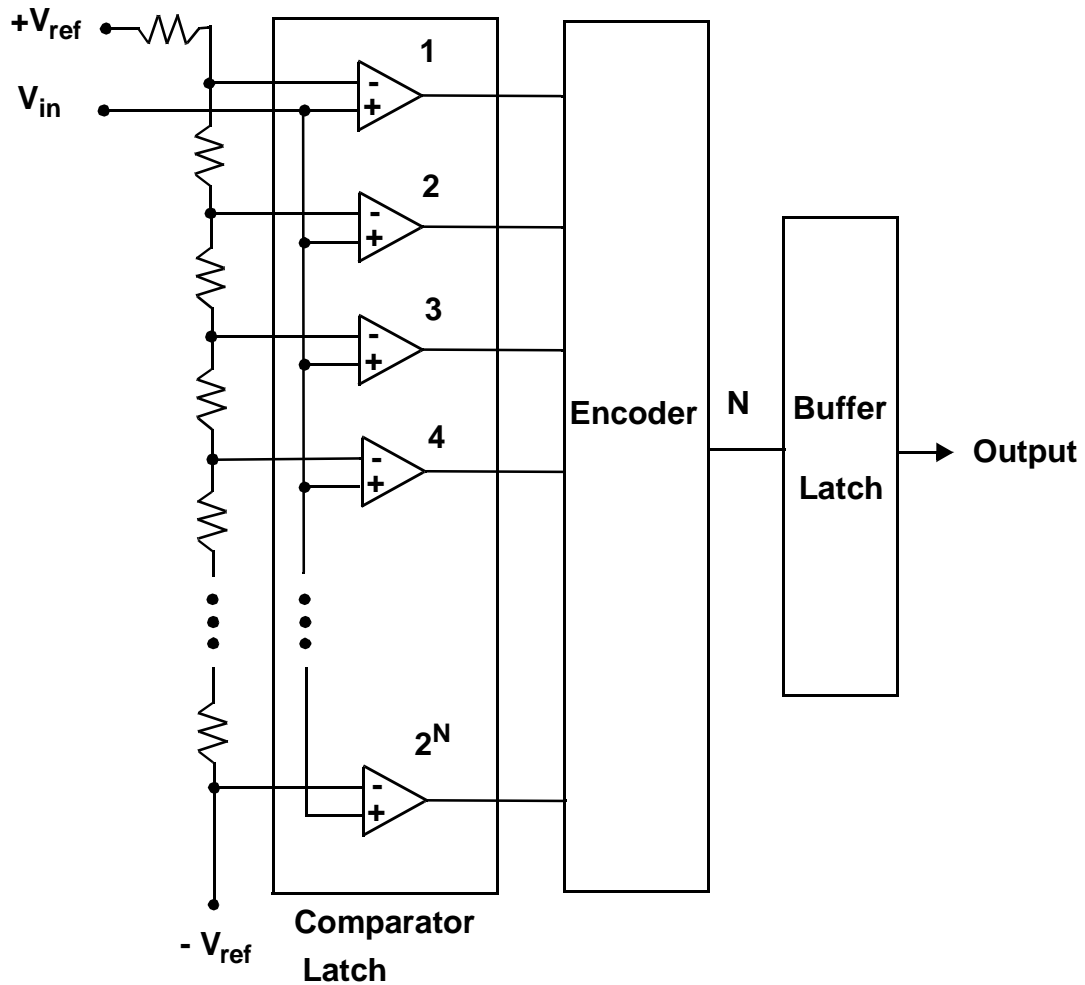


Figure 2.11: Flash analog-to-digital converter architecture.

provides higher resolution at higher sampling rates and orders of magnitude lower power dissipation. In addition, the speed requirements imposed by flash converters on the subsequent digital memory bank for data storage are removed.

2.7 Performance Parameter Definitions

The performance of an analog memory is typically characterized by a combination of parameters that are commonly used for sample-and-hold, amplifier, analog-to-digital con-

verter, and digital memory circuits. In this section, relevant dc and ac parameters are defined so as to avoid ambiguities.

- Amplifier input offset voltage

The dc input voltage required to provide zero voltage at the output of an amplifier.

- Pedestal voltage

The pedestal is the induced voltage step due to the switch charge injection onto the sampling capacitor when the sampling switch is turned off. The charge injection is the result of both capacitive coupling from the switch gate and charge trapped within the sampling switch.

- Pedestal variation

The pedestal variation is defined as the difference in the pedestal voltage of nominally identical sampling cells. The pedestal variation is mainly due to nonuniform charge injection onto the sampling capacitor from variations in sampling switch parameters.

- Dc gain error

Deviation in the voltage gain from unity, or a nominal gain, over the full scale voltage range.

- Integral linearity error

The maximum deviation from a linear fit to the output voltage versus the input voltage over the full-scale input voltage range, expressed as a percentage of the input voltage range.

- Write clock frequency

The write clock frequency, f_s , or sampling rate, is $1/t_s$, where t_s is the time between the turn-off of the write address switches in two adjacent memory cells.

- Acquisition time

The length of time that the write address switch must stay on in order to acquire a full scale step at the input to a specified accuracy.

- Record length

The record length for the acquired signal is the number of cells in a channel multiplied by the time between the turn-off of adjacent write switches; e.g. a 256-cell channel operated at a frequency of 200 MHz captures a record of 1.28 μ s length.

- Data acquisition cycle time

The data acquisition cycle time is the minimum time between two measurement cycles, which is the sum of the write time (or record length) and the readout time for one entire analog memory channel.

- Small-signal bandwidth

The small-signal bandwidth is the frequency at which the amplitude of the signal across the sampling capacitor is 3 dB less than the amplitude of a small signal sine wave at the input.

- Full power bandwidth

The full power bandwidth is the frequency at which the amplitude of the signal on the sampling capacitor is 3 dB less than the amplitude of a 95% full-scale sine wave at the input.

- Rms noise

The rms noise is defined as the square-root of the sum-of-squares of the residuals, i.e. differences from the average of repeated measurements.

- Thermal noise

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. A noise voltage is generated in the resistive component, R , of any impedance and has a value

$$\bar{v}_{th} = \sqrt{4kTR\Delta f}, \quad (2.12)$$

where v_{th} is the rms value of the noise voltage, k is the Boltzman's constant (1.38×10^{-23} Joules/K), T is the absolute temperature in Kelvin, and Δf is the bandwidth over which the noise is measured. Since the noise is related to the bandwidth over which the measurement is performed, the bandwidth must be specified.

- **Minimum detectable signal (MDS)**
Smallest input signal that the circuit can effectively detect or amplify. The MDS depends on the nature of the signal and the application. Without special filtering or coding techniques, the MDS considered here is equal to the input-referred rms noise voltage.
- **Dynamic range**
The ratio of a full-scale signal to the minimum detectable signal, usually expressed in dB or as an equivalent number of bits.
- **Effective precision**
The ratio of the amplitude of the input signal to the rms deviation from the ideal output value. For a given sampling rate the effective precision depends on the frequency of the input signal.
- **Signal-to-(noise+distortion) ratio**
A logarithmic expression of the ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth, including distortion components and timing errors, expressed in dB.
- **Droop rate**
The change in output voltage per unit of storage time as a result of leakage in the memory cells. The polarity depends on the source of leakage current within a given memory cell structure and is mainly the result of drain-to-substrate, drain-to-well, and sub-threshold drain-to-source leakage in MOS switches.

2.8 Summary

In this chapter the principle of analog waveform sampling through the use of analog memory circuits has been explained. Analog memories are suitable for applications where analog waveforms need only be captured over a limited period of time and where continuous digitization is not necessary. The waveform is sampled and stored at a high rate for a limited period of time, and subsequently retrieved at a lower rate and digitized. The memory essentially exploits the fact that the sampling and storage operation into a bank of analog

memory cells can be accomplished at a higher rate and with a higher resolution than a direct digital conversion.

In general, analog memory circuits are especially suitable for use in acquisition systems with hundreds or thousands of channels for which

- the number of components and interconnections must be minimized for cost, space, or reliability reasons, or
- low power dissipation is essential because of the location of the electronics in areas where heat extraction is difficult or because energy storage is limited (e.g. in portable electronic systems), or
- analog waveforms must be recorded at a very high rate with a large dynamic range.

This chapter has also reviewed several analog memory architectures. Implementations in which the sampling switch is placed in the signal path exhibit an input level dependent voltage error and may require individual cell offset, gain, and nonlinearity corrections. In addition, a serious drawback of these implementations in high-speed applications is the dependence of the sampling switch turn-off time on the signal level. In circuits based on traditional charge redistribution switched-capacitor techniques, charge injection can be made independent of the signal level, but the cell gain is a direct function of the size of the sampling capacitor. Hence, the memory cell gain matching across a channel is, in such an architecture, limited to the achievable capacitance matching.

A circuit architecture that allows for sampling at rates of several hundred MHz while avoiding input signal dependent voltage inaccuracies and gain errors directly related to component mismatch will be presented in Chapter 4. First, however, the main elements of an analog memory, the integrated capacitor and the MOS transistor switch, and their characteristics when configured as a sample-and-hold circuit are investigated in the following chapter.

Chapter 3

Analog Memory Cell Technology

3.1 Overview

The implementation of the basic function of an analog memory cell, the sampling and storage of analog information, calls for the availability of zero-offset, low-leakage switches. The prime monolithic component satisfying this requisite is the MOS transistor, which also provides a high impedance control terminal desirable for charge storage. In this chapter the operation of the MOS transistor is investigated with emphasis on its use in sample-and-hold configurations.

One of the drawbacks of MOS switches is that error voltages are introduced at turn-off of the devices [34, 35, 36, 37]. These errors are expressed in Section 3.3 and Section 3.4 for MOS transistors and CMOS transmission gates as a function of the circuit parameters. The storage of the sampled signal is accomplished by means of monolithic capacitors, and in Section 3.5 several implementations of these components are reviewed. For many analog memory applications the uniformity of the memory cell transfer characteristic within a channel is of much greater concern than the absolute channel offset and gain. The parameters limiting this uniformity are discussed in Section 3.6.

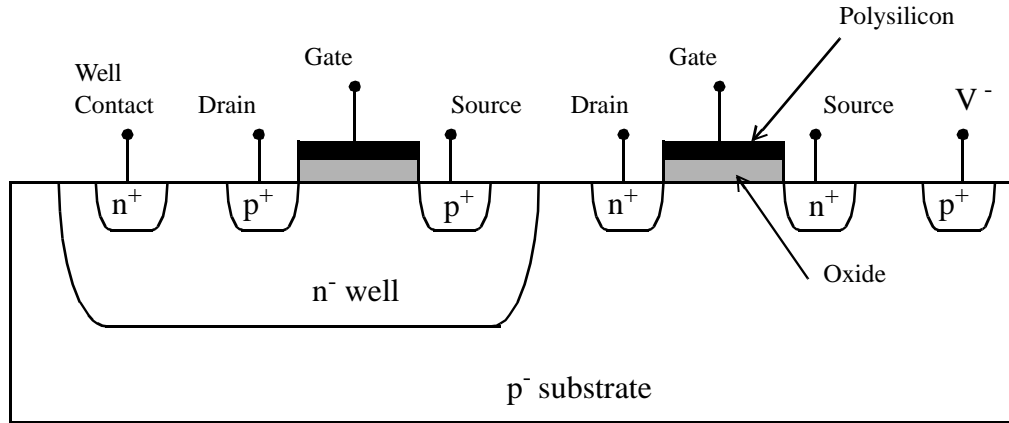


Figure 3.1: Cross section of PMOS and NMOS transistor in a n-well CMOS technology.

3.2 CMOS Technology

One of the significant advantages of MOS technologies is that they provide a low on-resistance, high off-resistance, low leakage switch, the MOS transistor. Shown in Figure 3.1 is a simple cross section of NMOS and PMOS transistors in an n -well technology. The NMOS or n -channel transistor is formed with two heavily doped n^+ regions diffused in a lighter doped p -substrate. The two n^+ terminals are interchangeable and are called source and drain. The terminal at lower potential is identified as the source. The channel between the source and drain region is separated from the gate control terminal by a thin dielectric layer. As long as the voltage applied to the gate is less than a threshold voltage, V_T , above the lowest voltage applied at the source or drain, the n^+ regions are separated by back-to-back diodes and the transistor is off. When the bias applied at the gate exceeds V_T , an inversion layer of minority carriers (electrons) is formed underneath the gate. A conductive path between the source and drain is established and the transistor is turned on.

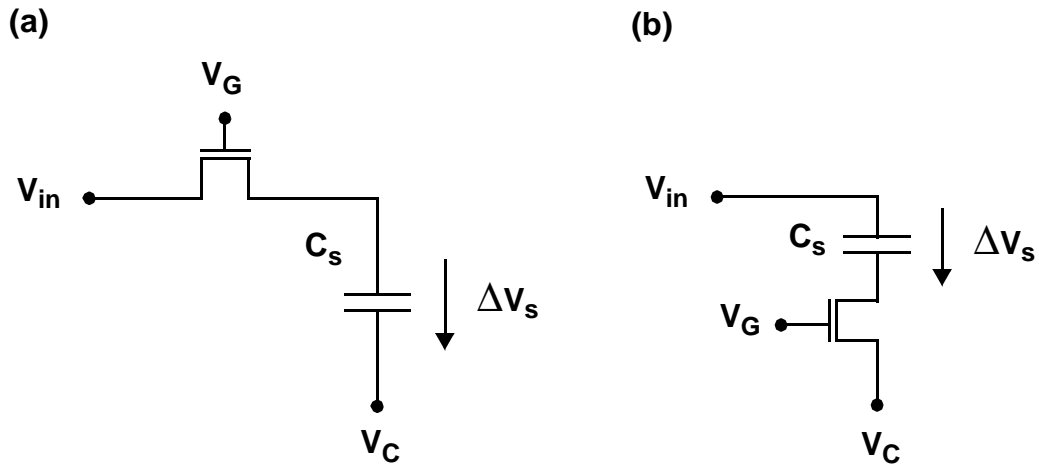


Figure 3.2: NMOS transistor placed in the (a) signal and (b) signal-return path.

The PMOS or p -channel transistor is formed similarly to the NMOS switch by inverting the doping polarities. The transistor is conducting as long as the gate bias is more than a threshold voltage below the highest potential of the source/drain region. Essentially both NMOS and PMOS transistors are four terminal devices. The p -substrate is common throughout the integrated circuit and is connected to the most negative voltage, V^- , whereas many n -wells can be fabricated on one chip connected to different circuit nodes depending on the application.

3.3 The NMOS Transistor as a Voltage Switch

3.3.1 Switch Resistance and Voltage Error

In an analog memory cell, the MOS transistor acts as a voltage switch and can be inserted in the signal or in the signal-return path. In Figure 3.2 two simple sample-and-hold configurations utilizing an NMOS transistor and a storage capacitor are shown. As long as the switches are conducting, the voltage across the storage capacitor C_s tracks the difference

between the input voltage V_{in} and the dc reference voltage V_C . The time constant, τ , with which the voltage across C_s follows a change in the input voltage depends on the on-resistance, R_{DS} , of the sampling switch and the size of the capacitor,

$$\tau = R_{DS}C_s. \quad (3.1)$$

For small drain-to-source voltages the transistor is in the linear region ($V_{GS} - V_T > V_{DS}$), and the current through the device is given by

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}, \quad (3.2)$$

where V_{GS} is the gate-to-source voltage, μ_n is the electron mobility in the channel, and W and L are the width and length of the channel. C_{ox} is the oxide capacitance per unit area.

The on-resistance of the channel can be approximated by

$$R_{DS} = \frac{1}{\frac{dI_{DS}}{dV_{DS}}} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)}. \quad (3.3)$$

The resistance of the channel is thus inversely proportional to the ratio of the width W over the length L of the channel. Furthermore, the resistance is nonlinear since it depends on the gate-to-source voltage.

The NMOS transistor turns off when the gate voltage drops to less than the threshold voltage above the source potential. Ideally, the voltage across the sampling capacitor in Figure 3.2 after turn-off is given by $\Delta V_s = V_{in} - V_C$. However, for fast sampling systems the result is perturbed by two principle error sources: the switch gate-overlap capacitance, C_{ov} , and charge, Q_{ch} , in the transistor channel.

The magnitude of the induced error voltage differs for the two cell arrangements depicted in Figure 3.2. In the configuration shown in Figure 3.2(a), the error voltage e_{ov} due to the overlap capacitance takes the form

$$e_{ov} = -\frac{C_{ov}}{C_{ov} + C_s} (V_{in} + V_T - V_L), \quad (3.4)$$

where V_L is the low level gate voltage, and C_{ov} is the parasitic capacitance between the gate and the source or drain of the transistor.

The total charge Q_{ch} in the channel of the transistor before turn-off is given by

$$Q_{ch} = -C_{ox}WL(V_H - V_{in} - V_T), \quad (3.5)$$

where V_H is the high level voltage of the gate control signal. At turn-off, a fraction of this charge is trapped in the channel,

$$Q_{tr} = \alpha_{tr}Q_{ch}. \quad (3.6)$$

The value for the coefficient α_{tr} , $0 \leq \alpha_{tr} \leq 1$, depends on the fall time of the gate voltage, t_f , and the channel transit time, τ_o . It reaches its maximum when t_f is short compared to τ_o [34, 35, 36, 37]. The fraction of the trapped charge that is subsequently injected onto the sampling capacitor depends on the impedances at the source and drain terminals of the transistor and is one half for equal impedances. A mismatch of these impedances changes the amount of injected charge

$$Q_{inj} = \alpha_m \frac{Q_{tr}}{2}, \quad (3.7)$$

where α_m , $0 \leq \alpha_m \leq 2$, is the impedance mismatch factor. As the impedance of the signal source driving the circuit increases, less channel charge returns to that end of the transistor and Q_{inj} becomes larger [34, 35, 36]. For equal source and drain impedances, α_m equals one.

In circuits where the fall time of the gate voltage is comparable to the channel transit time and where the impedances are not matched, the calculation of charge injection is impractical and often a worst case condition is assumed.

If it is assumed that the driving source impedances at nodes V_{in} and V_C in Figure 3.2 are identical, the coefficients α_{tr} and α_m are the same for both circuit configurations. For

the circuit in Figure 3.2(a), the voltage error, e_{ch} , due to the injected channel charge becomes

$$e_{ch} = \frac{Q_{inj}}{C_s} = \alpha \frac{Q_{ch}}{2C_s}, \quad (3.8)$$

where $\alpha = \alpha_m \alpha_{tr}$. With (3.5) the voltage error becomes

$$e_{ch} = -\frac{\alpha C_{ox} WL}{2C_s} (V_H - V_{in} - V_T). \quad (3.9)$$

The voltage across the cell capacitor in Figure 3.2(a), ΔV_s , after turn-off of the sampling switch is

$$\Delta V_s = V_{in} - V_C + V_{ped}, \quad (3.10)$$

where the pedestal voltage

$$V_{ped} = e_{ov} + e_{ch}. \quad (3.11)$$

The voltage errors e_{ov} and e_{ch} can be split into a gain error and an offset,

$$V_{ped} = \epsilon V_{in} + V_{of}. \quad (3.12)$$

The gain error in the circuit is

$$\epsilon = -\frac{C_{ov}}{C_{ov} + C_s} + \frac{\alpha C_{ox} WL}{2C_s}, \quad (3.13)$$

while the offset voltage is

$$V_{of} = -\frac{C_{ov}}{C_{ov} + C_s} (V_T - V_L) - \frac{\alpha C_{ox} WL}{2C_s} (V_H - V_T). \quad (3.14)$$

It is apparent from (3.10) through (3.13) that for the circuit configuration shown in Figure 3.2(a) the error voltage impressed on the sampling capacitor during turn-off depends on the input signal level.

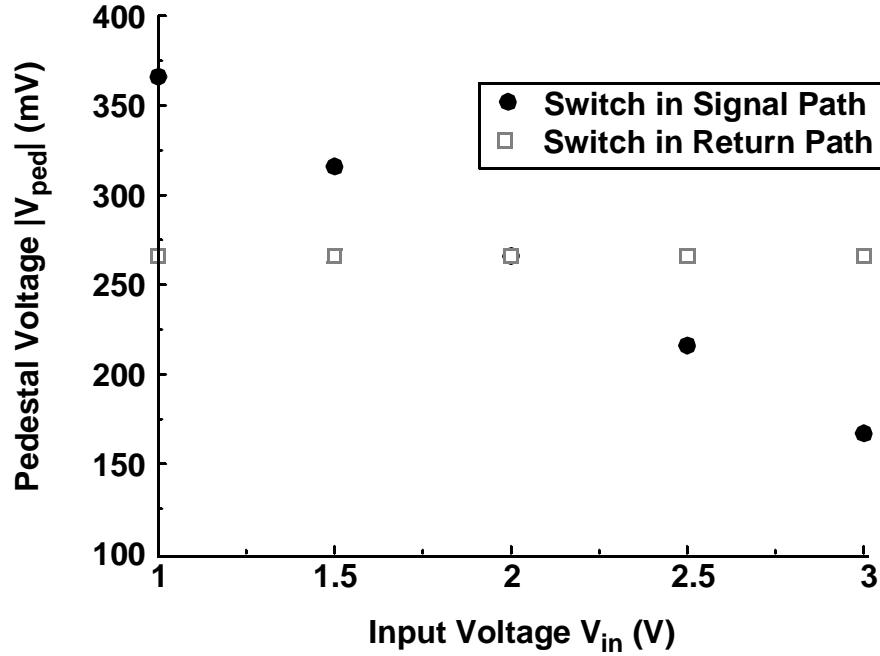


Figure 3.3: Pedestal voltage as a function of input voltage.

The circuit shown in Figure 3.2(b) can be analyzed in the same manner as the circuit in Figure 3.2(a), with the result that the voltage ΔV_s following turn-off of the sampling switch can be written as

$$\Delta V_s = V_{in} - V_C + V_{of}, \quad (3.15)$$

where

$$V_{of} = \frac{C_{ov}}{C_{ov} + C_s} (V_C + V_T - V_L) + \frac{\alpha C_{ox} WL}{2C_s} (V_H - V_T - V_C). \quad (3.16)$$

As is evident from these equations, the input signal dependence that was present in the Figure 3.2(a) switch configuration is avoided.

Shown in Figure 3.3 are the results of PSPICE [38] simulations demonstrating the difference between the two circuits when they are implemented in a typical 2- μm CMOS

technology. The absolute values of the simulated pedestal voltages, $V_{ped} = \Delta V_s - (V_{in} - V_C)$, are plotted as a function of the input voltage for the two circuit configurations. The width of the switch was 50 μm , the channel length was 2 μm , and the size of the sampling capacitance was 0.5 pF. The circuit input was driven by an ideal voltage source, and the gate control voltage fell from 5 V to 0 V in 0.3 ns. The pedestal voltage varies by 200 mV across an input voltage range of 2 V with the switch inserted in the signal path (Figure 3.2(a)), whereas it is constant for the alternative configuration (Figure 3.2(b)).

3.3.2 Distortion and Timing Errors

In the preceding section, the responses of two sample-and-hold cells to dc input signals were evaluated. For ac input signals, two additional error sources must be taken into account: the potential input voltage dependency of the sampling instant, and the signal dependency of the switch resistance.

The finite slew rate of the sampling clock transition causes an input level dependence in the sampling instant, and therefore sampling time errors, in the circuit shown in Figure 3.2(a). This process is illustrated in Figure 3.4 for a pulse input with an amplitude of A_s and rise and fall times of t_{tr} . The fall time of the gate control signal is t_f and its amplitude A_{clk} . The input MOS transistor turns off when the gate control voltage falls below a threshold voltage above the source/drain potential, which is equal to the input signal level. Hence, the input transistor turns off earlier for high level input signals as compared to low level inputs. The time t_s' when the signal is actually sampled is related to the ideal sampling instant t_s as follows:

$$t_s' = t_s + (A_{clk} - V_{in} - V_T) \frac{t_f}{A_{clk}} . \quad (3.17)$$

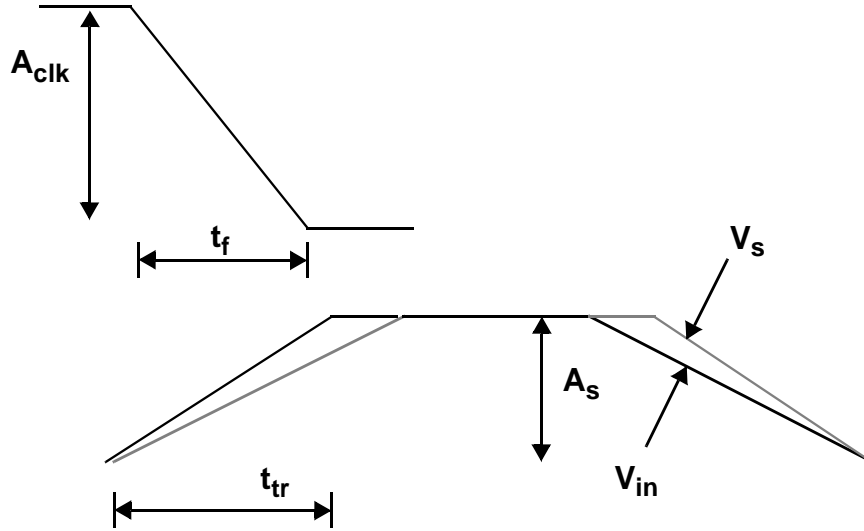


Figure 3.4: Input voltage level dependent sampling time.

The input signal dependent term in (3.17) causes the resulting signal slope dV_s/dt to be smaller for rising input signals and larger for falling signals, as indicated with dashed lines in Figure 3.4. The dependence of dV_s/dt on dV_{in}/dt can be expressed as

$$\frac{dV_s}{dt} = \left(1 - \frac{A_s t_f}{t_{tr} A_{clk}} \right) \frac{dV_{in}}{dt}, \quad (3.18)$$

where A_s/t_{tr} is positive for a rising input signal and negative for a falling input signal.

For sinusoidal input signals, $V_{in} = A_s \sin 2\pi f t$, the input level dependency of the sampling time leads to harmonic distortion, and the output waveform V_s can be approximated by

$$V_s = A_s \sin 2\pi f \left(t - \frac{A_s}{A_{clk}} t_f \sin 2\pi f t \right). \quad (3.19)$$

The second effect leading to signal distortion for the switch configuration shown in Figure 3.2(a) is the dependency of the switch resistance on the input signal level. The time

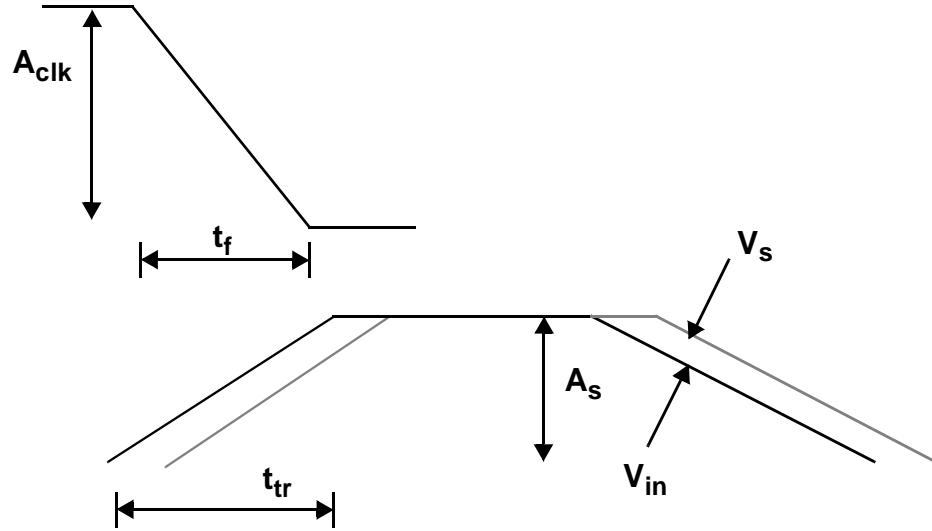


Figure 3.5: Input voltage independent sampling time.

constant with which the voltage across the sampling capacitor follows the input signal is $\tau = R_{DS}C_s$, where the switch resistance is a nonlinear function of the input voltage (3.3). For ac waveforms the signal across the sampling capacitor is therefore distorted. The magnitude of the error voltage depends on the amplitude and frequency of the ac input signal. The sample-and-hold configuration wherein the switch is inserted in the signal path thus introduces both input level dependent timing errors and signal distortion.

For the circuit of Figure 3.2(b), where the sampling switch is placed in the signal-return path, the effective sampling instant is given by

$$t_s' = t_s + (A_{clk} - V_C - V_T) \frac{t_f}{A_{clk}}. \quad (3.20)$$

Thus, there is a constant time delay for pulse inputs, as illustrated in Figure 3.5, and a constant phase shift for input sine waves. As a conclusion, the circuit in Figure 3.2(b) exhibits superior performance in respect to amplitude and timing errors, since both switch

terminals remain at a constant potential for signal frequencies below the bandwidth of the sampling cell.

It should be noted that an analog memory using a sample-and-hold cell as shown in Figure 3.2(b) requires some means of disconnecting the signal input from the sampling capacitor so that the voltage sampled and stored across the sampling capacitor can be sensed during readout. In addition, the circuit must be designed to minimize the influence of the parasitic plate capacitances of the sampling capacitor. An analog memory employing the sample-and-hold circuit in Figure 3.2(b) is described in Chapter 4.

3.4 The CMOS Transmission Gate

The presence of PMOS transistors in a CMOS technology allows for a switch configuration commonly called a CMOS transmission gate. An NMOS and a PMOS transistor are connected in parallel to form a complementary switch. Such a switch requires the generation of complementary control signals, which is a drawback for the design of high speed sampling circuits, as is discussed in Chapter 4. In the following sections the resistances and error voltage terms for the complementary switch are described.

3.4.1 CMOS Switch Resistance

In Figure 3.6 two basic sample-and-hold configurations employing CMOS switches and capacitors are shown. The resistance of the PMOS switch is

$$R_{DSp} = \frac{1}{\frac{dI_{DSp}}{dV_{DSp}}} \approx \frac{1}{\mu_p C_{ox} \frac{W}{L} (-V_{GSp} + V_{Tp})}, \quad (3.21)$$

where μ_p is the hole mobility. The gate-to-source voltage V_{GSp} and the threshold voltage V_{Tp} are negative.

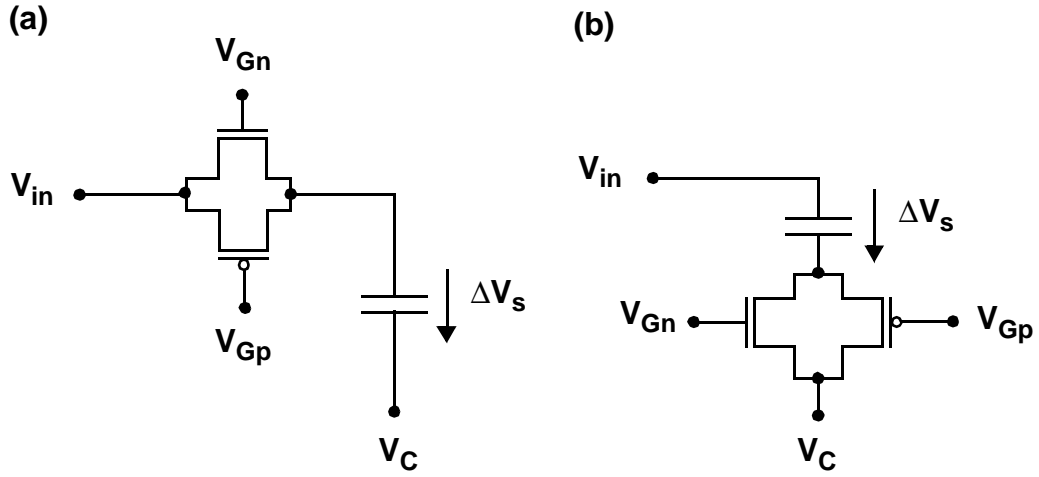


Figure 3.6: CMOS switch in (a) signal and (b) signal-return path.

The conductance of the complementary CMOS switch is simply the sum of the individual NMOS and PMOS conductances

$$\frac{1}{R_{DS}} \approx \mu_n C_{ox} \frac{W_n}{L_n} (V_{GSn} - V_{Tn}) + \mu_p C_{ox} \frac{W_p}{L_p} (-V_{GSp} + V_{Tp}) \quad (3.22)$$

With $V_{GSn} = V_{Gn} - V_S$, $V_{GSp} = V_{Gp} - V_S$, and $V_{Tn} = -V_{Tp} = V_T$, this equation can be rewritten as

$$\frac{1}{R_{DS}} \approx g_1 - \left(\mu_n C_{ox} \frac{W_n}{L_n} - \mu_p C_{ox} \frac{W_p}{L_p} \right) V_S \quad (3.23)$$

where g_1 is a term independent of the source voltage V_S ,

$$g_1 = \mu_n C_{ox} \frac{W_n}{L_n} (V_{Gn} - V_T) + \mu_p C_{ox} \frac{W_p}{L_p} (-V_{Gp} + V_H - V_T) \quad (3.24)$$

For the circuit shown in Figure 3.6(a), V_S is equal to the input signal voltage, V_{in} , and the conductance of the transmission gate therefore depends on the input signal level, as

expressed in (3.23). However, the second term in this equation can be eliminated by choosing the W/L ratios of the transistors according to their carrier mobility ratio

$$\frac{W_n L_p}{L_n W_p} = \frac{\mu_p}{\mu_n} . \quad (3.25)$$

In practice, a fraction of the input level dependence will remain since the ratio of the carrier mobilities cannot be accurately controlled in the fabrication process.

In Figure 3.6(b) the CMOS switch is placed in the return path of the signal, and the source voltage, V_S , in (3.23) is equal to the dc reference voltage V_C . The switch conductance is then independent of the applied input signal level for all transistor sizes.

3.4.2 Error Voltage

If it is assumed that the two complementary switches in Figure 3.6 turn off simultaneously, then the error voltages introduced by the NMOS and PMOS transistors can be summed. For the circuit configuration in Figure 3.6(a), the voltage, ΔV_s , sampled across the storage capacitor becomes

$$\Delta V_s = V_{in} - V_C + V_{ped} \quad (3.26)$$

with

$$V_{ped} = e_{ovn} + e_{chn} + e_{ovp} + e_{chp} . \quad (3.27)$$

The error voltages e_{ovp} and e_{chp} at turn-off of a PMOS transistor can be derived in a similar fashion to those for the NMOS transistor with the following result:

$$e_{ovp} = \frac{C_{ov}}{C_{ov} + C_s} (V_H - V_{in} - V_{Tp}) \quad (3.28)$$

$$e_{chp} = \frac{\alpha C_{ox} W_p L_p}{2C_s} (V_{in} + V_{Tp} - V_L) . \quad (3.29)$$

With the approximation that the magnitudes of the threshold voltages are identical for both transistor types, the pedestal voltage at turn-off can be written as follows.

$$V_{ped} = \varepsilon V_{in} + V_{of}, \quad (3.30)$$

where the gain error is

$$\varepsilon = (W_p L_p + W_n L_n) \frac{\alpha C_{ox}}{2C_s} - \frac{2C_{ov}}{C_{ov} + C_s}, \quad (3.31)$$

and the offset voltage component is

$$V_{of} = -(W_p L_p V_L + W_p L_p V_T + W_n L_n V_H - W_n L_n V_T) \frac{\alpha C_{ox}}{2C_s} + \frac{C_{ov}}{C_{ov} + C_s} (V_H + V_L) \quad (3.32)$$

If the logic high and low levels are symmetric about zero, and $W_p L_p = W_n L_n$ for the CMOS switch, then the expression for the pedestal voltage is reduced to

$$V_{ped} = \left(\frac{\alpha C_{ox} W_n L_n}{C_s} - \frac{2C_{ov}}{C_{ov} + C_s} \right) V_{in}. \quad (3.33)$$

The pedestal introduced in the circuit shown in Figure 3.6(b) can be evaluated in a similar fashion with the result that the pedestal voltage in (3.26) is independent of the input signal level:

$$V_{ped} = -(W_p L_p (V_C - V_L - V_T) + W_n L_n (V_C - V_H + V_T)) \frac{\alpha C_{ox}}{2C_s} - V_{ov} \quad (3.34)$$

with

$$V_{ov} = -\frac{2C_{ov}}{C_s + C_{ov}} (V_C - V_H - V_L). \quad (3.35)$$

Under the condition that $V_H = -V_L$ and $W_p L_p = W_n L_n$, V_{ped} for this circuit simplifies to

$$V_{ped} = -\left(\frac{\alpha C_{ox} W_n L_n}{C_s} - \frac{2C_{ov}}{C_{ov} + C_s}\right)V_C. \quad (3.36)$$

Note that the pedestal voltages have opposite signs for the two switch configurations.

As is the case for a single transistor switch, the circuit configuration with the switch in the signal path has a pedestal voltage that is dependent on the input signal voltage (3.33), whereas V_{ped} is constant when the switch is inserted in the signal-return path (3.36).

In this section it was assumed that the two complementary switches turn off simultaneously and part of the injected channel charge thus cancels. In practice, this is hard to accomplish, and the error voltages may be larger than suggested by (3.33) and (3.36).

3.5 Capacitors

The performance of an analog memory depends on the quality of capacitor structures available in the integrated circuit technology. Important issues are the matching of nominally identical capacitors and the absolute sizes and matching of associated parasitic capacitances. Capacitors suitable for analog circuit design can be classified into two categories. The first type employs the capacitance between a metal or polysilicon layer and the single-crystal silicon substrate, separated by an SiO_2 dielectric layer. In order to achieve a low voltage coefficient, dC/dV , the single-crystal silicon must be heavily doped, which generally requires an extra implantation step in conventional self-aligned fabrication processes. Typical values for the capacitor and its associated bottom plate parasitic capacitance in a 1.2- μm CMOS technology are 1.2 $\text{fF}/\mu\text{m}^2$ and 0.5 $\text{fF}/\mu\text{m}^2$, respectively [39]. The voltage coefficient is on the order of $1.5 \times 10^{-3} \text{ fF}/\mu\text{m}^2\text{V}$. The second type of capacitor uses the capacitance between metal or polysilicon and polysilicon. The advantage of this capacitor structure is its low voltage dependence. A typical value for the capacitance in a 2- μm CMOS technology with explicit poly-to-poly capacitors is 0.5 $\text{fF}/\mu\text{m}^2$, while the associated bottom plate parasitic capacitance is 0.05 $\text{fF}/\mu\text{m}^2$ [40].

3.6 Matching of Sampling Cell Performance

In many analog memory applications, the uniformity of the memory cell response in one channel is much more important than the absolute channel offset and gain. The uniformity is affected by two principal sources of error: inaccuracies in the fabrication process [41]-[43] and control signal feedthrough.

Although the memory cells are designed to be nominally identical, the degree of component matching is limited by imperfections in the fabrication process. Capacitor matching is determined by variations in the area of the capacitor plates and the thickness of the dielectric. The matching of transistor characteristics on a chip is determined by the matching of threshold voltages, mobilities, oxide and gate-overlap capacitances, and the widths and lengths of the transistor gates. The main contribution to cell response variations within a memory channel is the mismatch in the charge injected during turn-off of the switch. Under fast turn-off conditions the variation in channel charge dominates the charge injection mismatch [42] and can be modeled as part of the mismatch of two geometric parameters, the channel width and length.

The difference in channel area, $\delta(WL)$, of two mismatched transistors is

$$\delta(WL) = (W + \delta W)(L + \delta L) - WL \quad , \quad (3.37)$$

where δW and δL are the variations in channel width and length. With the approximation that $\delta W = \delta L \equiv \delta P$, it follows from (3.9) that the pedestal error voltage, δV_{ped} , can be approximated as

$$\delta V_{ped} \approx \frac{\alpha C_{ox}(W + L)\delta P}{2C_s}(V_H - V_S - V_T) \quad , \quad (3.38)$$

where $V_S = V_{in}$, and $V_S = V_C$ for the circuit configurations shown in Figure 3.2(a) and Figure 3.2(b), respectively. The voltage error due to nonuniform charge injection, δV_{ped} , is thus proportional to the channel width and length of the sampling transistor. This implies

that the size of the error voltage and the input time constant, given by (3.1), are related. If it is assumed that $W \gg L$, the time constant τ can be approximated as

$$\tau = R_{DS}C_s \approx \frac{\alpha L \delta P}{2\mu_n \delta V_{ped}}. \quad (3.39)$$

Thus, switches with smaller W/L ratio yield smaller pedestal mismatches but limit the signal bandwidth of the sampling cell.

Often CMOS switches are employed to reduce the absolute pedestal voltage introduced at turn-off of the sampling switch, as discussed in Section 3.4. However, the use of CMOS switches does not improve the matching of the sampling cell performance, since the pedestal error voltages δV_{ped} of the PMOS and NMOS transistors are independent and the resulting pedestal error is therefore not cancelled. Assuming that the mismatch of the PMOS and NMOS devices is uncorrelated, the situation actually worsens because the total error voltage is then given by the square-root of the sum of the squares of the individual error voltages. This situation also applies to the use of “dummy” switches for the cancellation of the injected charge.

Another potential source of non-uniformity of the pedestal voltages resulting from charge injection mismatch is the variation in sampling capacitance. The voltage error δV_{erc} from charge injection onto two mismatched capacitors can be written as

$$\delta V_{erc} = \frac{\alpha Q_{ch}}{2} \left(\frac{1}{C_s} - \frac{1}{C_s + \delta C_s} \right) \approx \frac{\alpha Q_{ch}}{2C_s} \left(\frac{\delta C_s}{C_s} \right), \quad (3.40)$$

where δC_s is the variation in the sampling capacitance and Q_{ch} is defined in (3.5). Typically, this error is small compared to the error from the mismatch of the sampling switches and can therefore be neglected.

The uniformity of the sampling cell transfer characteristics is also affected by feedthrough of control signals via the substrate and parasitic inter-layer capacitances. In analog memories, the input waveform is sampled sequentially onto a bank of memory cells. The capacitive coupling from control signal lines to individual memory cell nodes may not be uniform across the chip. The architecture and layout of the circuit must be carefully designed so as to minimize coupling through parasitic inter-layer capacitances

and through the substrate. In addition, perturbations (e.g. ringing) on common power, ground, signal, or signal-return buses, induced by control signals, can be the cause of memory cell performance mismatch, since the signal is captured at different times in the memory cells of the channel.

3.7 Summary

The MOS transistor is an important building block in analog memory circuits because of its high off-resistance, low on-resistance, and zero offset when used as a switch. Together with monolithic capacitors, MOS switches provide the basic sample-and-hold function needed to acquire and store analog waveforms. A voltage switch can be realized by means of a single NMOS or PMOS transistor, or with a CMOS transmission gate. One of the limitations of MOS switches is that error voltages are introduced during turn-off of the devices. The CMOS transmission gate shows a lower absolute error voltage when compared to a single MOS transistor because of the cancellation of two opposite-signed switch charges injected by the PMOS and NMOS transistors. However, transmission gates require complementary control signals, which are especially a burden on high speed designs. In addition, the uniformity of the individual memory cell responses in one channel is generally more important than the absolute error voltage. This uniformity does not benefit, but rather actually worsens if CMOS transmission gates are used.

A voltage switch can be inserted in the signal or signal-return path of the sample-and-hold cell. With the latter approach the error voltages introduced at turn-off are independent on the input signal level and can therefore be cancelled by a simple subtraction procedure. Furthermore, the turn-off timing instant is also independent of the input signal level, which eliminates the sampling time error present when the switch is used in the signal path.

The analysis of sample-and-hold configurations presented in this chapter provides a basis for the design of an analog memory circuit for high speed applications, as proposed in the following chapter.

Chapter 4

Analog Memory Circuit Design

4.1 Overview

A number of analog memory circuit architectures were presented and described in Chapter 2. These circuits can be classified into two main categories: those where the memory cell amplitude and timing errors are a function of the input signal level, and those where the memory cell gain uniformity within a signal channel is limited by the achievable level of matching of its constituent capacitors. In this chapter, an architecture for an analog memory is proposed that circumvents both of these limitations. A circuit implementation of the architecture and its theoretical performance are investigated in detail. A high-speed write control circuit for the analog memory is presented in Section 4.3.

Shown in Figure 4.1 is a block diagram of an analog waveform recorder with M memory channels. The analog waveforms applied at the M inputs are sampled and stored in the main analog memory core. The write and read addresses for the core are generated in the write and read control blocks, respectively. The architecture and circuit implementations of the analog memory core, the write control, and the read control are described in the following sections.

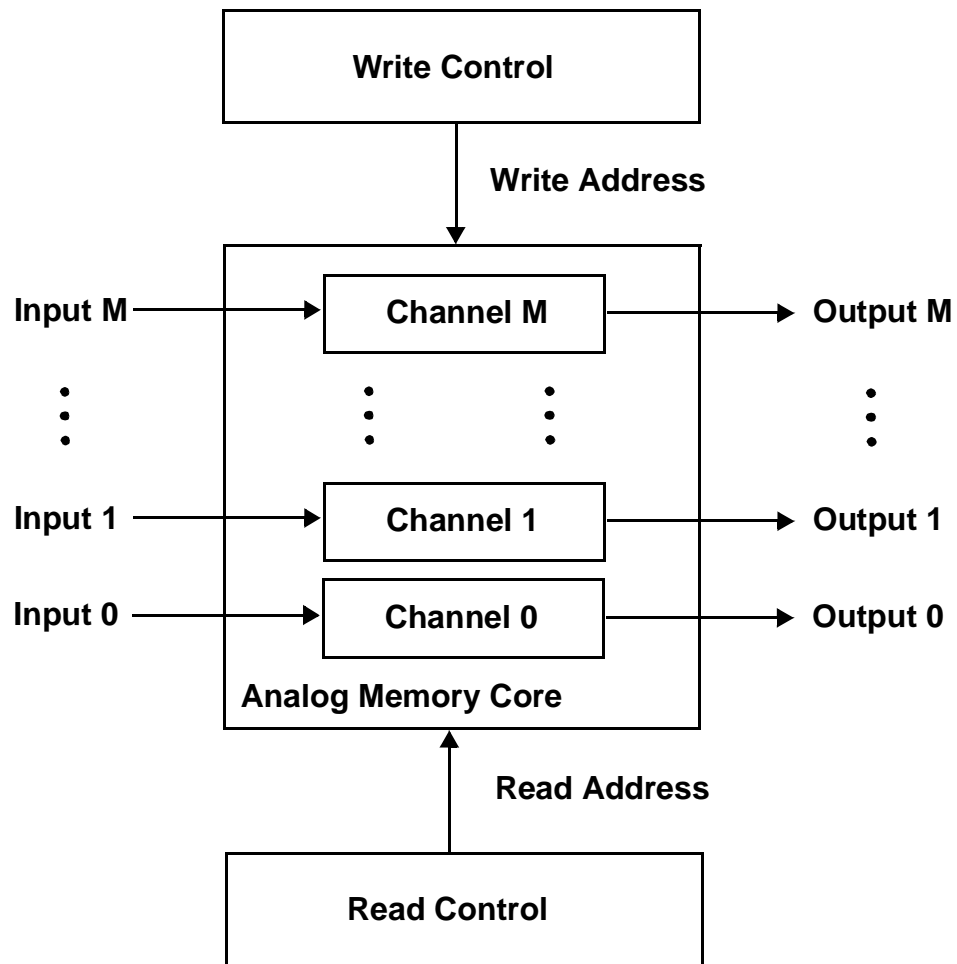


Figure 4.1: Analog memory block diagram.

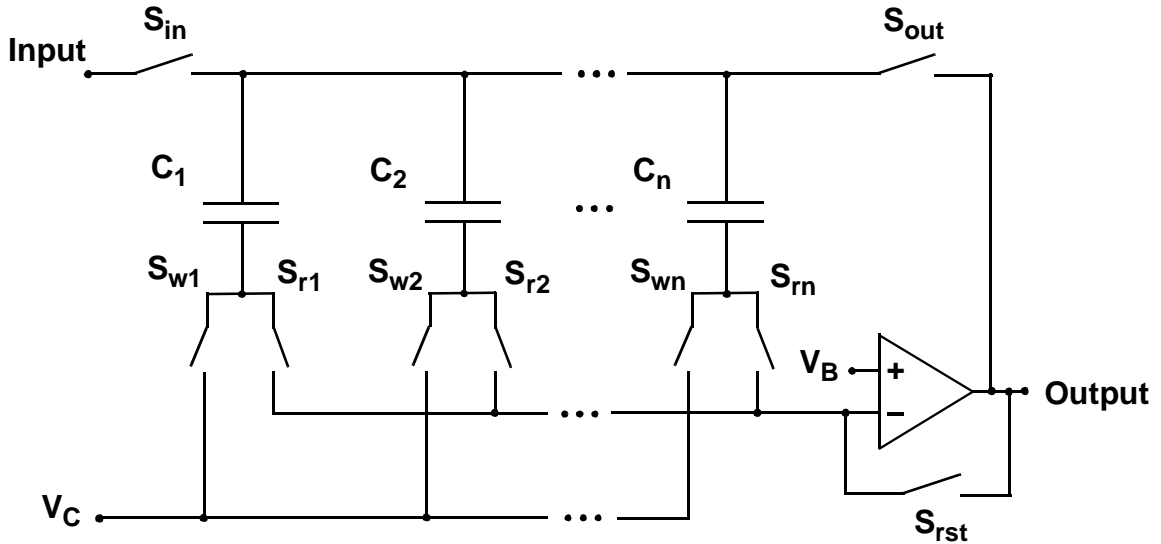


Figure 4.2: Bus-oriented architecture with one amplifier per channel. The sampling switches S_{wi} are inserted in the signal return path.

4.2 Analog Memory Core

4.2.1 Architecture

The proposed architecture of one channel of the analog memory core is shown in Figure 4.2. Voltages V_B and V_C are dc references. During the write phase, switches S_{in} and S_{rst} are closed, while S_{out} and read switches S_{r1} through S_{rn} are open. The input waveform is then sampled and stored on the capacitors by sequentially closing and opening write switches S_{w1} through S_{wn} . After the input waveform has been recorded, switch S_{in} is opened and S_{out} is closed. The stored analog waveform can then be read out by consecutively closing and opening read switches S_{r1} through S_{rn} .

The architecture of Figure 4.2 employs a bus-oriented voltage sensing scheme with a single readout amplifier to minimize power dissipation, area, and cell-to-cell response variations. Each memory cell incorporates separate write and read switches as opposed to

the configuration shown in Figure 2.7, which has one generic address switch for each cell and one common write and one common read switch per channel. The use of independent write and read address switches for each cell simplifies the write control circuit considerably, thereby enabling the design of circuits for very high-speed addressing. In order to circumvent limitations due to input-level dependent cell pedestals and sampling times, the write switches are inserted in the signal-return path in Figure 4.2, as suggested in Chapter 3. The input switch S_{in} is required so that the sampling capacitors can be disconnected from the signal input for readout. The capacitors are switched across the amplifier during readout in order to obtain a cell gain that is insensitive to the size of the sampling capacitor. The operation and theoretical performance of a circuit implementation of the architecture shown in Figure 4.2 are analyzed in the following sections.

4.2.2 Circuit Description and Operation

A simplified schematic of one channel of the proposed analog memory comprising N memory cells is shown in Figure 4.3. Each memory cell consists of a large write (sampling) transistor M_{wi} , a minimum-size read transistor M_{ri} , and a sampling capacitor C_i . The cells are addressed via write lines ϕ_{w1} through ϕ_{wN} and read lines ϕ_{r1} through ϕ_{rN} . The top plates of the capacitors are interconnected and can be shorted to the channel input or output by means of switches M_{in} and M_{out} . Voltage V_C is a dc reference common to the sources of all write transistors, M_{wi} . Switch M_{rst} serves to configure the operational amplifier as a voltage follower in order to force the nodes connected to the amplifier input and output to the dc bias level V_B during reset.

The operation of the circuit can be described by dividing the data acquisition process into write and read cycles. In the write phase, analog signals applied at the channel input, V_{in} , are sampled and stored in the memory cells of the circuit at a high rate. The stored analog information is subsequently read out serially at the channel output, V_o , at a lower speed.

During the write phase, switch M_{in} is turned on, connecting the signal V_{in} to the input bus, while switch M_{out} and the read switches M_{r1} through M_{rN} are all off, isolating the input bus from the read bus. Switch M_{rst} is on to keep the read bus at a defined potential,

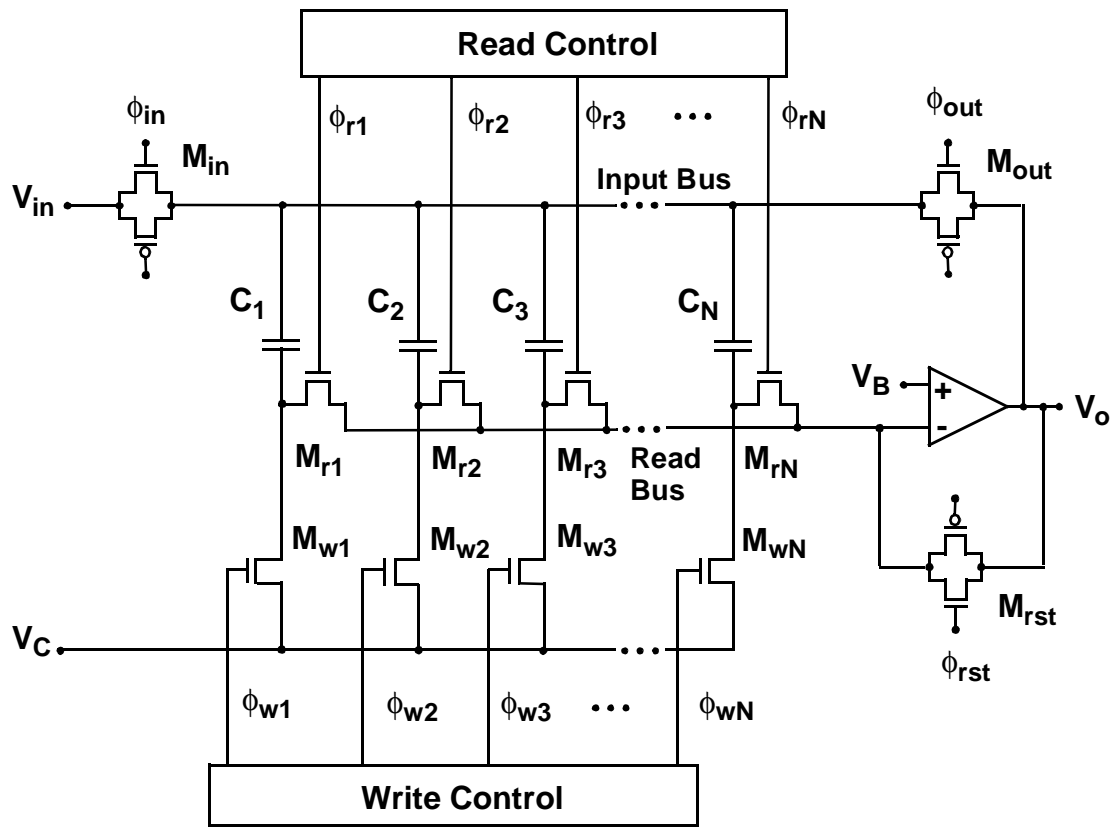


Figure 4.3: Simplified schematic of one signal channel.

V_B , during the entire write phase. An analog signal applied at the circuit's input is sampled onto the cell capacitors C_i by sequentially turning transistors M_{w1} through M_{wN} on and off as illustrated in Figure 4.4(a). Samples of the input waveform at N discrete times are thereby stored in the memory channel.

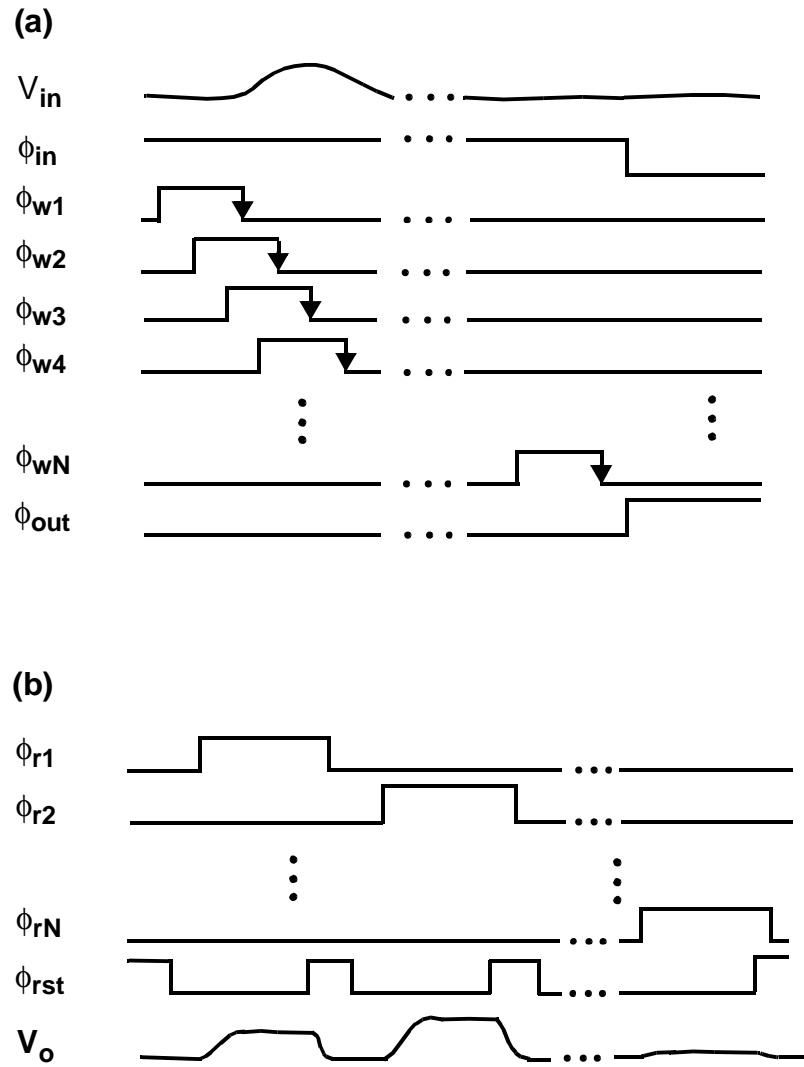


Figure 4.4: Timing diagram for (a) write and (b) read phase.

The voltage ΔV_{si} across capacitor C_i in memory cell i , $1 \leq i \leq N$, is

$$\Delta V_{si} = V_{in} - V_C - V_{pwi} , \quad (4.1)$$

where V_{pwi} is the pedestal voltage due to charge injection in switch M_{wi} after turn-off. As derived in Appendix A, with the source and drain terminals of the write transistor at reference voltage V_C at turn-off, the pedestal voltage V_{pwi} can be written as

$$\begin{aligned} V_{pwi} = & -\frac{\frac{C_{ox}W_{wi}L_{wi}}{2} + C_{wi}}{C_t} \sqrt{\frac{\pi UC_t}{2\beta}} \operatorname{erf}\left(\sqrt{\frac{\beta}{2UC_t}}(V_H - V_T - V_C)\right) \\ & - \frac{C_{wi}}{C_{pi} + C_i} (V_C + V_T - V_L) \end{aligned} \quad (4.2)$$

where C_{wi} is the write transistor gate overlap capacitance, C_i is the sampling capacitance, V_T is the threshold voltage, V_L and V_H are the low and high levels of the write-transistor gate voltage, C_{ox} is the oxide capacitance per unit area, W_{wi} and L_{wi} are the width and the length of the write transistor, $\beta = \mu_n C_{ox} W_{wi}/L_{wi}$, μ_n is the electron mobility in the channel, and U is the slew rate of the gate voltage. C_{pi} is the parasitic capacitance associated with the sampling capacitor terminal connected to the write switch M_{wi} and read switch M_{ri} ,

$$C_{pi} = C_{ss} + C_{wi} + C_{ri} + C_{wss} + C_{rss}, \quad (4.3)$$

where C_{ss} is the parasitic bottom plate capacitance of the sampling capacitor, C_{ri} is the gate overlap capacitance of the read transistor, and C_{wss} and C_{rss} are the source-to-substrate capacitances of the write and read switches. The capacitance C_t in (4.2) is

$$C_t = C_i + C_{pi} + \frac{C_{ox}W_{wi}L_{wi}}{2}. \quad (4.4)$$

It is apparent from (4.2) that the pedestal voltage V_{pwi} is independent of the input voltage V_{in} .

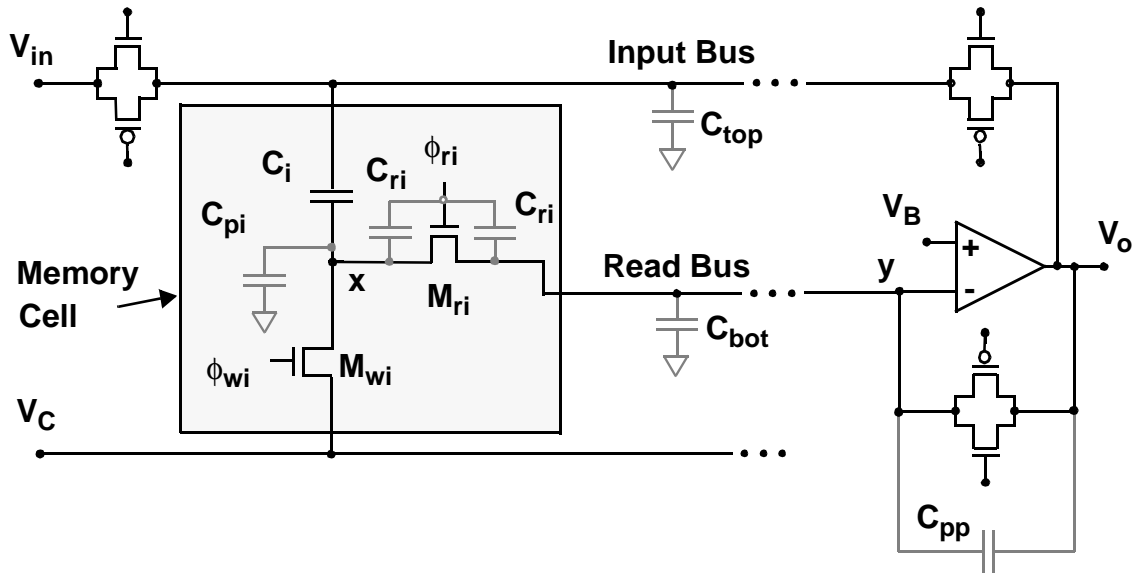


Figure 4.5: Analog memory with relevant parasitic capacitances.

After the write phase has been completed and the input waveform is stored in the analog memory, the read cycle is initiated. During readout, transfer gate M_{in} is turned off while M_{out} and M_{rst} are turned on, forcing both the input bus and the read bus to V_B . Transistor M_{rst} is then turned off and the voltage stored in the first cell is read out by turning transistor M_{r1} on, as illustrated in Figure 4.4(b). After the output has settled, the signal may be digitized with an external low-speed, low-power A/D converter. Following digitization, M_{rst} is again turned on and M_{r1} is turned off, which forces the input bus back to V_B in preparation for the readout of the next cell. This cycle is repeated for all cells. It is essential that the input bus always be forced back to V_B before a new cell is read out; otherwise, charge sharing and parasitic capacitances will seriously degrade the circuit's performance. By turning the cell read switches off after the reset switch is turned on, the potential across the capacitors is initialized to a defined (nominally 0 V) state for the next write phase. The minimum readout time is dependent on the number of cells to be read out and the performance of the amplifier.

4.2.3 DC Transfer Function

Once the write switch is turned off, the cell capacitor nodes connected to the cell transistors are left in a high-impedance state for the remainder of the write phase and the entire read phase. The charge at these nodes is thus conserved and, with the input and output busses forced to V_B in between readout of adjacent memory cells, only three parasitic capacitances influence the dc transfer function of a memory cell. One is the capacitance C_{pi} associated with the sampling capacitor terminal connected to the write switch M_{wi} , as illustrated in Figure 4.5 and described by (4.3). The second parasitic capacitance is the gate overlap capacitance of the read switch, C_{ri} , and the third parasitic capacitance to be considered is the capacitance, C_{pp} , between the input bus and the read bus. C_{pp} consists of the capacitance between the inverting input and the output of the amplifier, which is a fraction of the gate-drain capacitance of the amplifier input transistor (as explained in Chapter 5), together with capacitances associated with interconnections on the chip.

The transfer function of the memory can be derived using the schematics given in Figure 4.6 and Figure 4.7, which show a memory cell together with the readout amplifier before and after the cell is addressed for readout, respectively. In this analysis the only capacitances considered are those for which the potential changes from the write to the read phase. The total charge stored at memory cell node x in Figure 4.6 immediately after the write transistor M_{wi} is turned off is

$$Q_{xi} = (V_C + V_{pwi} - V_{in})C_i + (V_C + V_{pwi})C_{pi} + (V_C + V_{pwi} - V_L)C_{ri} \quad (4.5)$$

The charge is conserved at this node until the memory cell is addressed for readout. The charge Q_{yi} stored at the inverting input node of the amplifier, y , before the memory cell is addressed for readout is

$$Q_{yi} = (V_B - V_L)C_{ri} \quad (4.6)$$

because this node is reset to V_B before the cell is read out, as explained in Section 4.2.2.

After the read switch has been turned on by raising the gate signal ϕ_{ri} from V_L to V_H , node x and node y are shorted, and the memory cell is read out as illustrated in Figure 4.7.

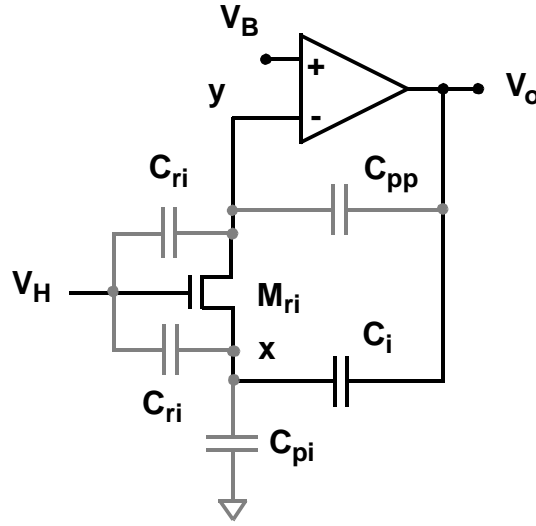


Figure 4.7: Circuit configuration when the memory cell is addressed for readout.

$$V_{rox} = V_H - V_{opm} - V_T. \quad (4.10)$$

By solving (4.5) to (4.8), the output of the amplifier when memory cell i is selected for readout can be described as a function of the input voltage, V_{in} , in the form

$$V_{oi} = A_i V_{in} + V_{offi}. \quad (4.11)$$

The gain factor A_i in (4.11) is

$$A_i = \frac{1}{1 + \frac{C_{pp}}{C_i} + \frac{1}{G} \left(1 + \frac{C_{pi} + C_{pp}}{C_i} \right)} \approx \frac{1}{1 + \frac{C_{pp}}{C_i}}. \quad (4.12)$$

The sampling capacitance C_i can be made large compared to C_{pp} , which, with careful circuit layout, will be dominated by the input-to-output capacitance of the amplifier. The open loop gain G of the amplifier can be made greater than 60 dB in practical CMOS circuits, so that A_i is close to one.

The offset voltage V_{offi} in (4.11) is given by

$$V_{offi} = V_B - A_i V_C + A_i \frac{C_{pi}}{C_i} (V_B - V_C) + A_i V_{poi} + V_{ch} . \quad (4.13)$$

V_{ch} is an offset voltage term common to all cells in one memory channel and includes both the charge injected at the turn-off of reset switch M_{rst} and the amplifier input offset voltage. The cell-specific parasitic offset voltage V_{poi} is

$$V_{poi} = \frac{2C_{ri}}{C_i} (V_L - V_H) - \frac{C_{ox} W_{ri} L_{ri}}{C_i} (V_H - V_B - V_T) - V_{pwi} \left(1 + \frac{C_{pi}}{C_i} \right) . \quad (4.14)$$

Because both A_i and V_{offi} are independent of the input voltage, V_{in} , it follows that the output voltage of the analog memory channel, V_o , is a linear function of V_{in} .

4.2.4 Memory Cell Response Variations and Calibration

In order to simplify the calibration and correction procedure, the uniformity of the sampling cell transfer characteristics must be considered. For applications where a high input bandwidth is required, the write transistor must be made large because the cell bandwidth, B , is determined by the size of the sampling capacitor and the resistance of the write transistor:

$$B \propto \frac{\mu_n C_{ox} \frac{W_{wi}}{L_{wi}} (V_H - V_C + V_T)}{C_i} . \quad (4.15)$$

In the circuit presented in Figure 4.3, memory cell response variations across a channel are governed by switch charge injection mismatch of the large write transistors. With the reference voltage V_C set to the bias voltage V_B , and W_w much larger than W_r (width of the read switch), the output voltage expressed in (4.11) is approximately

$$V_{oi} = V_{in} - V_{pwi} \left(1 + \frac{C_{pi}}{C_i} \right) . \quad (4.16)$$

In fast turn-off conditions the variation in channel charge dominates the charge injection mismatch, as explained in Section 3.6, and can be modeled as part of the mismatch of two geometric parameters, the channel width and length. Smaller switches yield smaller pedestal mismatches but limit the signal bandwidth of the sampling cell. The size of the write transistor is thus a trade-off between input bandwidth and pedestal mismatch for a given sampling capacitor value, which in turn is chosen on the basis of thermal noise considerations and the need to make relevant parasitics negligible.

A single NMOS transistor is used as a write switch to avoid the need for complementary control signals, which impose a burden on high speed designs. Complementary cell switches would reduce the overall cell pedestal sizes, but would not improve and might even worsen the cell pedestal uniformity across a channel, as described in Section 3.6. Since the pedestals can be accurately determined and then subtracted from the output by either analog or digital methods, their mean value is not of great concern. The pedestals are measured by applying a dc reference level at the channel input, recording the responses of the cells, and then subtracting the results during readout. In this context it is important that the charge injected by transistors M_{w1} through M_{wn} be independent of the signal level, which is not the case in other published analog memory architectures ([6], [9], [12] - [17]). Note that in the analyses presented in some of these references the error voltages from the sampling switches are neglected, which is not a valid assumption for a high input bandwidth analog memory.

During calibration, a reference voltage V_{cal} is applied to the input and the output voltage V_{oci} of cell i is recorded,

$$V_{oci} = A_i V_{cal} + V_{offi}. \quad (4.17)$$

During data acquisition, the circuit response to the applied input signal V_{sig} is

$$V_{oi} = A_i V_{sig} + V_{offi}. \quad (4.18)$$

The input signal V_{sig} can then be determined by subtracting V_{oci} from V_{oi}

$$V_{sig} = \frac{1}{A_i} (V_{oi} - V_{oci}) + V_{cal}. \quad (4.19)$$

Memory cell specific offset, as well as channel offsets, can thus be eliminated.

The influence of the size of the sampling cell capacitance on the memory cell gain A_i can be derived from (4.12), and the gain variation across a channel as a function of capacitor mismatch is

$$\frac{\delta A}{A_i} = \frac{C_{pp}}{C_i + C_{pp}} \left(\frac{\delta C_i}{C_i} \right). \quad (4.20)$$

In order to estimate the order of magnitude of the gain variation expected from capacitor size mismatch, the following practical values were assumed: $C_i = 500 \text{ fF}$, $C_{pp} = 2 \text{ fF}$, and $\delta C_i/C_i = 0.5 \%$. The calculated gain variation is then 20×10^{-6} , which translates into a memory cell gain matching better than 15 bits. An essential feature of the circuit is that the gain is insensitive to the capacitance mismatch and thus uniform across a signal channel, as long as C_i is much larger than C_{pp} .

4.2.5 Signal Range

Since the cell capacitor nodes connected to the cell transistors remain floating after the write switch is turned off, care must be taken to ensure that no significant leakage occurs at those nodes, for all possible ac and dc input signals, during the entire write and read phases. To avoid subthreshold leakage, the maximum input voltage swing, ΔV_{in} , in the write phase is limited. The waveforms in Figure 4.8 can be used to illustrate this constraint. Figure 4.8(a) is a triangular input waveform with a voltage swing of $\Delta V_{in} = V_{in2} - V_{in1}$. Shown in Figure 4.8(b) are the waveforms at node x in Figure 4.5 with the write switch turned off at times t_1 and t_2 , respectively. The cell transistors enter the subthreshold region when the voltage V_x falls below the low level of the gate voltage V_L . In addition, V_x must not fall below the switch substrate potential. To avoid subthreshold leakage, the maximum input voltage swing ΔV_{in} in the write phase is thus

$$\Delta V_{in} \leq V_C - V_L. \quad (4.21)$$

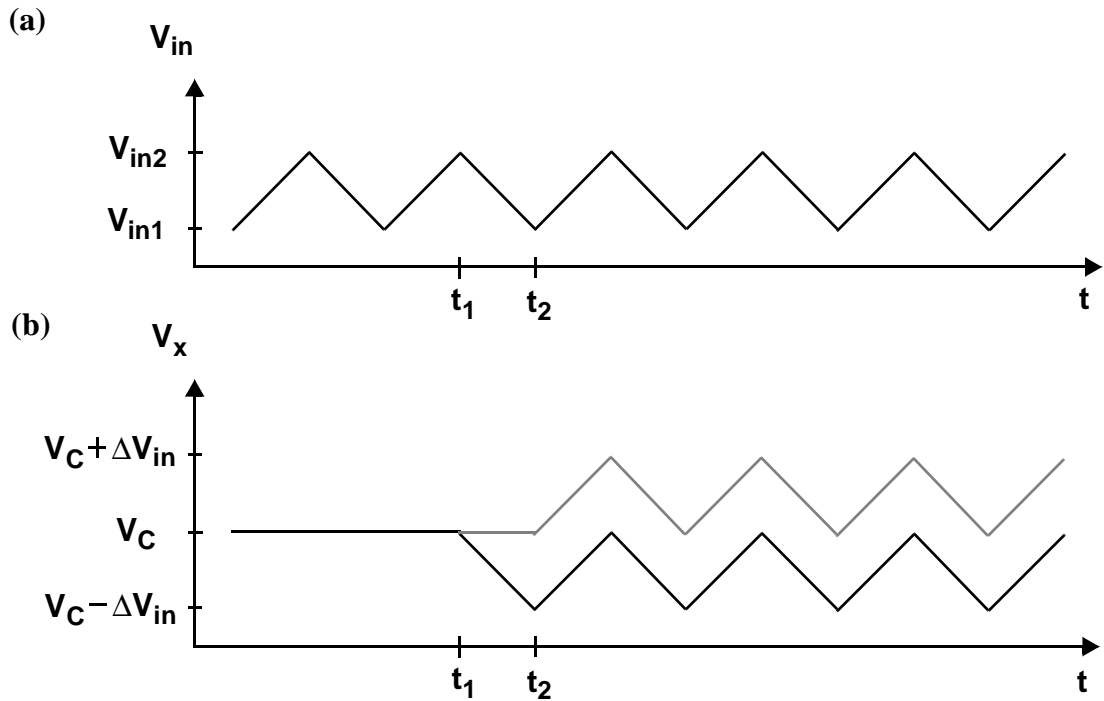


Figure 4.8: (a) Triangular input waveform (b) Waveforms at node x in Figure 4.5 with the write switch turned off at time t_1 (solid line) and t_2 (dashed line).

It is apparent that the maximum voltage swing is limited by the value of the reference input voltage V_C , which must be chosen so that the sampling switch resistances are small enough to achieve the desired bandwidth, as given by (4.15). It should be noted that the use of CMOS transmission gates as write switches would remove this bandwidth constraint on the maximum value of V_C , but the voltage swing would then be limited to $\Delta V_{in} \leq 0.5(V_H - V_L)$ so as to keep both types of transistors from entering the subthreshold region. The use of NMOS switches thus provides the additional benefit that the voltage V_x may exceed the high level control voltage V_H (when $\Delta V_{in} > V_H - V_C$).

In the read phase, the maximum voltage swing, ΔV_{oi} , at the output of the amplifier must be less than $(V_B - V_L)$ so as to avoid subthreshold leakage. It follows from (4.11) that the corresponding limit for the input voltage swing during the write phase is

$$\Delta V_{in} = \frac{\Delta V_{oi}}{A_i} \leq \frac{V_B - V_L}{A_i}. \quad (4.22)$$

The bias level V_B is therefore set to avoid leakage during the read phase and to ensure that V_o does not exceed the amplifier output voltage range.

Finally, it should be noted that in the design presented herein, the turn-off time of the sampling switches is independent of the signal level, thus eliminating a timing error that would otherwise be present for high frequency input signals. The input switch M_{in} in the proposed design is a CMOS transmission gate so as not to restrict the input voltage signal range.

4.2.6 Noise

The output voltage of the analog memory circuit is contaminated by noise originating from a variety of sources. The main sources of noise are thermal and flicker noise generated in the switches and in the operational amplifiers, and noise coupled directly or capacitively through the power, ground, and clock lines, and through the substrate. The circuit must be carefully laid out so that coupling between the control and signal traces is minimized. The power supply lines have to be bypassed to ground sufficiently to attenuate potential noise sources. Noise injected from clock lines into circuit nodes and into the substrate may contribute to the pedestal voltage of a memory cell. However, this error voltage can be cancelled by a simple subtraction correction procedure provided that the effect is independent of the input signal voltage level.

Thermal noise introduced by the resistance of the sampling switch determines the minimum size of the sampling capacitor C_i . The thermal noise is given by [44]

$$\overline{v^2} = \frac{kT}{C_i}, \quad (4.23)$$

where k is the Boltzman constant (1.38×10^{-23} AVs/K) and T is the absolute temperature. As an example, a 500 fF capacitor yields an rms noise voltage of 0.1 mV at 300 K.

Noise introduced by the amplifier consists of the thermal and the flicker (or 1/f) noise. Generally, the amplifier is designed so that the noise from the input transistor is dominant; the input-referred noise power density can then be written as [48]

$$S_{op}(f) = \frac{v_{op}^2}{\Delta f} = 4kT \left(\frac{2}{3} \frac{1}{g_m} \right) + \frac{K_f}{C_{ox}WL} \frac{1}{(f)^a}, \quad (4.24)$$

where $g_m = \sqrt{2\mu C_{ox}I_{DS}(W/L)}$ is the transconductance of the input transistor. The process dependent parameters K_f and a are the flicker noise coefficient and exponent, respectively. A typical value for K_f is 3×10^{-24} V²F/Hz and a is close to unity [40].

The first term in (4.24) represents the thermal noise of the transistor due to the finite resistance of the channel. As an example, the thermal noise voltage generated in a PMOS transistor with $W/L = 100 \mu\text{m}/8 \mu\text{m}$ and a gate oxide of 400 Angstroms is $10 \text{ nV}/\sqrt{\text{Hz}}$ when operated at a drain current of $I_{DS} = 20 \mu\text{A}$. The second term in (4.24) represents the contribution from flicker noise, which arises from the charging and discharging of energy states at the Si/SiO₂ boundary in the channel. For the above transistor parameters the flicker noise at 100 kHz is $6 \text{ nV}/\sqrt{\text{Hz}}$.

In order to illustrate the noise performance of the proposed analog memory, the simplified circuits shown in Figure 4.9, which correspond to the write and read configuration, respectively, are considered. The capacitance C_{op} is the parasitic capacitance at the inverting amplifier input and is dominated by the gate capacitance of the amplifier input transistor. In the write phase the thermal noise voltage, kT/C_i , is sampled onto the cell capacitor when the write switch is turned off; at that time the reset switch across the amplifier is closed. In the read phase the capacitor C_i is switched across the amplifier, and the square of the total noise voltage is given by

$$\overline{v_n^2} = \frac{kT}{C_i} + \left(\frac{C_i + C_{op}}{C_i} \right)^2 \overline{v_{op}^2}. \quad (4.25)$$

To determine the input-referred noise $\overline{v_{op}^2}$ from the amplifier, the power density $S_{op}(f)$ in (4.24) must be multiplied by a noise transfer function and integrated over the unity-gain bandwidth of the amplifier. The noise transfer function takes into account the effect of the

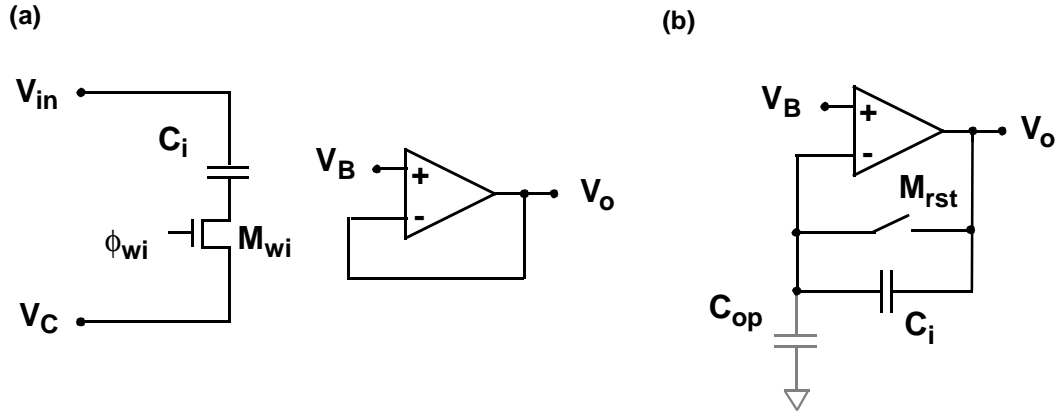


Figure 4.9: Circuit during the (a) write and (b) read phase.

sampling process in the read phase. Since the reset switch, M_{rst} , across the amplifier in Figure 4.9(b) is closed and opened before the memory cell is addressed for readout, the circuit forms a correlated double sampling (CDS) system [45, 46] that filters the amplifier noise. The noise transfer function of a CDS system is given by [47]

$$H(f) = 2 \sin\left(\frac{2\pi f T_s}{2}\right), \quad (4.26)$$

where T_s is the interval between the time the reset switch is opened until the time the output of the amplifier is sampled for digitization. The noise contributed from the amplifier in Figure 4.9(b) is then given by

$$\overline{v_{op}^2} = \int_0^{J_u} S_{op}(f) H^2(f) df. \quad (4.27)$$

4.2.7 Small-Signal Acquisition Bandwidth

The small-signal bandwidth of the analog memory circuit is governed by the impedances of the MOS switches, the size of the sampling capacitor, and by the size of associated parasitic capacitances. In Figure 4.10 the equivalent circuit of a memory cell is shown during

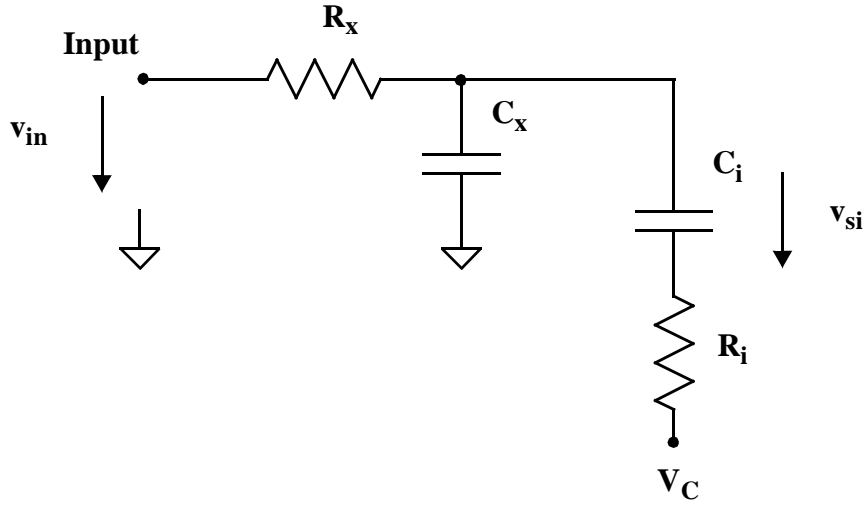


Figure 4.10: Circuit model with capacitors and resistors.

signal acquisition. Resistances R_x and R_i represent the input and write transistors, respectively. The capacitance C_x is given by

$$C_x = C_{in} + C_{top} + nC_i + (N - n)C_i', \quad (4.28)$$

where N is the number of memory cells in a channel, n is the number of memory cells that are simultaneously addressed, C_{in} is the drain capacitance of the input switch, C_{top} is the capacitance between the input bus and the substrate, C_i is the sampling capacitance, and C_i' is the parasitic series capacitance of a memory cell when the cell write switch is turned off. C_i' consists of the series combination of the sampling capacitance, C_i , and the parasitic capacitance C_{pi} as defined in (4.3).

As long as $R_x \ll R_i$, the frequency dependence of the voltage v_{si} across the sampling capacitor C_i can be approximated by

$$\frac{v_{si}}{v_{in}} = \frac{1}{\left(1 - \frac{s}{p_x}\right)\left(1 - \frac{s}{p_i}\right)} \quad (4.29)$$

with $p_x = -1/R_x C_x$ and $p_i = -1/R_i C_i$.

In general, the resistance of the input switch should be low enough so that the acquisition bandwidth of the analog memory is determined by the size of its cell components. The -3 dB frequency for the circuit is then given by

$$f_{-3dB} = \frac{P_i}{2\pi}. \quad (4.30)$$

In the proposed design a CMOS transmission gate is used as an input switch. The relative sizes of its PMOS and NMOS transistors should be chosen so that a switch resistance is obtained that is independent of the input voltage level V_{in} in order to avoid signal distortion.

4.2.8 Acquisition Time

The length of time that the sampling switches must remain in the sample mode is a function of the desired accuracy. The small-signal behavior of the analog memory can be approximated by a single pole expression provided that $|p_x|$ is much larger than $|p_i|$ in (4.29). The circuit response to a voltage step $v_{in}(s) = v_a/s$ at the input is

$$v_{si}(s) = v_a \left(\frac{1}{s} - \frac{1}{s - p_i} \right). \quad (4.31)$$

The time response to a step input is therefore

$$v_{si}(t) = v_a (1 - e^{p_i t}). \quad (4.32)$$

The relationship between the time t_α that the write switch must remain in the sample mode and the accuracy α in % is therefore

$$t_\alpha = -\tau \left(\ln \left(1 - \frac{\alpha}{100} \right) \right), \quad (4.33)$$

where $\tau = -1/p_i$ is the time constant of the memory cell.

4.2.9 Record Length

The record length, t_{rec} , of the acquired signal is defined to be the number of cells, N , in the channel divided by the sampling rate f_s ,

$$t_{rec} = \frac{N}{f_s}. \quad (4.34)$$

As an example, a signal channel with 256 memory cells operated at a sampling frequency of 200 MHz has a record length of 1.28 μ s. In low speed applications the number of cells in each channel, and thus the record length, is only restricted by the chip size, whereas for high-speed applications the maximum number of cells may be limited by the size of the input transistor needed to meet the bandwidth requirement, as explained in Section 4.2.7. For analog memories that require very long record lengths, as is the case for the input stages of analog sampling oscilloscopes, the single large common input switch can be replaced by smaller cell-specific input switches.

4.2.10 Leakage Current and Readout Speed

Leakage currents in the source and drain junctions of the NMOS write and read transistors are strong functions of temperature and double for every 8 $^{\circ}$ C rise in temperature [49]. A typical value for I_L is 15 fA/ μ m² at room temperature, which corresponds to a leakage current of 3 pA for a 50 μ m x 4 μ m source region. The rate of discharge for a 500 fF storage capacitor is then 6 μ V/ μ s. It should be noted that the effect of a constant leakage current manifests itself merely as a cell dependent offset voltage, which can be cancelled through a subtraction procedure.

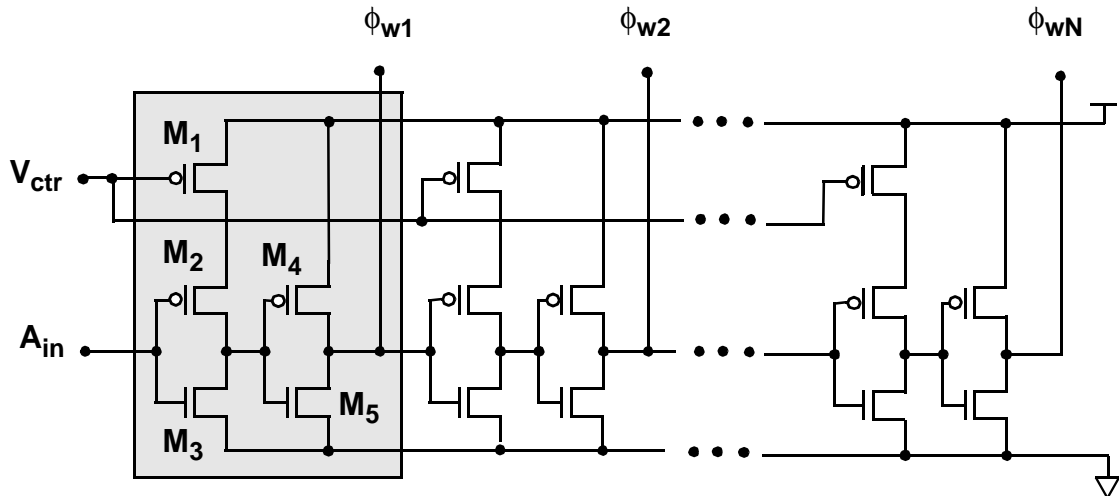


Figure 4.11: Inverter delay chain write control.

4.3 High Speed Write Addressing Circuit

4.3.1 Circuit Description

Traditionally, shift registers have been used for write address control in analog memory circuits. At sampling rates above 100 MHz this approach is difficult to implement, and in the proposed design a starved inverter delay chain, illustrated in Figure 4.11, is used instead. Such inverter chains have been employed previously in digital applications [50]. Each delay element in the chain consists of five MOS transistors, as indicated by the shaded box in Figure 4.11. A write pulse applied at input A_{in} propagates through the delay elements, thereby producing the write address signals ϕ_{w1} through ϕ_{wN} for the analog memory core. The delay of the write pulse through the chain is set by control voltage V_{ctr} which determines the on-resistance of PMOS transistor M_1 . This resistance together with the gate capacitance of the following inverter stage, M_4 and M_5 , provides an adjustable RC time delay that governs the sampling frequency of the memory.

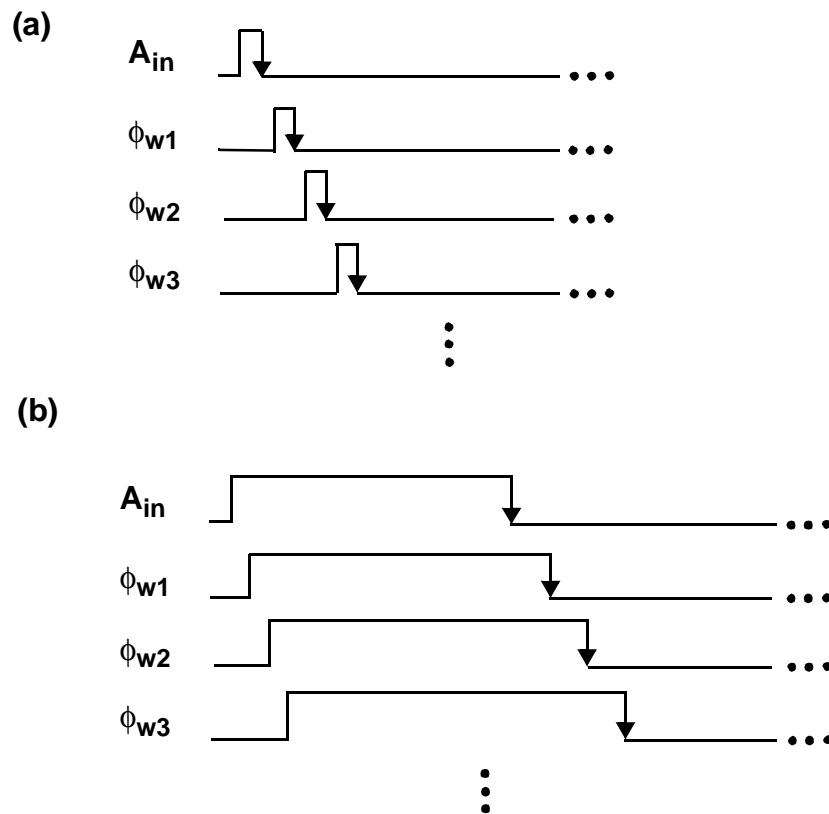


Figure 4.12: Write signals generated from a (a) short and (b) long input pulse A_{in} .

Shown in Figure 4.12 is a timing diagram for two different pulse widths applied to the control input A_{in} . For the short pulses in Figure 4.12(a), only a single memory cell is addressed at a time. The minimum width of the control pulse A_{in} (minimum acquisition time of the memory cell) is constrained by the accuracy with which the analog signal is to be acquired and the input time constant of the sampling cell. The acquisition time can be lengthened through an increase in the pulse width as shown in Figure 4.12(b), in which case the memory cells are preaddressed. In this mode several memory cells are addressed simultaneously and the additional capacitance at the input must be considered in the bandwidth calculations, as indicated in (4.28)-(4.33). Note that only the timing of the falling write clock edges is controlled by the circuit shown in Figure 4.11.

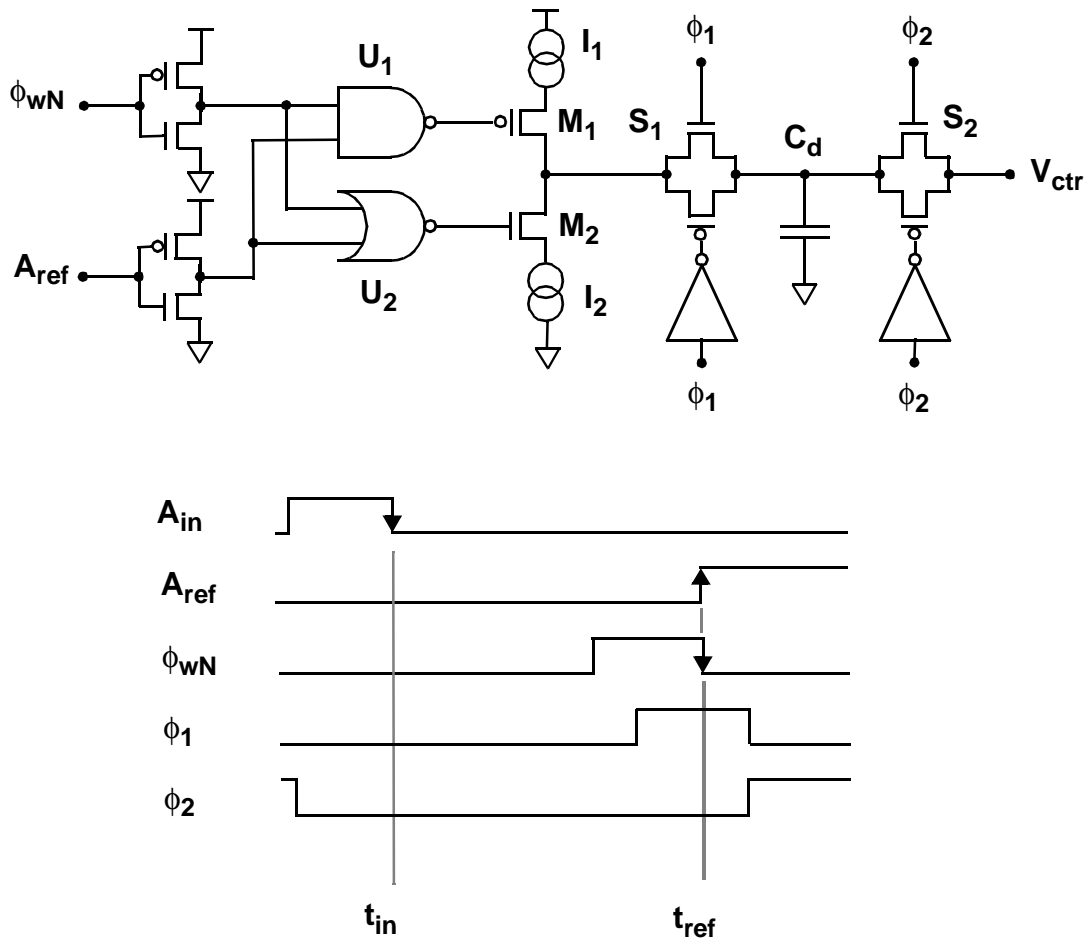


Figure 4.13: Servo feedback circuit with timing diagram.

In order to ensure an inverter chain delay, and thus sampling frequency, that is independent of variations in the fabrication process, the servo feedback circuit shown in Figure 4.13 is used. The leading edge of a reference input signal A_{ref} is compared to the trailing edge of the last write sample clock ϕ_{wN} . When the delay is less than the intended value, logic gate U_1 turns transistor M_1 on, which in turn connects current source I_1 to capacitor C_d . The voltage across C_d is increased, thereby slowing the inverter chain via the control voltage V_{ctr} . Likewise, V_{ctr} is reduced via current source I_2 should the inverter chain delay increase above the ideal value. The time difference $t_{ref} - t_{in}$ between signals A_{in} and A_{ref} thus determines the write sample frequency, $f_s = n / (t_{ref} - t_{in})$. This feed-

back circuit eliminates the sensitivity of the delay chain to process parameters and compensates for the effects of temperature and supply variations.

The speed with which V_{ctr} , and thus the sampling frequency, can be adjusted, is governed by the magnitude of currents I_1 and I_2 and the size of capacitor C_d , which is selected to avoid perturbations from the leakage currents of switches S_1 and S_2 between two acquisition cycles. The net leakage current is given by the sum of the currents flowing through the four reverse-biased source/drain pn-junctions of S_1 and S_2 in Figure 4.13. Switch S_1 is included so that the voltage across C_d is modified only while the delays are being compared during the write phase. Switch S_2 is added to ensure that V_{ctr} remains constant during the write phase. S_2 is turned on during the read phase in order to update V_{ctr} in preparation for the next write cycle. The start-up time of the circuit is determined by the sizes of I_1 , I_2 , and C_d .

This dynamic servo feedback delay circuit can be used only for synchronous repetitive signal acquisition. Otherwise, the discharge of C_d by leakage currents will introduce timing errors.

4.3.2 Timing Accuracy

The relative sampling time accuracy within a signal channel is affected mainly by delay variations among nominally identical inverter delay stages. The deviations from the nominal delay arise from inaccuracies in the fabrication process and are thus constant over time. The individual delay values can be determined experimentally by applying an ac waveform to the input of the signal channel and fitting the output response to an ideal curve with the element delays as variables.

The total delay of the inverter chain is regulated by the feedback control circuit. Inaccuracies in this circuit manifest themselves as variations of the control voltage level V_{ctr} , and thus in a variation in the delay of the entire inverter chain. As a consequence, the sampling frequency may vary from one measurement cycle to the next.

It should again be noted that in the proposed analog memory design the turn-off time of the sampling switches is independent of the input signal level, eliminating a timing error that would otherwise be present for high frequency input signals.

4.4 Read Addressing Circuit

The readout of the analog memory is controlled by an on-chip two-phase shift register together with the logic used to generate the read control signals ϕ_{r1} through ϕ_{rN} , as illustrated in Figure 4.14. The shift register is initialized by raising both read clocks ϕ_{s1} and ϕ_{s2} high while serial input ϕ_{rin} is low. The readout commences by setting ϕ_{rin} high for one clock period and shifting the voltage level at the serial input through the dynamic register by non-overlapping clocks ϕ_{s1} and ϕ_{s2} . The enable signal ϕ_{en} is used to disable the read addresses, ϕ_{r1} through ϕ_{rN} , while the analog memory is reset between readout of two successive memory cells, as shown in Figure 4.4(b).

4.5 Summary

In this chapter an analog memory circuit for use in high speed data acquisition systems has been introduced. Each channel in this memory consists of a bank of memory cells for storing samples of the input waveform and a single operational amplifier for reading out the stored samples. Each memory cell comprises a storage capacitor, a write switch, and a read switch.

The circuit's dc transfer function was derived, and it was shown analytically that the output voltage is a linear function of the input voltage with a gain term that is close to unity. It was also shown that the memory cell gain is insensitive to variations in cell component sizes. In order to achieve a high input bandwidth the write transistors must be made large, which unavoidably leads to substantial cell-to-cell response discrepancies. However, in the proposed architecture the cell specific pedestal voltages can be cancelled by means of a simple subtraction procedure since this pedestal voltage is not dependent on the input signal level, as is the case in many other waveform recording circuits. The pedestal voltage is governed by charge injection at turn-off of the large write switch and a theoretical expression for this voltage is derived in Appendix A. This analysis is valid even for circuits wherein the gate oxide and parasitic capacitances are not negligible in comparison with the sampling capacitance.

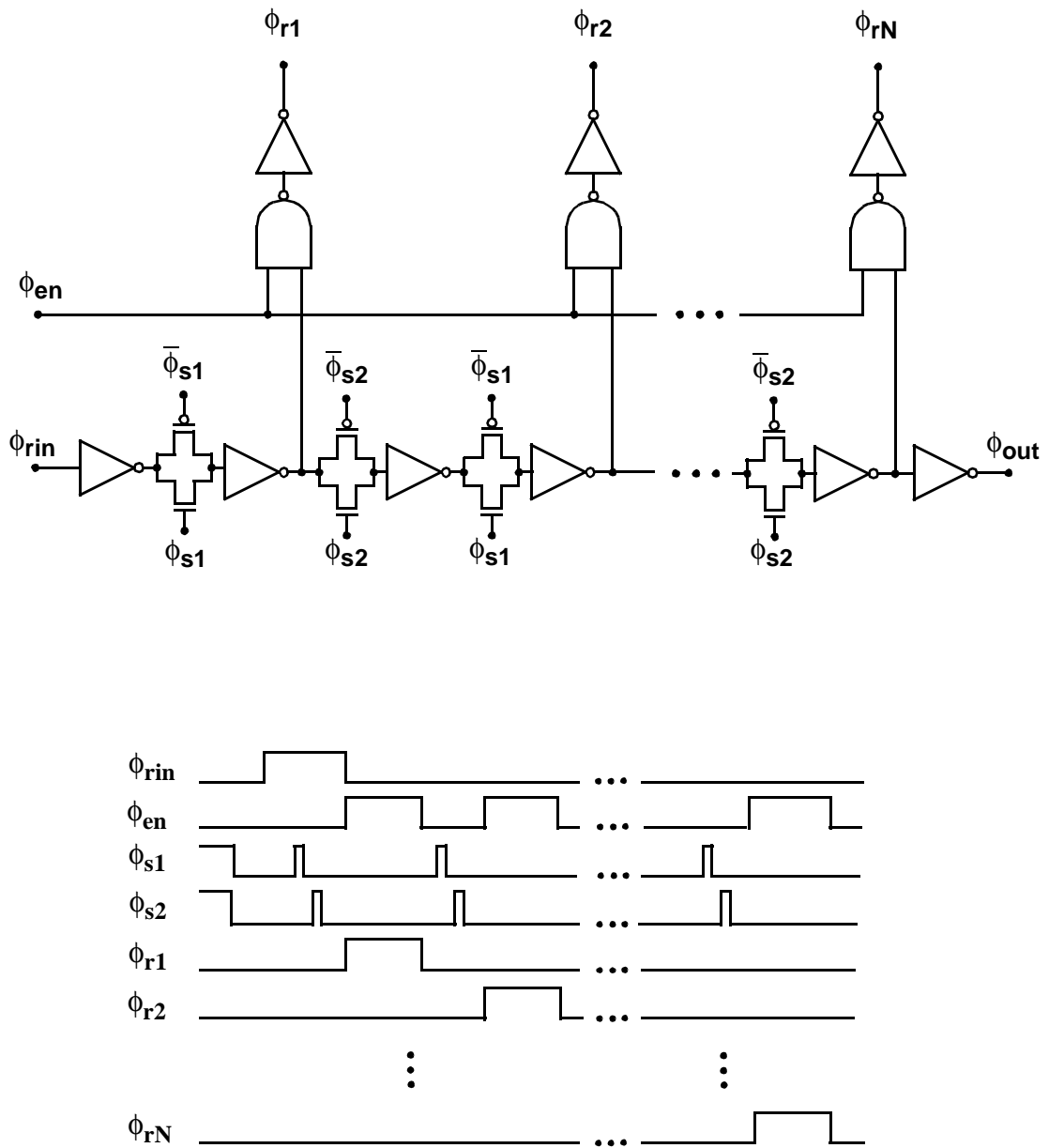


Figure 4.14: Read control circuit with timing diagram.

The main analog memory core has been designed so that the sampling time of the individual memory cells is independent of the input signal level. This removes the need for extensive ac calibration and sampling time error correction procedures that are otherwise required in high speed signal acquisition systems.

The high speed sampling clock required for the data sampling is typically derived from external clocks by means of shift registers. At high speeds, extensive ac calibration procedures are usually necessary to cancel cell-to-cell sampling period errors due to variations in gate delays between banks of interleaved shift registers or even within a shift register. In the proposed design an inverter delay chain is included instead and an external high-speed sampling clock is thus not needed. The performance of such an inverter delay chain is intrinsically sensitive to fabrication process variations, the operating temperature, and the power supply level. In the proposed circuit a dynamic servo feedback circuit has thus been included in the write control so as to establish a sampling frequency that is independent of these parameters. The sampling clock period is derived by a division of the time delay between two external control signal edges by the number of sampling cells within a channel.

In this chapter it was also shown that analog sampling circuits based on switched capacitor technology enable high speed sampling with a wide dynamic range since the resolution and baseline circuit noise is limited only by the kT/C noise of the sampling capacitor and the noise generated in the output amplifier.

Chapter 5

Folded Cascode Amplifier

5.1 Introduction

Each channel of the analog memory architecture presented in the previous chapter includes an on-chip operational amplifier that is used during the readout phase. The amplifier must provide sufficient gain, speed, and noise performance for the intended analog memory application. An open-loop gain of more than 60 dB and a readout settling time to 0.1% in several micro-seconds are the principle requirements for the present application. In addition, the noise contribution of the amplifier to the total circuit noise should be small compared to the kT/C noise sampled in the analog memory. The folded-cascode architecture lends itself to a simple realization of the stated goals and is attractive because the load capacitor provides the frequency compensation. Since the amplifier must drive an off-chip load of several picofarads, stable operation is assured. The folded-cascode topology is capable of achieving a higher stable closed-loop bandwidth with a large capacitive load than, for example, a two stage design. Also, its output voltage range is a good match to the limited input signal range of the analog memory, as alluded to in Section 4.2.5.

In Section 5.2 the folded-cascode architecture is examined with respect to gain, bandwidth, and flicker and thermal noise. A specific circuit implementation was simulated, fabricated, and tested. Measurement results characterizing its performance are presented

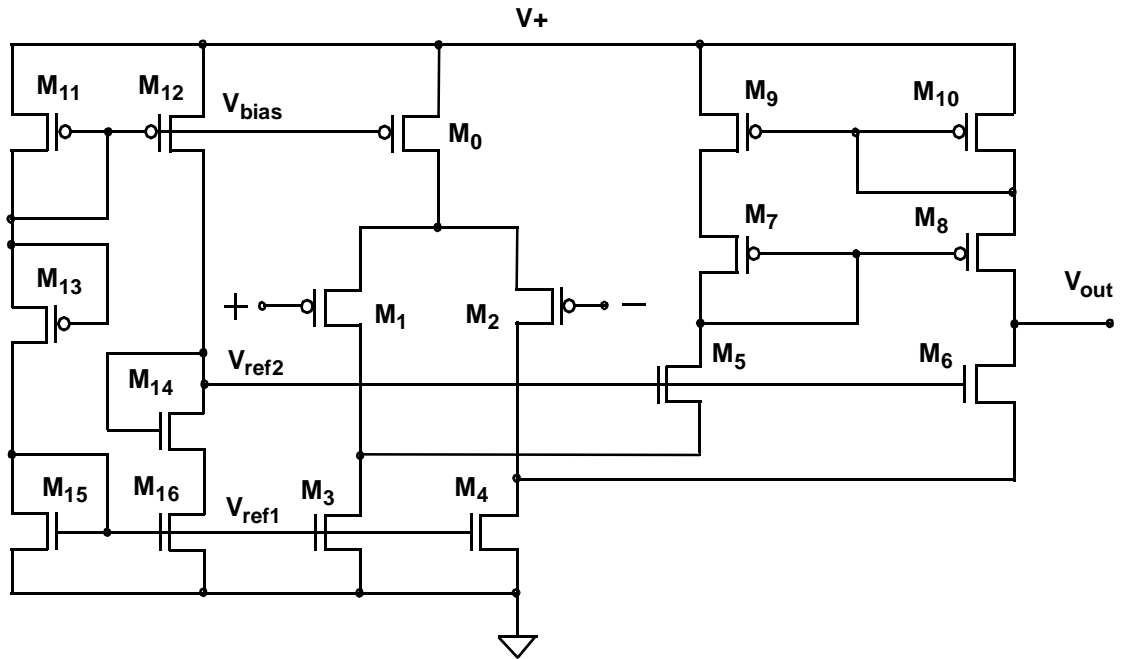


Figure 5.1: Schematic of the folded-cascode amplifier with bias generator.

in Section 5.3. The performance results were obtained with the amplifier in both follower and inverting amplifier configurations. The test setup is described in detail in Appendix B.

5.2 Output Amplifier Circuit

Figure 5.1 shows the schematic of a folded-cascode amplifier with a p-channel differential input pair. The circuit comprises a cascade of a common-source and a common gate stage and uses a current folding circuit technique to permit direct connection of the drains of the p-channel differential pair to the sources of the cascode devices. Transistors M_3 and M_4 operate as current sources. The currents through M_3 and M_4 equal the sum of the currents from the differential pair, M_1 and M_2 , and from the cascode mirror formed by M_7 through M_{10} . The reference voltages required to bias the amplifier, V_{ref1} , V_{ref2} , and V_{bias} , are generated by the bias generator formed by transistors M_{11} - M_{16} in Figure 5.1.

The dc voltage gain G of the amplifier in Figure 5.1 is the product of the transconductance of the input transistor, g_{m1} , and the impedance at the output node, r_{out} ,

$$G = g_{m1}r_{out} \approx \frac{g_{m1}}{\frac{g_{o2} + g_{o4}}{g_{m6}r_{o6}} + \frac{g_{o10}}{g_{m8}r_{o8}}} . \quad (5.1)$$

The dominant pole p_1 of the circuit is determined by the impedance at the output node together with the output capacitance C_{out} ,

$$p_1 = \frac{1}{2\pi}(r_{out}C_{out}) , \quad (5.2)$$

where C_{out} consists of the load capacitance and the parasitic capacitance at the output node.

The input-referred noise generated in the folded-cascode amplifier is the sum of the statistically independent mean-square noise currents from the transistors M_1 through M_4 and M_9 and M_{10} . The noise generated in these devices is coupled to the amplifier output through the low-to-high impedance transformation of common-gate transistors M_5 , M_6 , M_7 , and M_8 . The noise currents generated in M_5 through M_8 are injected into the output node with a much smaller gain and hence can be neglected. With matched transistors in each of the pairs $M_1 - M_2$, $M_3 - M_4$, and $M_9 - M_{10}$, the input-referred flicker noise spectral density for the folded-cascode amplifier can be expressed as

$$\frac{\overline{v_f^2}}{\Delta f} = \frac{\sum i_f^2}{g_{m1}^2 \Delta f} = \frac{2}{C_{ox} g_{m1}^2} \frac{1}{f} \left(K_{fp} \left(\frac{g_{m1}^2}{W_1 L_1} + \frac{g_{m9}^2}{W_9 L_9} \right) + K_{fn} \left(\frac{g_{m3}^2}{W_3 L_3} \right) \right) . \quad (5.3)$$

With the transistors M_9 and M_{10} biased at the same current as the input devices, the currents through M_3 and M_4 are twice that current. If it is assumed that the gate oxide capacitance per unit area is the same for p-channel and n-channel devices, the spectral density of the flicker noise is then given by

$$\frac{\overline{v_f^2}}{\Delta f} = \frac{2K_{fp}}{C_{ox} W_1 L_1} \frac{1}{f} \left(1 + \left(\frac{L_1}{L_9} \right)^2 + \frac{2K_{fn} \mu_n}{K_{fp} \mu_p} \left(\frac{L_1}{L_3} \right)^2 \right) . \quad (5.4)$$

The factor $K_{fn}\mu_n$ is approximately five times $K_{fp}\mu_p$ for a typical CMOS process [40] and the common assumption that the total flicker noise can be approximated by the noise generated in the input devices is therefore only valid if L_3 is much larger than L_1 when p-channel input devices are used.

The density of the input-referred thermal noise power generated in the amplifier circuit can similarly be derived and is given by

$$\frac{\overline{v_{th}^2}}{\Delta f} = \frac{\sum i_{th}^2}{g_{m1}^2 \Delta f} = \frac{16}{3} kT \frac{1}{g_{m1}} \left(1 + \frac{g_{m3} + g_{m9}}{g_{m1}} \right). \quad (5.5)$$

If it is assumed that the gate oxide capacitance per unit area is the same for p-channel and n-channel devices, one obtains

$$\frac{\overline{v_{th}^2}}{\Delta f} = \frac{16}{3} kT \frac{1}{g_{m1}} \left(1 + \sqrt{2 \frac{\mu_n (W/L)_3}{\mu_p (W/L)_1}} + \sqrt{\frac{(W/L)_9}{(W/L)_1}} \right). \quad (5.6)$$

Note that the thermal noise contribution of transistor M_3 can only be neglected if $(W/L)_1$ is much larger than $(W/L)_3$.

5.3 Experimental Results

In order to investigate the performance of the folded-cascode amplifier, the circuit was simulated using PSPICE [38] and fabricated in the Stanford University 2- μm BiCMOS technology [51]. The drawn dimensions of the channel lengths and widths are listed in Table 5.1. The biasing network establishes a nominal current of 40 μA in M_0 , and the corresponding power dissipation of the amplifier and the biasing network from a +5 V supply is 400 μW each. The simulation results for the currents and reference voltages match the measured values, as illustrated in Table 5.2. The drains of transistors M_0 and M_9 through M_{12} were bonded to separate package pins so that the currents through these transistors could be measured individually.

Reference	W/L
M_0	100/18
M_1, M_2	100/8
M_3, M_4	100/16
M_5, M_6	100/8
M_7, M_8	100/8
M_9, M_{10}	100/16
M_{11}	100/18
M_{12}	15/10
M_{13}	10/22
M_{14}	200/8
M_{15}, M_{16}	100/16

Table 5.1: Drawn transistor dimensions of the circuit shown in Figure 5.1.

Variable	Simulation	Measurement
V_{bias}	3.64 V	3.51 V
V_{ref1}	1.05 V	0.98 V
V_{ref2}	1.82 V	1.84 V
I_{M0}	40 μA	46 μA
I_{M9}	20 μA	23 μA
I_{M10}	20 μA	23 μA
Power Dissipation	400 μW	460 μW

Table 5.2. Simulation and measurement results.

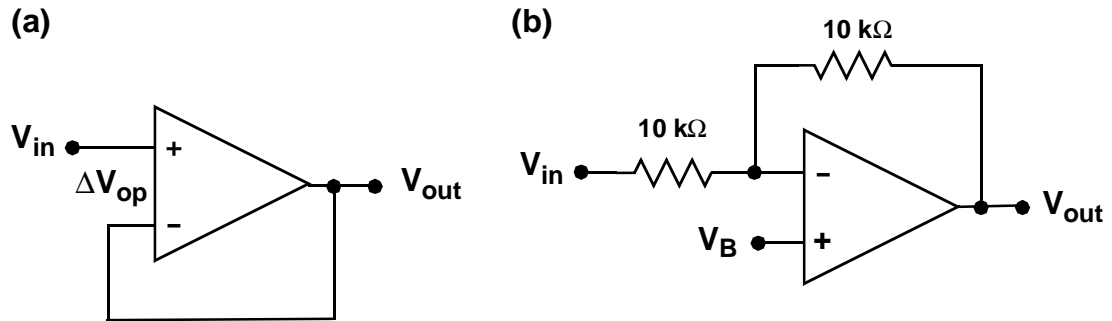


Figure 5.2: Amplifier in the (a) voltage follower and (b) inverter configuration. The circuits are shown simplified; see Appendix B for a complete test circuit description.

The amplifier was operated in two different configurations in order to measure performance parameters such as input offset voltage, linearity, and dc and ac open-loop gain. Simplified schematics of the amplifier connected as a voltage follower and as an inverter are shown in Figure 5.2(a) and (b), respectively. As indicated, the amplifier was evaluated in closed-loop, as opposed to open-loop configurations. Closed-loop measurements are much easier to accomplish because the closed-loop circuits are not sensitive to voltage drifts at the amplifier input. The complete test setups are described in Appendix B.

The input offset voltage and the follower (unity-gain buffer) voltage range of the amplifier were measured by recording the output voltage V_{out} as a function of input voltage V_{in} , with the amplifier in the follower configuration. In Figure 5.3 the difference between the output and the input voltages, $\Delta V_{op} = V_{out} - V_{in}$, of the follower is plotted for the follower as a function of the input voltage. The solid and the dashed curves represent the results obtained from measurements and simulations, respectively. The measured offset voltage is 5 mV. For the simulations it was assumed that the input transistors are identical (no mismatch), corresponding to a zero an offset voltage.

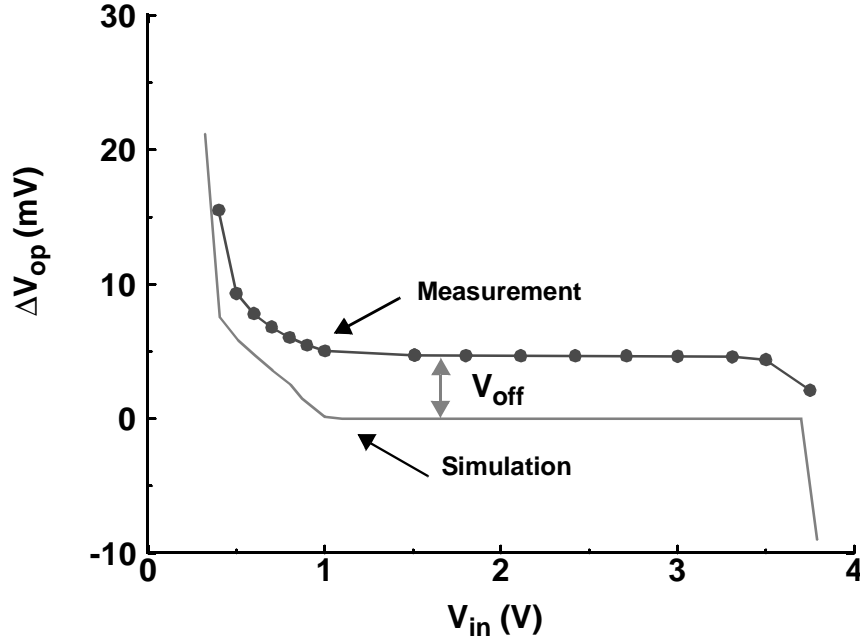


Figure 5.3: Output voltage minus input voltage, ΔV_{op} , as a function of the input voltage (measurement and simulation).

The output voltage of the follower circuit is given by

$$V_{out} = \frac{G}{1+G}(V_{in} + V_{off}), \quad (5.7)$$

where G is the open-loop gain and V_{off} is the input offset voltage of the amplifier. This equation can also be formulated as

$$\frac{\Delta V_{op}}{V_{out}} = V_{off} \left(\frac{1}{V_{out}} \right) - \frac{1}{G}. \quad (5.8)$$

In Figure 5.4 the ratio $\Delta V_{op}/V_{out}$ is plotted as a function of $1/V_{out}$ for an input voltage range from 1.2 V to 3.2 V. From (5.8) follows that the input offset voltage and the dc open-loop gain can be obtained from a linear fit to the data plotted in Figure 5.4. The slope of the fit is equal to V_{off} , and the extrapolated zero crossing ($1/V_{out} = 0$) determines the term $1/G$. The analytical fit to the measurement data yields an offset voltage of 4.8 mV and a dc

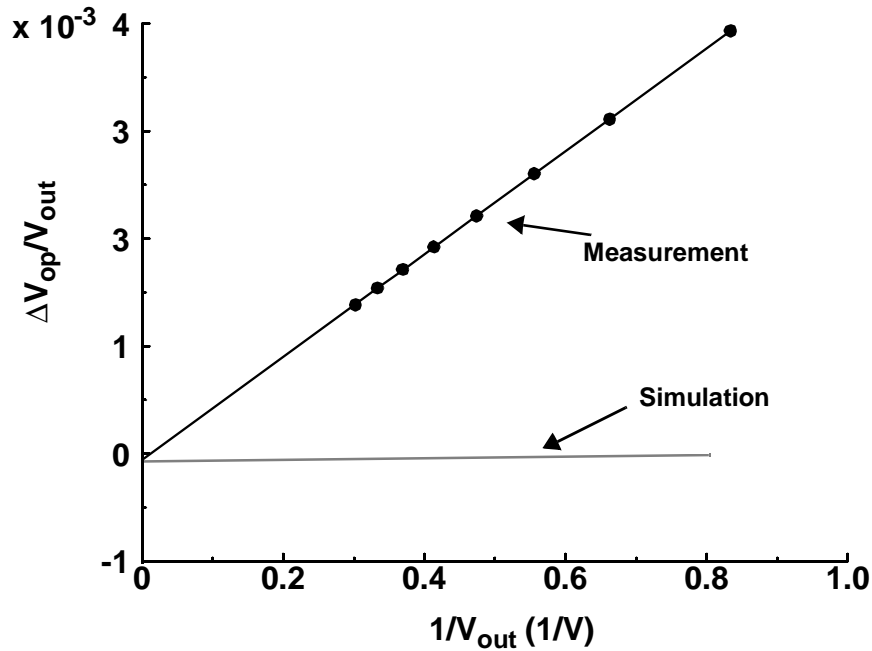


Figure 5.4: Plot for offset and gain determination. The slope corresponds to the offset voltage. The extrapolated zero crossing ($1/V_{out} = 0$) determines the term $1/G$.

open-loop gain of 83 dB. This compares to a nominal offset voltage of zero and a gain of 82 dB from the fit to the simulation output.

The amplifier output voltage range, its linearity, and the frequency dependence of its open-loop gain were measured with the amplifier in the inverter configuration, as depicted in Figure 5.2(b). In Figure 5.5 the input voltage, V_{in} , is plotted as a function of the output voltage V_{out} , together with the deviations from a linear fit across a 2.5 V output voltage range. The non-inverting input of the amplifier was set to $V_B = 2.45$ V. As indicated by the schematic of the test setup in Figure 5.2(b), the inverting input of the amplifier is forced to the reference level, V_B , at the noninverting input by the feedback action of the test circuit. The measured integral non-linearity is 0.03% over an output voltage range of 2.5 V.

In Figure 5.6 the open-loop gain and phase are plotted as a function of frequency. The solid and dashed lines correspond to the measurement and simulation results, respectively. For the simulations a 10 pF load capacitance was used, which approximately represents the output load capacitance in the test setup. This capacitance accounts for the amplifier

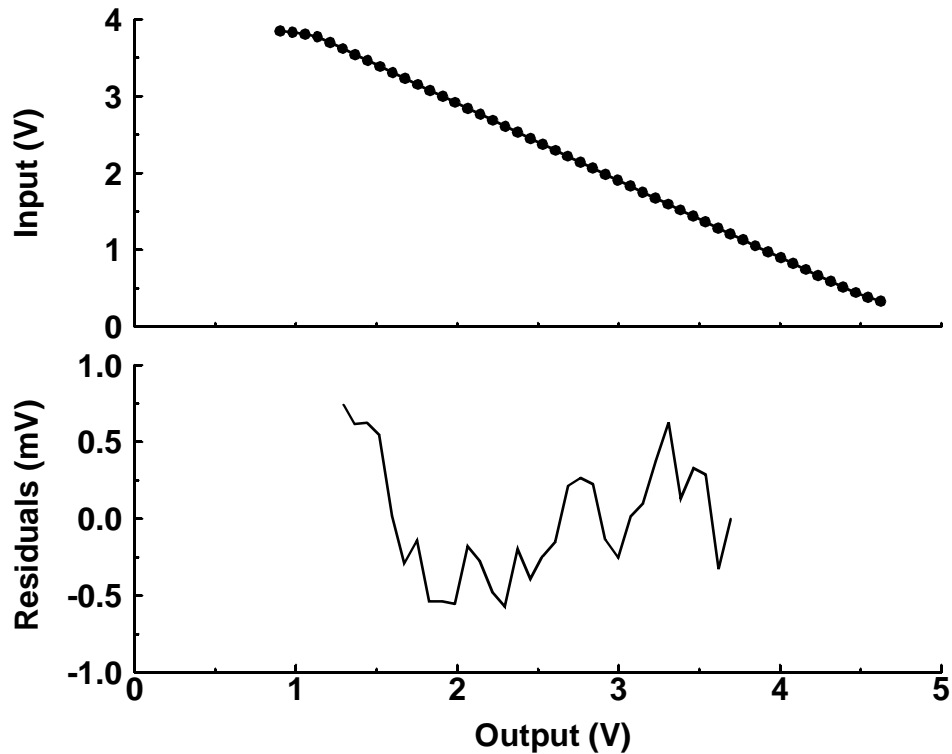


Figure 5.5: Upper: Input voltage V_{in} as a function of output voltage V_{out} . Lower: Residuals from a fit to a 2.5 V output voltage range.

package and socket (68 pin PLCC), traces on the pc board, and the input capacitance of the AD 843 amplifier (6 pF). The simulated and measured results are summarized in Table 5.3. The measurements and simulations agree well.

5.4 Summary

In this chapter the folded-cascode amplifier architecture has been examined and its gain, bandwidth, and noise performance have been characterized. One of the advantages of the folded-cascode amplifier is that its frequency response is dominated by the pole associated with its load capacitance; no internal compensation is needed to ensure stability. The amplifier is well-suited for use in the analog memory architecture introduced in Chapter 4.

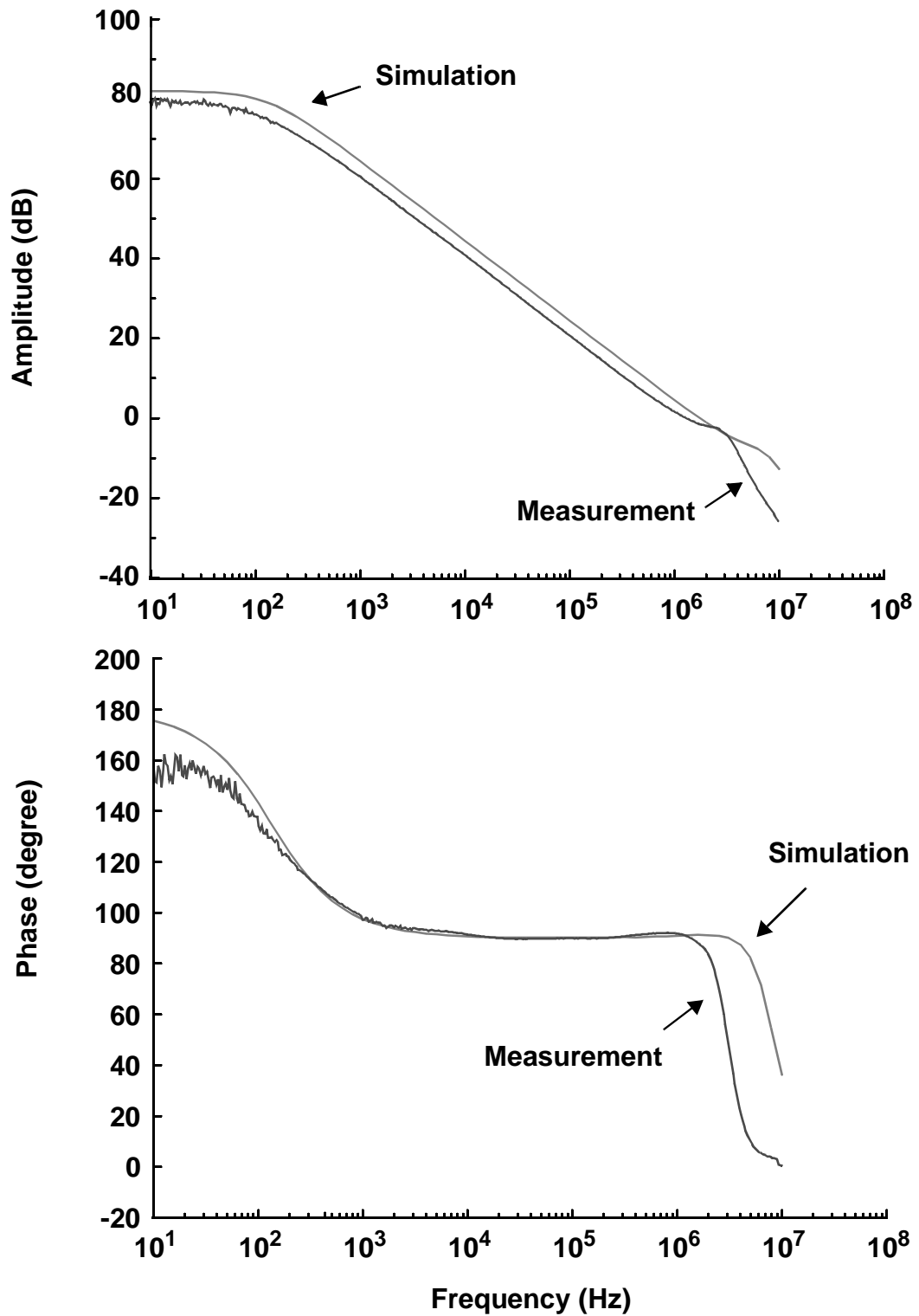


Figure 5.6: Amplitude (upper) and phase (lower) plotted as a function of frequency. (Starting frequency: 10 Hz).

Variable	Simulation	Measurement
Open-loop gain	82 dB	79 dB
-3dB bandwidth	125 Hz	100 Hz
Unity-gain bandwidth	1.8 MHz	1.6 MHz

Table 5.3. Simulation and measurement results ($C_L = 10$ pF).

It provides sufficient gain and bandwidth, and its output voltage range is a good match to that of the analog memory.

An experimental circuit was designed, simulated, and fabricated in a 2- μm BiCMOS technology at Stanford University. This amplifier operates from a single 5-V power supply with a power dissipation of 400 μW . The bias circuitry that generates the reference voltages for the amplifier was included on the chip. The amplifier characteristics were measured in both voltage follower and inverter configurations. The measurement setups are described in detail in Appendix B. The measured results agree well with simulations. The simulations predict an open-loop gain of 82 dB and a unity-gain bandwidth of 1.8 MHz with a 10 pF load capacitance. The experimental implementation was measured to have an open-loop gain of 79 dB and a unity-gain bandwidth of 1.6 MHz with a 10 pF equivalent load capacitance. The measured input offset voltage was 5 mV and the integral linearity was 0.03% for a 2.5 V output voltage range.

Chapter 6

A 2 x 32 Analog Memory Circuit

6.1 Introduction

An analog memory architecture for acquiring analog waveforms was proposed in Chapter 4. To demonstrate the operation and performance of such a memory, a complete two-channel experimental prototype with 32 memory cells in each channel has been designed and fabricated in a 2- μm CMOS technology with poly-poly capacitors [40]. Two versions of the circuit were realized; a low-speed version that employs a shift register to generate the write control signals and a high-speed circuit employing an inverter delay chain for write control. The overall chip architecture and the circuits for the analog storage and control blocks are described in Section 6.2. The test setup used to measure the performance of the experimental circuits is described in Appendix C, and the results from these measurements are reported in Section 6.3.

The sampling rate for the low-speed analog memory circuit was set to 13 MHz, while the high-speed circuit was operated at sampling rates as high as 700 MHz. The output responses of the two versions to dc inputs proved to be essentially identical. Thus, the dc results presented in this chapter for the high-speed memory are representative of both memory versions. It will be shown in this chapter that the high-speed experimental memory achieves a significant improvement in acquisition speed and dynamic range when

compared to other published waveform sampling circuits and to monolithic analog-to-digital converters.

6.2 Chip Architecture

A block diagram of the experimental high-speed analog memory is shown in Figure 6.1 (the low-speed circuit differs only in the write control circuitry). Two channels with 32 memory cells each were integrated in the experimental circuit. The analog input signals are V_{in1} and V_{in2} , while the analog outputs are V_{o1} and V_{o2} . The write address signals ϕ_{w1} through ϕ_{w32} are generated in the write address block from the external control signals A_{in} , A_{ref} , ϕ_1 , and ϕ_2 , as described in Chapter 4.3. The read address signals ϕ_{r1} through ϕ_{r32} are generated in the read control block. The write and read address lines are common to both memory channels.

Figure 6.2 is a photograph of the analog memory chip. The die measures 2.2 mm x 2.2 mm. The large input transistors are seen on the left, the banks of analog memory cells are in the middle, and the folded-cascode amplifiers appear on the right. The inverter delay chain write address circuitry is located above the analog memory channels, and the read control is located below those channels. The feedback delay control circuit is located in the upper right corner of the chip.

A schematic of one 32-cell analog memory channel is shown in Figure 6.3. The channel dimensions of the NMOS and PMOS transistors comprising the input switch are $W/L=1200\ \mu\text{m}/2\ \mu\text{m}$ and $W/L=2000\ \mu\text{m}/2\ \mu\text{m}$, respectively. As suggested in Chapter 3, the relative sizes of these devices were chosen so as to minimize the signal dependence of the switch on-resistance. The drawn dimensions of the read transistors, M_{ri} , are $W/L=3\ \mu\text{m}/2\ \mu\text{m}$ (minimum size). The area of a single memory cell is $40 \times 40\ \mu\text{m}^2$ and is dominated by the 500 fF capacitor and the sampling switch ($W/L=50\ \mu\text{m}/2\ \mu\text{m}$). The output amplifier is a folded-cascode design of the type described in the previous chapter.

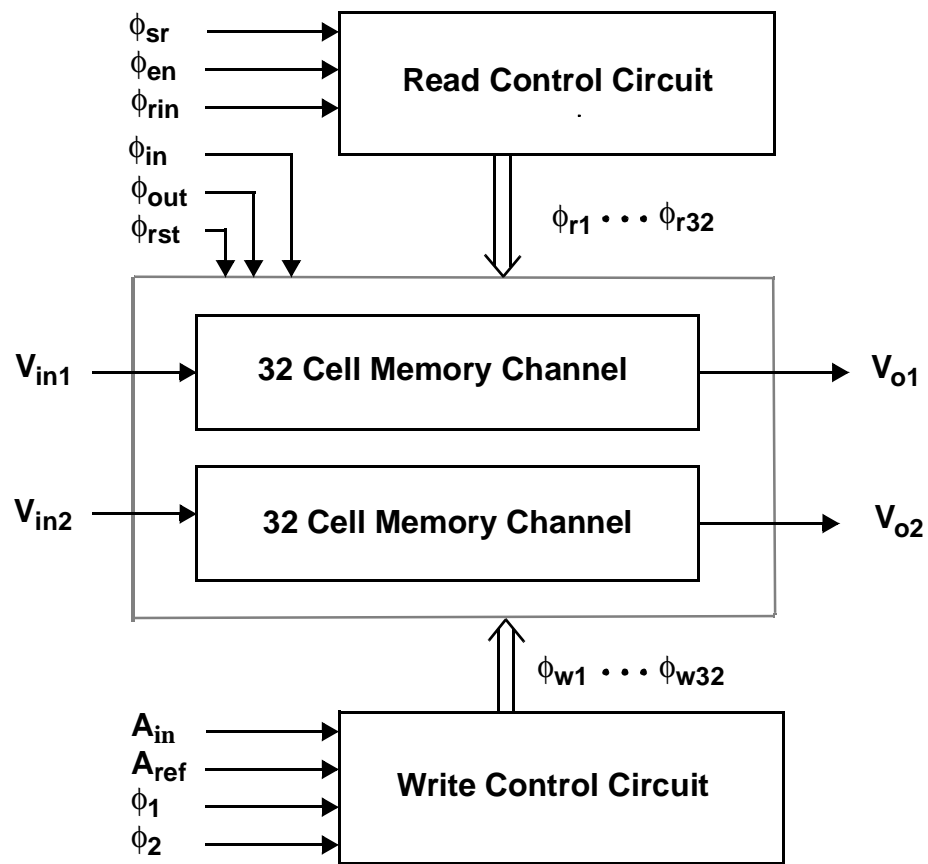
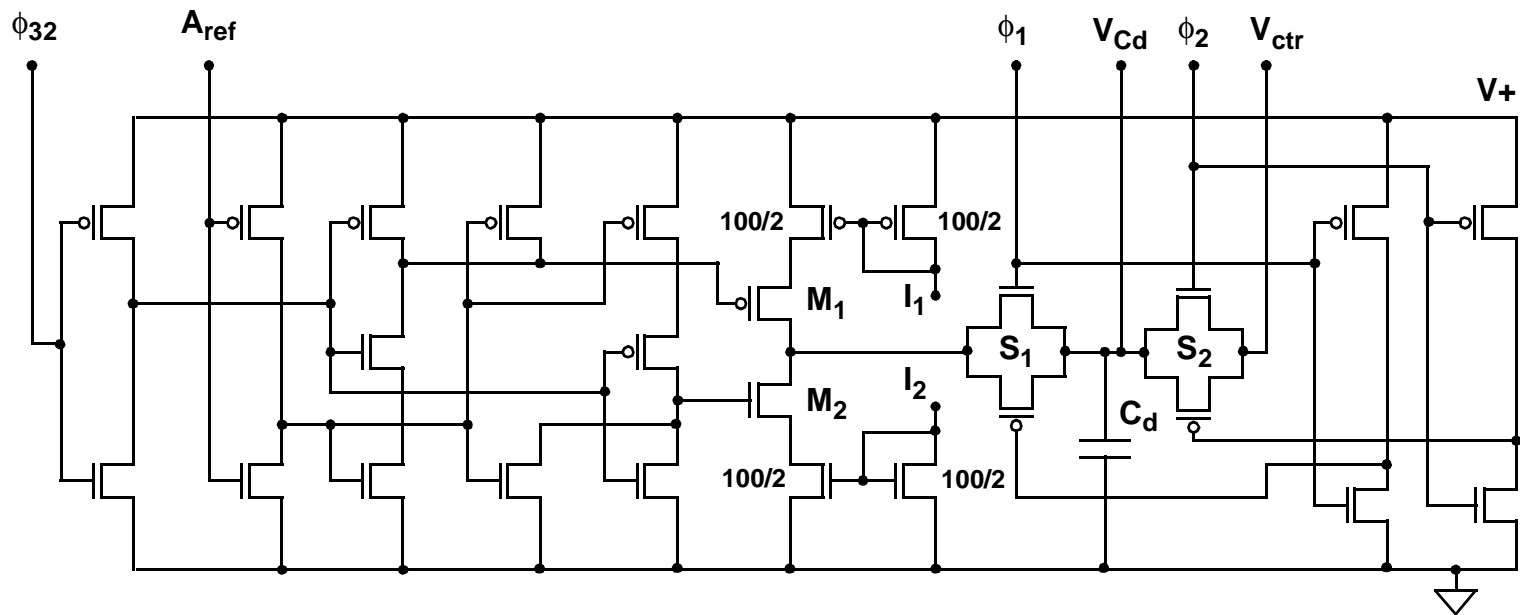


Figure 6.1: Block diagram of the two channel analog memory prototype.

Figure 6.2: Die photo.



$W/L = 3/2$ for NMOS and $W/L = 6/2$ for PMOS unless noted otherwise

Figure 6.4: Delay feedback circuit.

with which the control voltage V_{ctr} adjusts can be varied. The magnitude of the current is a trade-off between the number of cycles needed to reach the nominal sampling frequency at start-up and the delay jitter once the nominal frequency is established.

6.2.2 Read Control Circuit

A 32-stage dynamic two-phase shift register has been included on the chip to generate the read address signals ϕ_{r1} to ϕ_{r32} . The circuit is shown in Figure 4.14; the NMOS and PMOS transistor dimensions are $W/L = 3 \mu\text{m}/2 \mu\text{m}$ and $W/L = 6 \mu\text{m}/2 \mu\text{m}$, respectively. The two-phase clock is generated from an external single read clock, ϕ_{sr} , using a pair of cross-coupled NOR gates as depicted in the upper part of Figure 6.5. The nonoverlapping characteristic of the resulting shift-register clocks, ϕ_{s1} and ϕ_{s2} , is ensured by the delays of the extra inverters.

6.3 Experimental Results

The experimental test setup used to evaluate the performance of the experimental analog memory circuits is described in detail in Appendix C. The responses of the two different analog memory versions to dc input signals were virtually identical. The dc results presented in this chapter for the high-speed circuit are thus representative for the performance of both devices. The dc power dissipation for each 32-cell channel, when operated from a single 5-V supply, was measured to be 2 mW and was dominated by dissipation of the output amplifier, the bias generator, and the servo feedback circuit.

The response of one channel to a 2-V input voltage step with a 3-ns rise time is shown in Figure 6.6(a) and illustrates the operation of the high-speed memory with V_B and V_C set to 2.5 V. The output signal levels of the 32 memory cells are alternated with the amplifier reset level, V_B , as illustrated in the timing diagram in Figure 4.4(b). The delay feedback control signal, A_{ref} , was adjusted to establish a sampling rate of 700 MHz (1.42 ns between the turn-off of adjacent sampling transistors). The readout time for each cell was set at 11 μs , which is the conversion time of the 16-bit ADC used to digitize the output samples. In Figure 6.6(b) the output pulse is plotted as a function of input time, and the

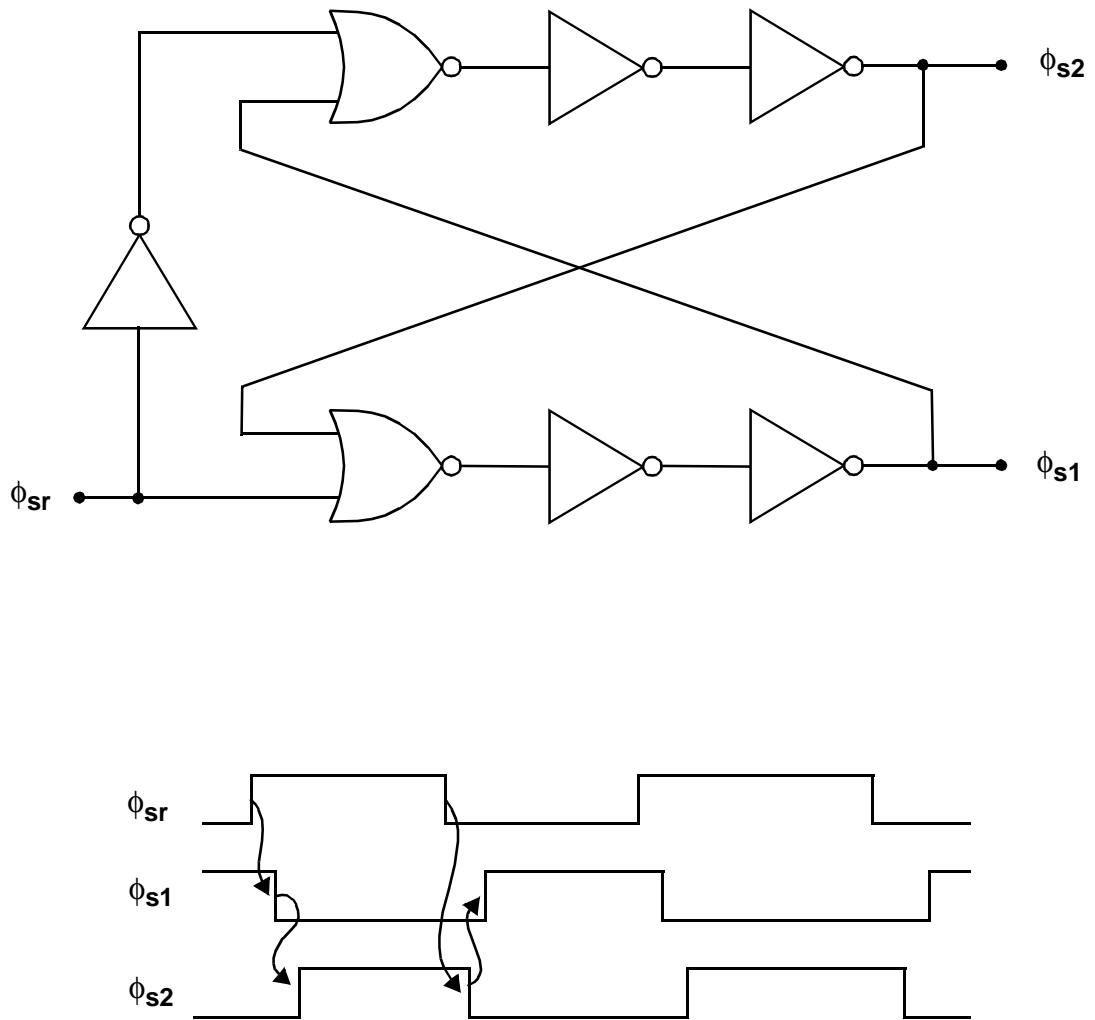


Figure 6.5: Two-phase clock generator with timing diagram.

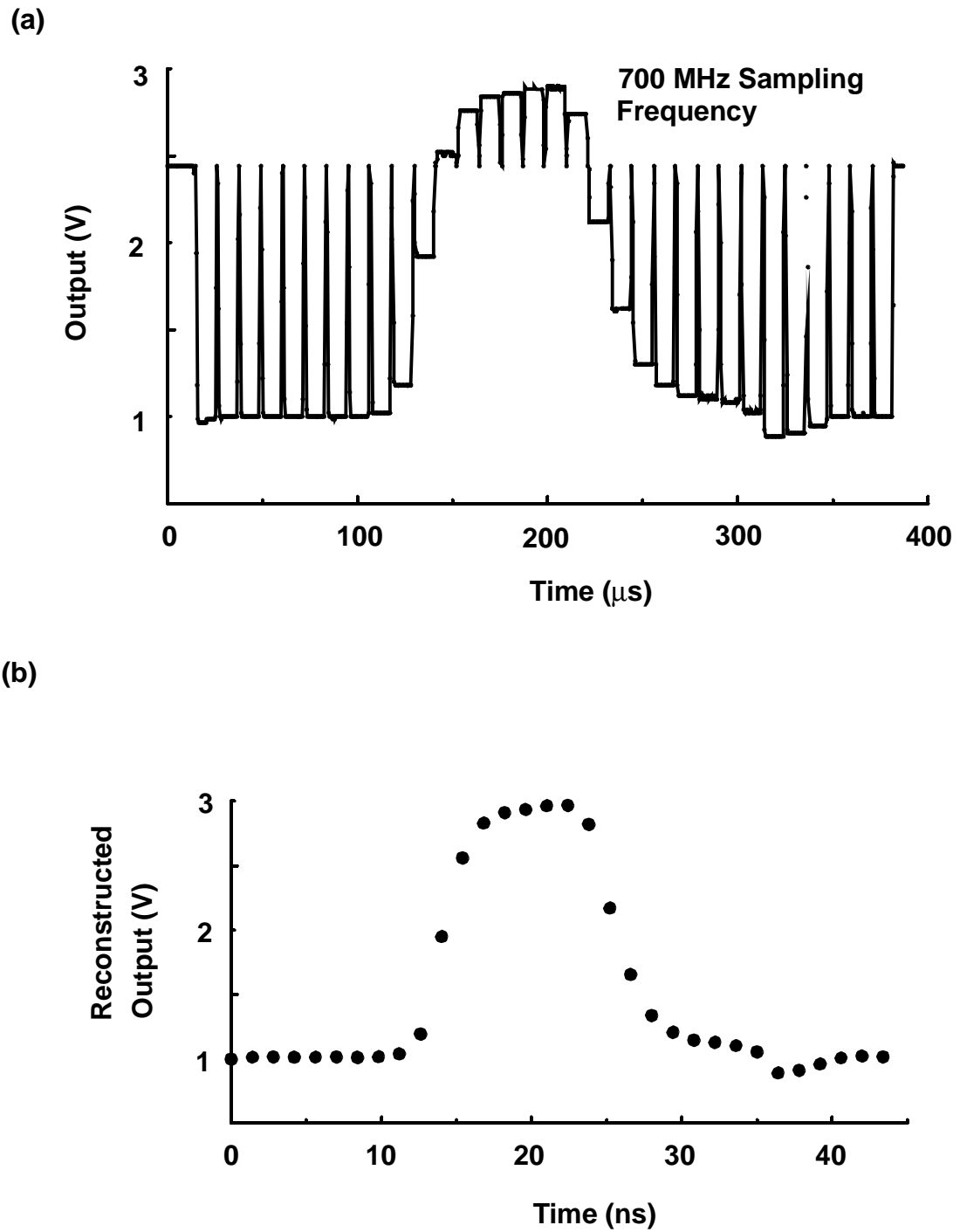


Figure 6.6: Pulse response plotted on a (a) read and (b) write time scale.

results agree with the input pulse, as monitored on an oscilloscope, with respect to rise and fall times, pulse width, and signal undershoot. The input time constant of the memory, defined as the product of the on-resistance of the cell write transistor and sampling capacitance C_i , was designed to be less than 0.5 ns for $V_C = 2.5$ V.

6.3.1 Noise and Dynamic Range

The dynamic range of an analog waveform storage circuit is commonly defined as the maximum recordable signal divided by the baseline noise, which governs the smallest detectable signal. The baseline noise of this analog memory was determined by recording the circuit response to repeated measurements with a constant input voltage level and calculating the mean square rms voltage error

$$\bar{v}_{rms} = \frac{\sqrt{\frac{1}{M-1} \sum (V_{oi} - V_{avg})^2}}{\sqrt{M-1}}, \quad (6.1)$$

where V_{avg} is the output voltage of memory cell i , averaged over M measurements. An rms error voltage of 0.3 mV was obtained from sets of 100 repeated measurements, independent of the input signal level. The dynamic range of the circuit is therefore better than 8,000/1, or 13 bits, for a 2.5 V input voltage range.

In order to compare the measured baseline noise with the theoretical noise value, the contributions from the individual circuit blocks are estimated for the 2- μ m CMOS process in which the memory was integrated [40]. The flicker noise coefficients provided by the manufacturer, $K_{fn} = 4 \times 10^{-24}$ and $K_{fp} = 2 \times 10^{-24}$, were used for the noise estimates. The simulated open-loop gain of the amplifier used in the analog memory is 74 dB, and its unity-gain frequency is 800 kHz in the test board environment ($C_L = 3$ pF, see Appendix C). As explained in Section 4.2.6, the square of the total input-referred noise voltage for the analog memory can be expressed as

$$\bar{v}_n^2 = \frac{kT}{C_i} + \left(\frac{C_i + C_{op}}{C_i} \right)^2 \bar{v}_{op}^2, \quad (6.2)$$

where C_{op} is the capacitance at the inverting input node of the amplifier during readout, and v_{op} is the input-referred noise voltage of the amplifier. At a temperature of 300 K, the noise sampled onto the 500 fF sampling capacitor during the write phase is $\sqrt{kT/C} = 90\mu\text{V}$. In Section 4.2.6 it was shown that in order to obtain the amplifier noise voltage, v_{op} , the amplifier noise power density is integrated over the unity-gain bandwidth of 800 kHz, as expressed in (4.27). The time interval T_s in (4.26) was 2.5 μs . T_s was the interval from the time the reset switch was turned-off until the time the cell was addressed for readout, the amplifier output had settled, and the output voltage was sampled for digitization. For the implemented amplifier circuit, the total noise could not be approximated by the noise generated in its input transistors. In Table 6.1 the squares of the individual thermal and flicker noise contributions of the individual transistors of the amplifier are listed. The notation used in Table 6.1 corresponds to Figure 5.1.

Transistors	W/L [$\mu\text{m}/\mu\text{m}$]	Thermal [μV^2]	Flicker [μV^2]
M_1	100/8	138	437
M_2	100/8	138	437
M_3	100/16	194	512
M_4	100/16	194	512
M_9	100/16	95	73
M_{10}	100/16	95	73

Table 6.1: Noise contribution from the individual amplifier transistors.

As analyzed in Chapter 5.2, the square of the total input-referred noise voltage of the amplifier, v_{op}^2 , is the sum of the squares of the individual input-referred transistor noise voltages. With a value for C_{op} that is approximately 2.5 times the sampling capacitance, C_i , the total circuit noise in the system, expressed by (6.2), is theoretically

$$v_n = \sqrt{(8100\mu\text{V}^2) + (3.5)^2(2898\mu\text{V}^2)} = 209\mu\text{V} . \quad (6.3)$$

This value compares to a measured noise of 300 μV .

To investigate whether the measured noise is limited by the amplifier, various capacitances were added to the output of the amplifier so as to change its closed-loop bandwidth. As a result, the measured rms noise decreases with a factor of the square-root of the increase in the observed amplifier output rise time. It is therefore concluded that the baseline noise that was measured for the fabricated analog memory circuit is limited by the noise in the amplifier. The theoretical kT/C sampling cell noise value could be achieved by modifying the amplifier design, or reducing its bandwidth; a reduction in bandwidth will increase the memory readout time.

6.3.2 Dc Transfer Characteristic

The nonlinearity of the experimental circuit was measured by applying 38 equally spaced input voltages and fitting the output levels to a straight line using the least-squares method. Figure 6.7(a) shows the output of a typical cell plotted as a function of input voltage over a range of 3 V, and in Figure 6.7(b) the deviations are shown for the chosen input voltage range of 2.5 V. The maximum deviation is 0.7 mV, or 0.03% of full scale.

The average small-signal gain of a memory channel at low frequencies was measured to be 0.9967, with an rms gain variation across the channel of 0.0001, as indicated by Figure 6.8. The attenuation of the input signal is due to the input-to-output capacitance, C_{pp} , of the folded-cascode amplifier

$$A_i = \frac{1}{1 + \frac{C_{pp}}{C_i}} . \quad (6.4)$$

C_{pp} is governed by the gate-to-drain capacitance of the amplifier input transistor M_2 , divided by the voltage gain of the cascode transistor M_6 in Figure 5.1,

$$C_{pp} = \frac{C_{GD}(M_2)}{Gain(M_6)} . \quad (6.5)$$

C_{GD} is approximately 40 fF for the input device in the fabrication process used; with a calculated voltage gain of 60 for the cascode device, a value for C_{pp} of approximately 1 fF is

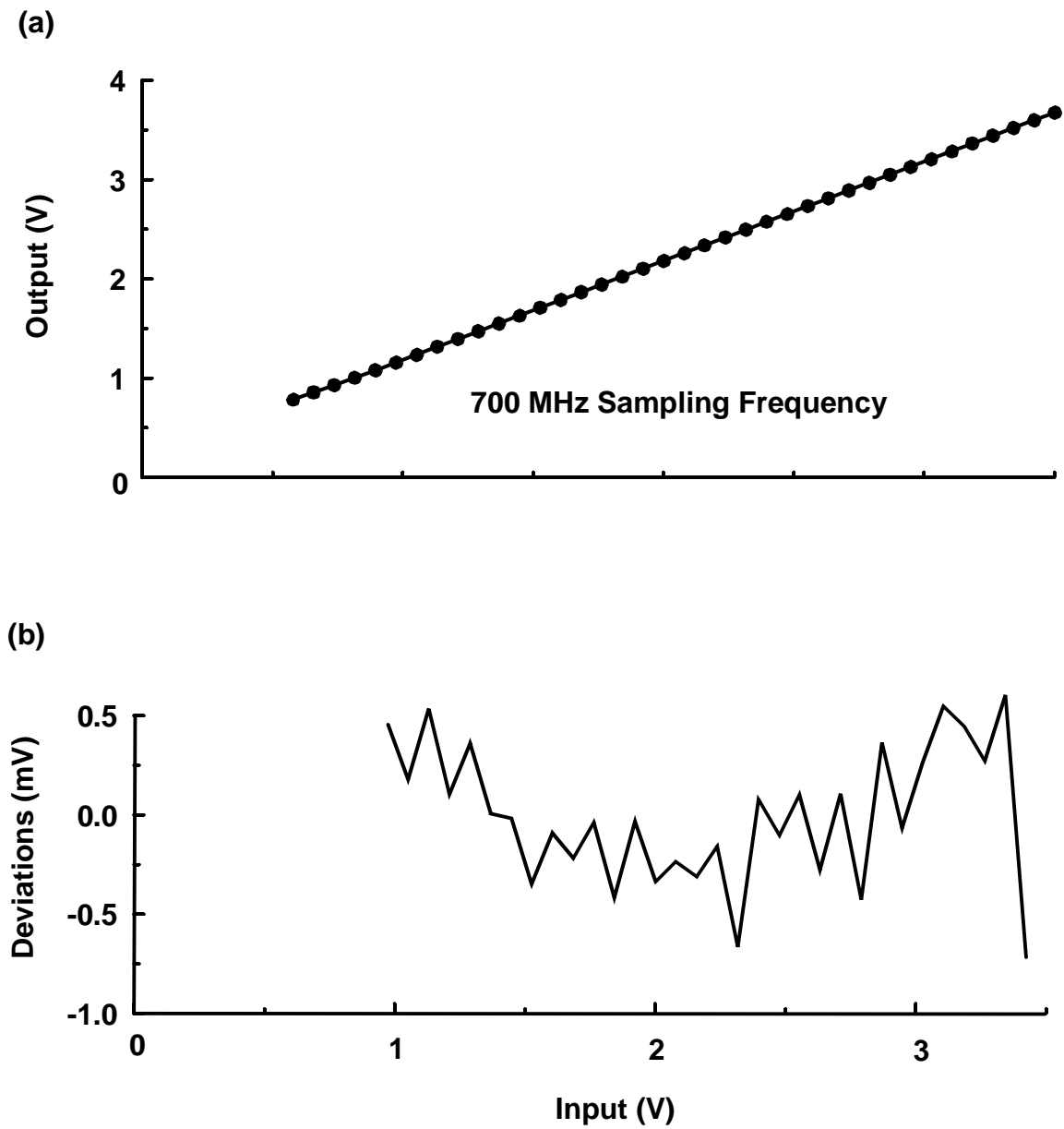


Figure 6.7: (a) Output plotted as a function of input voltage. (b) Deviations from a linear fit for the selected 2.5 V input signal range.

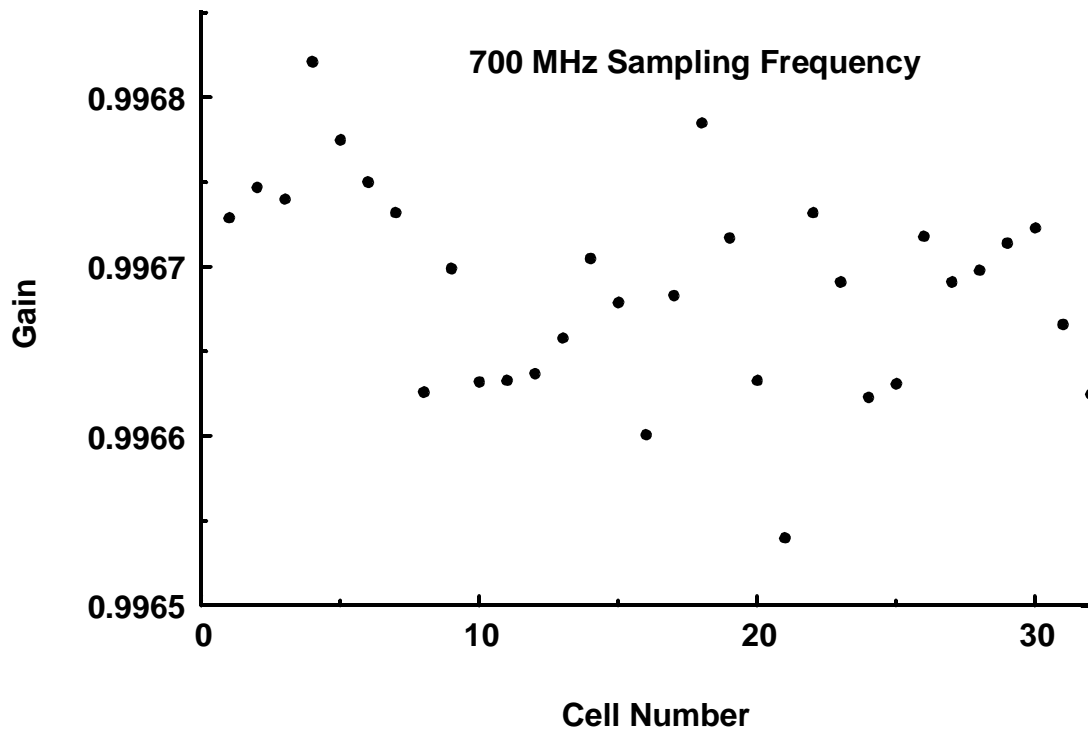


Figure 6.8: Gain of all 32 cells in one channel.

obtained. The resulting gain, A_i , is 0.998, which approximately agrees with the measured gain average of the analog memory.

The measured pedestal voltages for the 32 cells in a channel are plotted in Figure 6.9 as a function of the input voltage with the average response of the channel subtracted. The cell-to-cell pedestal variations result in an rms deviation from the average of 1.8 mV across a channel. This is expected for the design's switch and capacitor sizes and the fabrication process used.

In order to investigate whether the cell pedestals depend on the input signal, the responses to various dc input levels were recorded, and the response to one dc reference level, $V_{in} = 2$ V, was subtracted from these measurements. The differences for all 32 cells are plotted in Figure 6.10 as a function of the input voltage. In order to plot the data on the same scale, the average channel response has been subtracted. Each data point represents the mean value from five measurements so that variations due to baseline noise (0.3 mV)

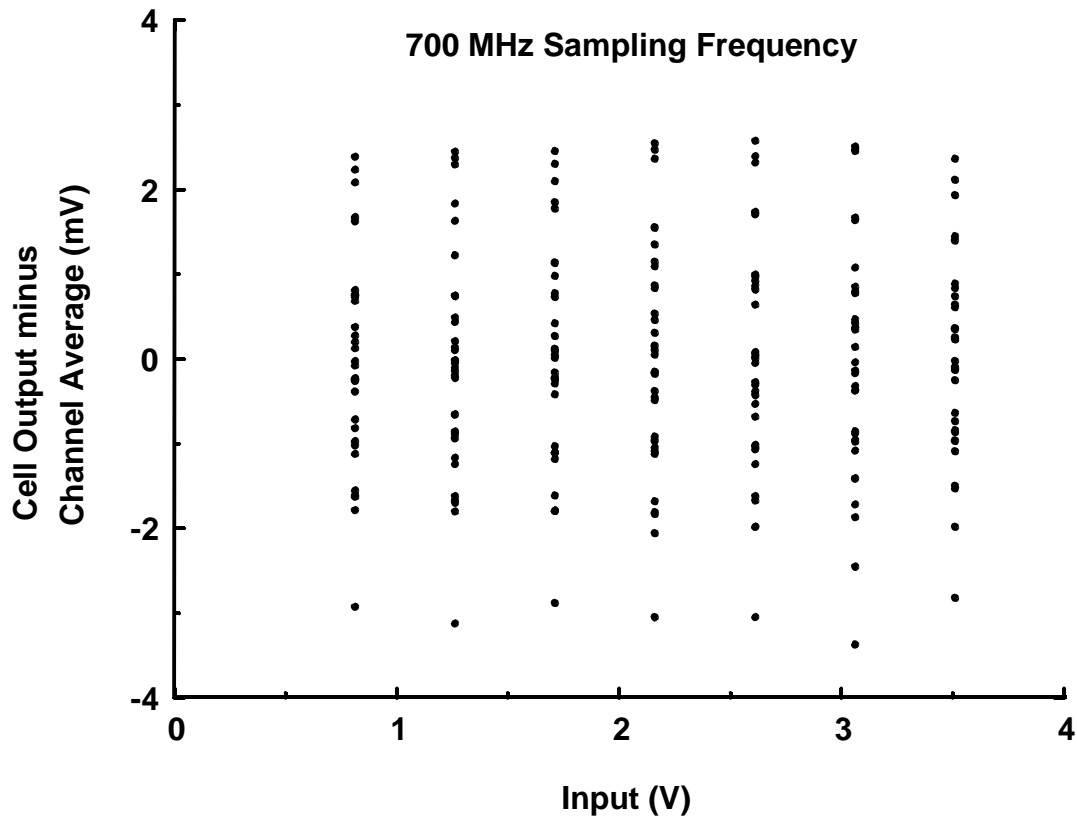


Figure 6.9: Cell pedestals as a function of input voltage for the 32 memory cells.

are attenuated by a factor of two. The rms cell response variation after cell pedestal subtraction across the whole input signal range is only 0.3 mV, demonstrating that the sampling switch charge injection is independent of the dc input level and can be reduced to the level of the baseline noise by a simple subtraction. Calibration and correction of the channel response therefore requires only a simple cell pedestal subtraction in order to achieve a precision of better than 12 bits for dc signals.

The last parameter obtained from the dc measurements was the parasitic capacitance C_{pi} in Figure 4.5. This capacitance was experimentally determined by recording the mem-

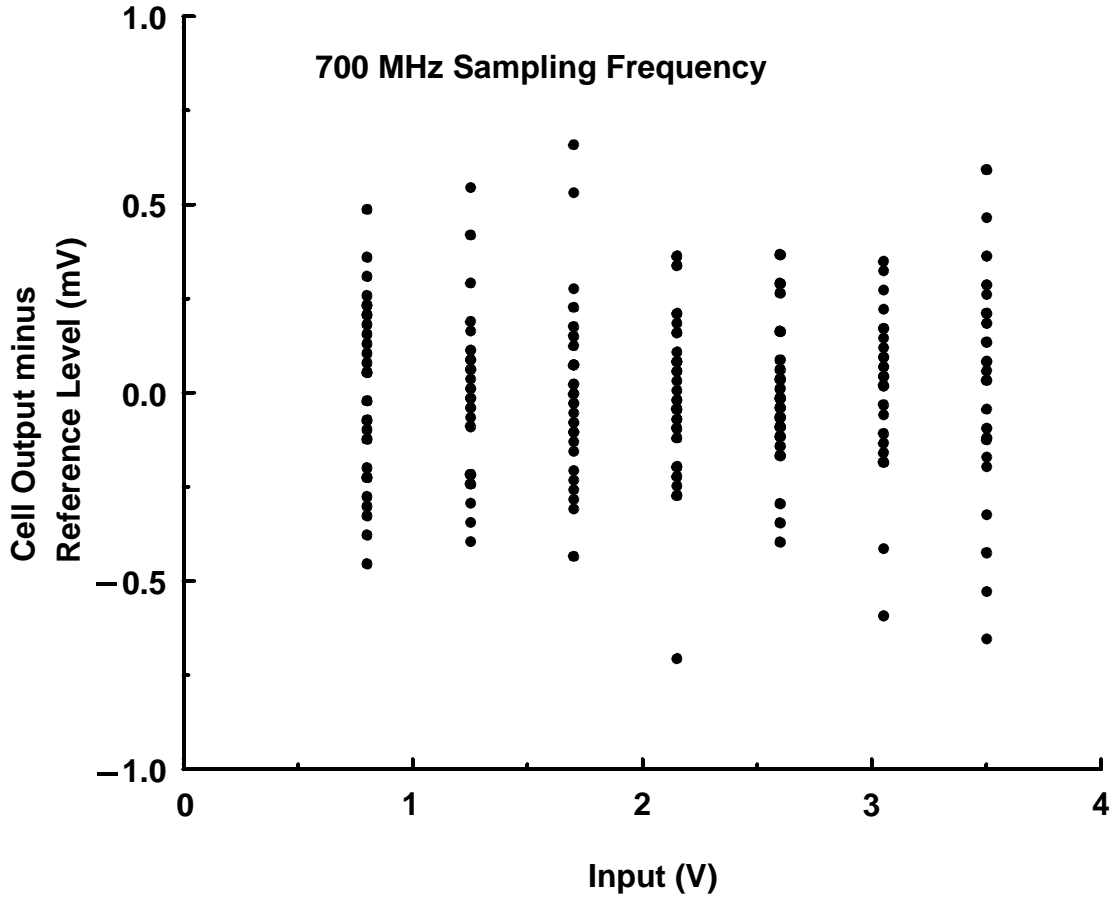


Figure 6.10: Cell pedestals after baseline subtraction.

ory output voltage as a function of the applied dc reference voltage V_B . From (4.13) and (4.14), C_{pi} can be calculated from the change in the memory cell offset voltage ΔV_{off} as

$$C_{pi} = C_i \left(\frac{\Delta(V_{off} - V_B)}{\Delta V_B} \right) + C_{ox} W_{ri} L_{ri} . \quad (6.6)$$

From this equation, a value for C_{pi} of 100 fF was obtained. For the experimental circuit, capacitance C_{pi} , as defined in (4.3), comprises the parasitic bottom plate capacitance C_{ss} of the sampling capacitor and the source-to-substrate capacitance C_{wss} and the gate-overlap capacitance C_{wi} of the large write switch. From the fabrication process parameters

these capacitances were estimated to have the following values: $C_{wss} = 25$ fF, $C_{wi} = 13$ fF, and $C_{ss} = 40$ fF. The total parasitic capacitance, C_{pi} , is thus 78 fF, which agrees well with the value obtained from the measurements. The bottom plate of the sampling capacitance was intentionally placed at the terminal connected to the cell transistors so as to minimize the parasitic capacitance of the input bus. This benefits the ac performance as discussed in Section 4.2.7. The resulting increase in the cell pedestal voltage of approximately 10% is not crucial, since these cell pedestals are cancelled in the subtraction procedure.

6.3.3 Ac Response of the High-Speed Memory

The ac performance of the circuit was quantitatively evaluated by applying free running sine waves of various amplitudes and frequencies at the analog input. Since the phase of the input signal was not synchronized to the sampling process, the results also provide a measure of the ac uniformity of the cells across a channel. The pedestal-subtracted responses for 20 separate sets of measurements were fitted to an ideal sine wave with a common frequency, offset, and amplitude and a free phase for each set of measurements [53], [54]. The signal-to-(noise+distortion) ratio (SNDR) was then calculated based on the residuals from an ideal fit. The errors can be attributed to a variety of sources, including errors in sampling time and amplitude, variations in the ac response of different cells, nonlinearities, and electronic noise.

Figure 6.11 shows a 100-mV_{pp}, 21.4-MHz sine wave fitted to the data and plotted modulo the phase along with the residuals. The fit yields rms residuals of 0.4 mV. The amplitude and residuals remain stable for various dc input voltage levels, demonstrating the good small-signal ac linearity across the signal range. Figure 6.12 depicts the memory response and the deviations from an ideal curve for a 2-V_{pp} sine wave. The rms value of the residuals is 3.4 mV. Shown in Figure 6.13 is a plot of the SNDR as a function of the input amplitude, as measured for the 21.4 MHz input frequency. An input level of 0 dB represents a full-scale peak-to-peak amplitude of 2.5 V. The circuit achieves a peak SNDR of 60 dB and a dynamic range of 74 dB.

The performance of the analog memory degrades at large signal amplitudes principally because of amplitude distortion and timing errors.

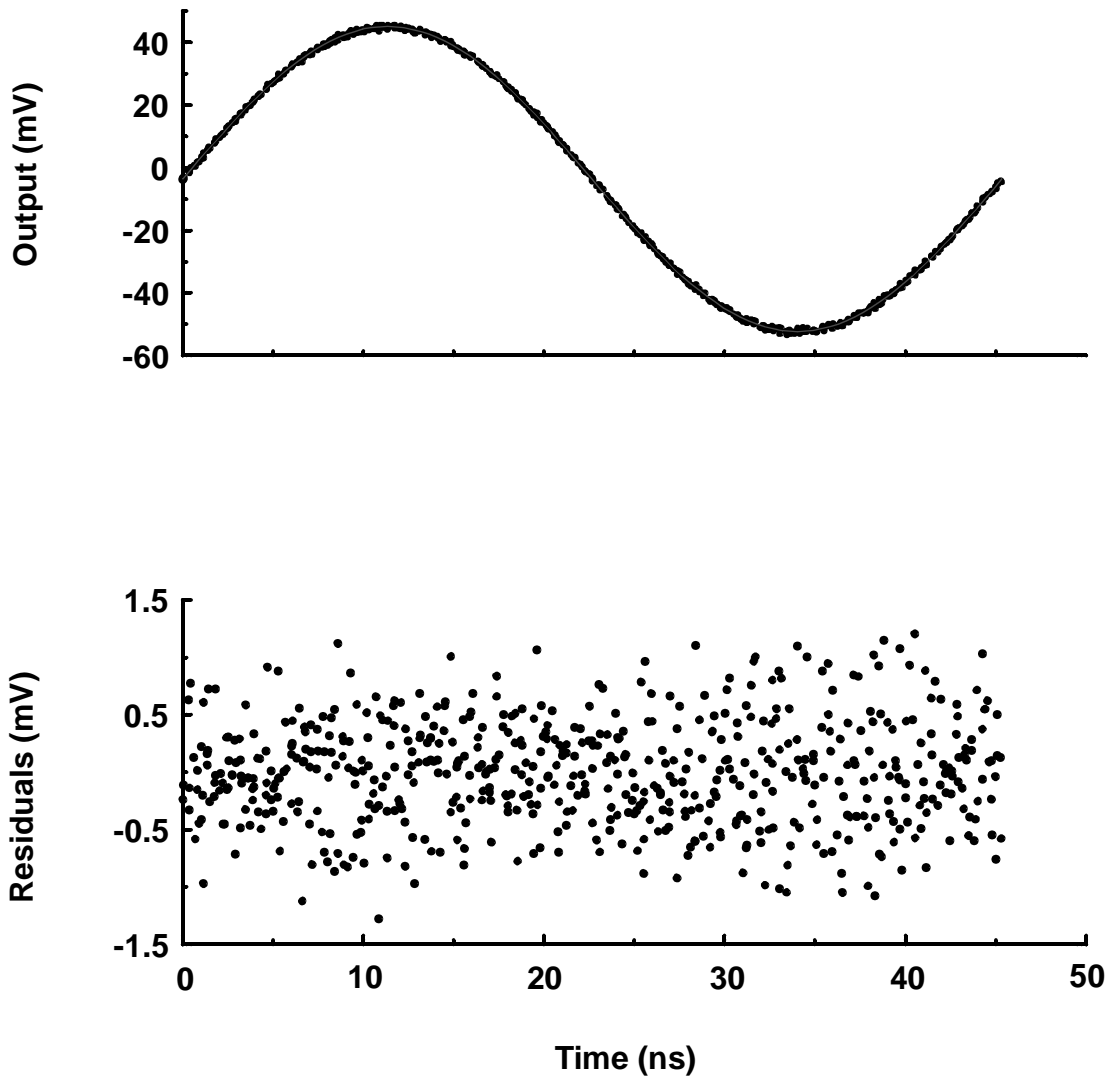


Figure 6.11: Upper: Results of 20 measurement sets from a 100-mV_{pp}, 21.4-MHz sine wave sampled at 700 MHz and plotted on a time scale modulo the period of the sine wave. Lower: Residuals from the fit to the ideal curve.

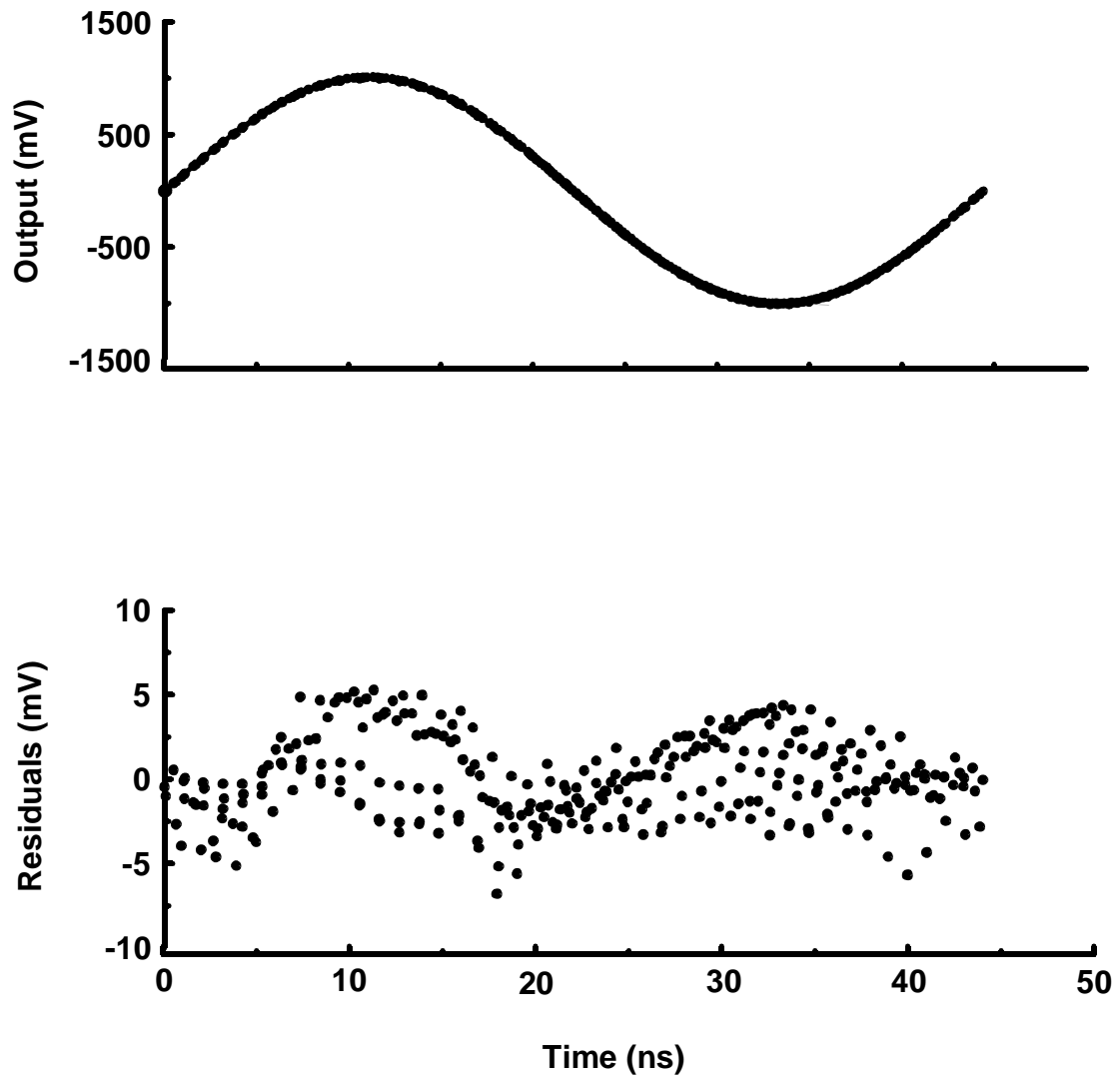


Figure 6.12: Upper: Results of 20 measurement sets from a 2-V_{pp} , 21.4-MHz sine wave sampled at 700 MHz and plotted on a time scale modulo the period of the sine wave. Lower: Residuals from the fit.

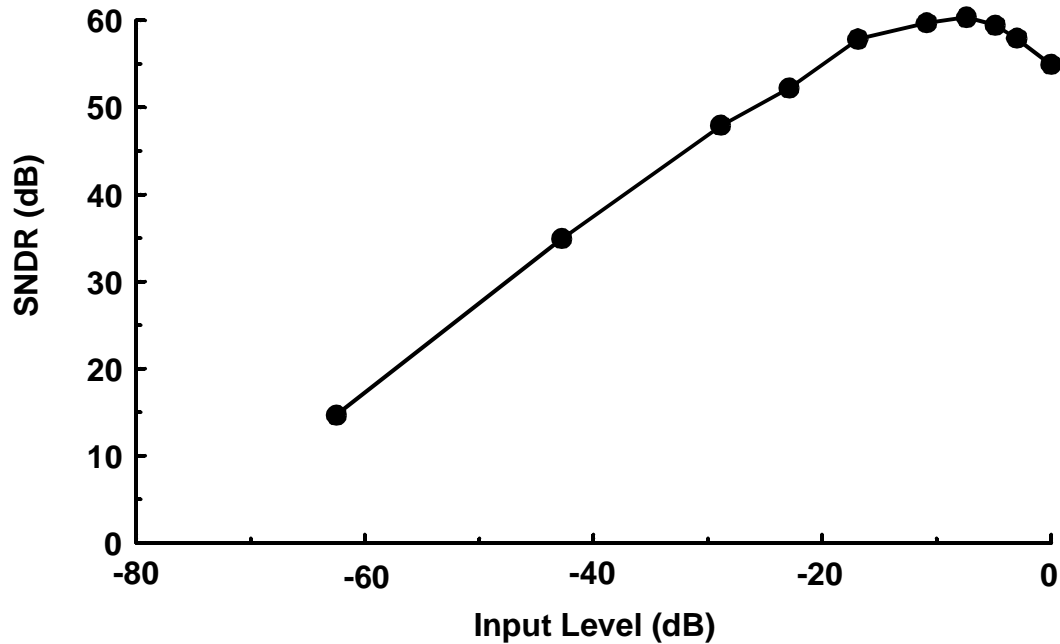


Figure 6.13: Signal-to-(noise+distortion) ratio as a function of input amplitude for a 21.4-MHz sine wave sampled at 700 MHz.

6.3.4 Timing Errors and Distortion in the High-Speed Memory

Errors in the sampling time can be attributed primarily to two sections of the circuit, the delay chain and the feedback control. The total delay of the inverter chain is regulated by the feedback control circuit. The peak-to-peak timing jitter measured at the end of the 32 stage delay chain is less than 1 ns, which translates into 31 ps per sampling interval or delay element. This jitter corresponds to a sampling frequency error of 2% at the 700 MHz rate and will decrease linearly with an increase in the number of delay elements. An additional error is introduced by cell-to-cell sampling time, or delay, variations. These variations have been estimated by fitting the measurements to a sine wave with the individual delays of the elements as parameters (with the same element delays for each of the 20 measurements sets). The best fit yielded an rms value of 25 ps for the element delay varia-

tions across a channel. This timing error is independent of the input signal level and can be corrected for if required.

As explained in Appendix C, the input of the analog memory was driven from a 50 ohm source in the test setup. For applications where high-frequency input signals must be sampled, a lower impedance driver must be added at the memory signal input so as to avoid distortion that results from variations in the memories input capacitance during the write phase.

6.3.5 Ac Response of the Low-Speed Memory

The ac performance of the analog memory version with the shift-register write control was measured for a 2-MHz input sine wave. The external write clock that controls the dynamic two-phase write shift register was set to 13 MHz. In Figure 6.14 the output responses of the memory cells are shown together with the deviations from an ideal sine wave. The rms deviations are 0.3 mV for the 100-mV_{pp} sine wave. Shown in Figure 6.13 is a plot of the SNDR as a function of the input amplitude. A peak SNDR of 54 dB was achieved.

6.4 Summary

The implementation of a two-channel analog memory with 32 cells in each channel has been described in this chapter. Two versions of the chip were fabricated; a low-speed version that employs a dynamic shift register for write control and a high-speed circuit that uses an inverter delay chain for write control. Measurement results at sampling rates as high as 700 MHz were presented. The dc performance proved to be identical for the two versions of the analog memory. The dc and ac results of the performance tests are summarized in Table 6.2. The peak SNDR obtained for the low-speed memory is lower than the result reported for the high-speed memory. This may be due to perturbations caused by the external write clock generated on the test board, routed on board traces to the chip package, and connected via bonding wires and on-chip traces to all stages of the write shift register. Conversely, the clock signals in the high-speed memory are generated locally on-chip and are thus confined to a small area on the chip.

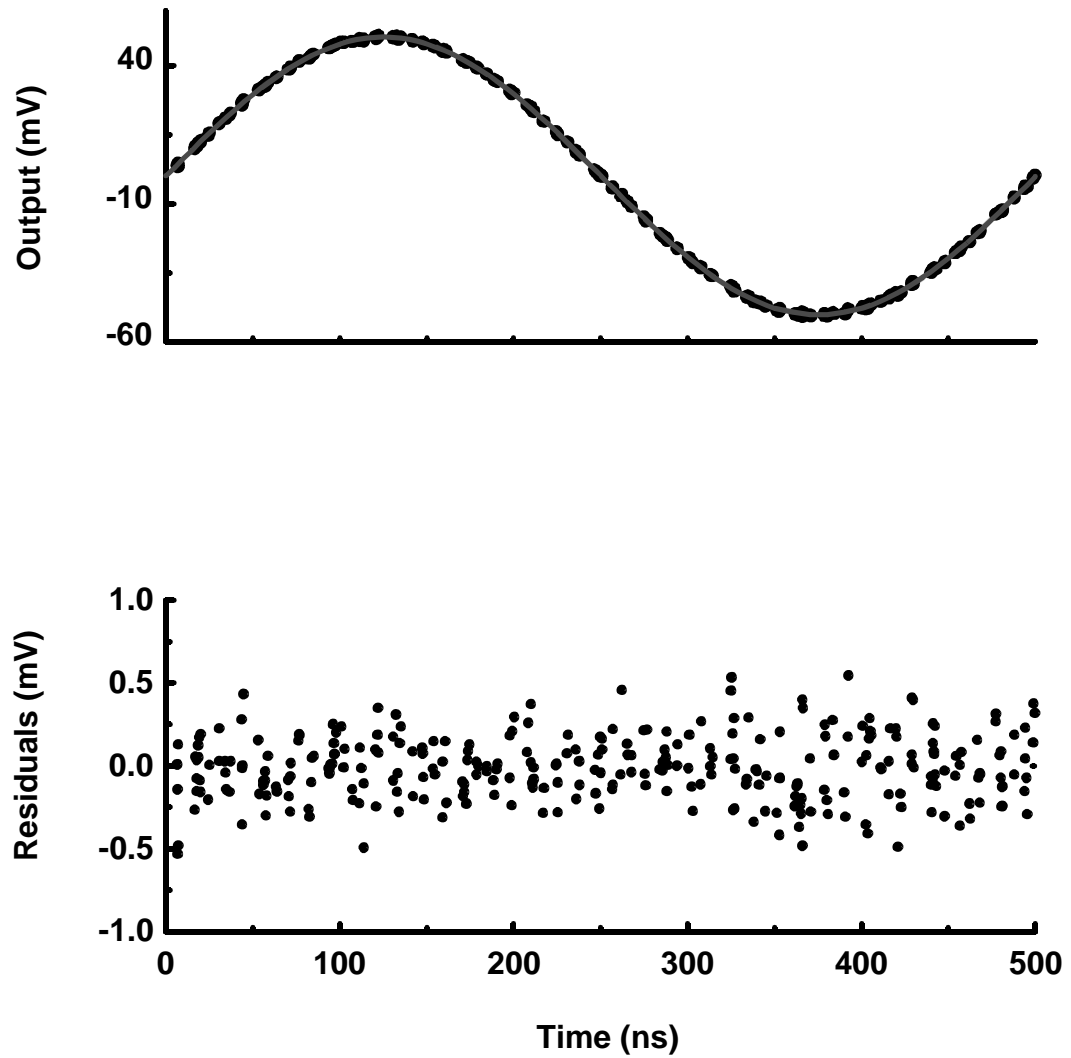


Figure 6.14: Upper: Results of 20 measurement sets from a 100-mV_{pp} , 2-MHz sine wave sampled at 13 MHz and plotted on a time scale modulo the period of the sine wave. Lower: Residuals from the fit.

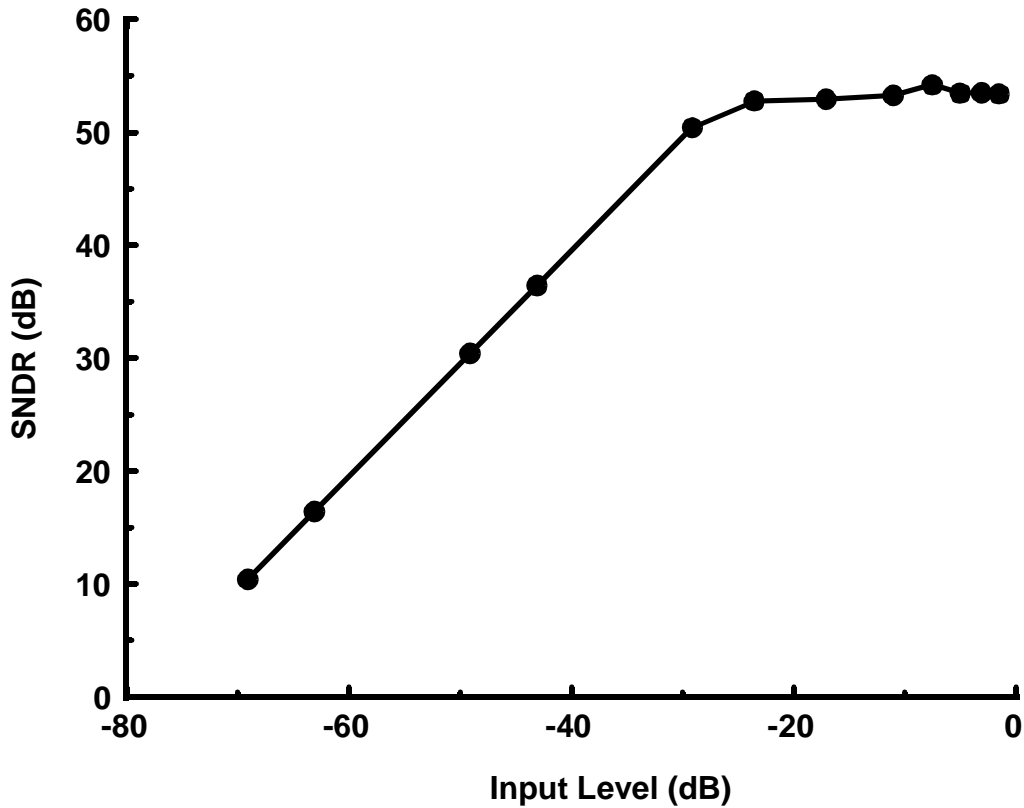


Figure 6.15: Signal-to-(noise+distortion) ratio as a function of input amplitude for a 2 MHz sine wave sampled at 13 MHz.

It was shown that the measured baseline noise for the fabricated circuits is limited by the amplifier and that this noise can be reduced by increasing the readout time. The maximum sampling rate for the high-speed memory was 700 MHz and could potentially be increased through use of a more advanced process technology.

In Figure 6.16 the dynamic range is shown as a function of the sampling rate for several circuits that can be used for analog waveform acquisition, including analog-to-digital converters. In Table 6.3 the components represented by data points A through R are listed. Data points A through C are published analog memory devices and correspond to the designs reported in [16], [18], and [20], respectively. Data points D through Q correspond to commercial and recently published analog-to-digital converters as specified in

Rms noise floor	0.3 mV
Cell offset variation across full input range uncorrected	1.8 mV
with reference level response subtracted	0.3 mV
Nonlinearity (for 2.5 V full scale)	0.03%
Cell gain nonuniformity (mean gain: 0.9967)	0.01%
Dynamic range	74 dB
Power dissipation of one channel (+5 V)	2 mW
Low-speed version: Peak SNDR (2 MHz input sine wave, 13 MHz sampling frequency)	54 dB
High-speed version: Minimum sampling frequency	200 MHz
Maximum sampling frequency	700 MHz
Peak SNDR (21.4 MHz input sine wave, 700 MHz sampling frequency)	59 dB

Table 6.2. Analog memory performance summary.

Table 6.3. The data point R represents the performance of the high-speed memory presented in this work. Analog memory circuits not commercially available or not published have not been included. It should also be noted that the power dissipation for the analog-to-digital converters listed are between 1 and 10 W, whereas the proposed circuit only dissipates 2 mW.

Data Point	Component
A	[16]
B	[18]
C	[20]

Table 6.3. Analog memories and commercial converters compared in Figure 6.16.

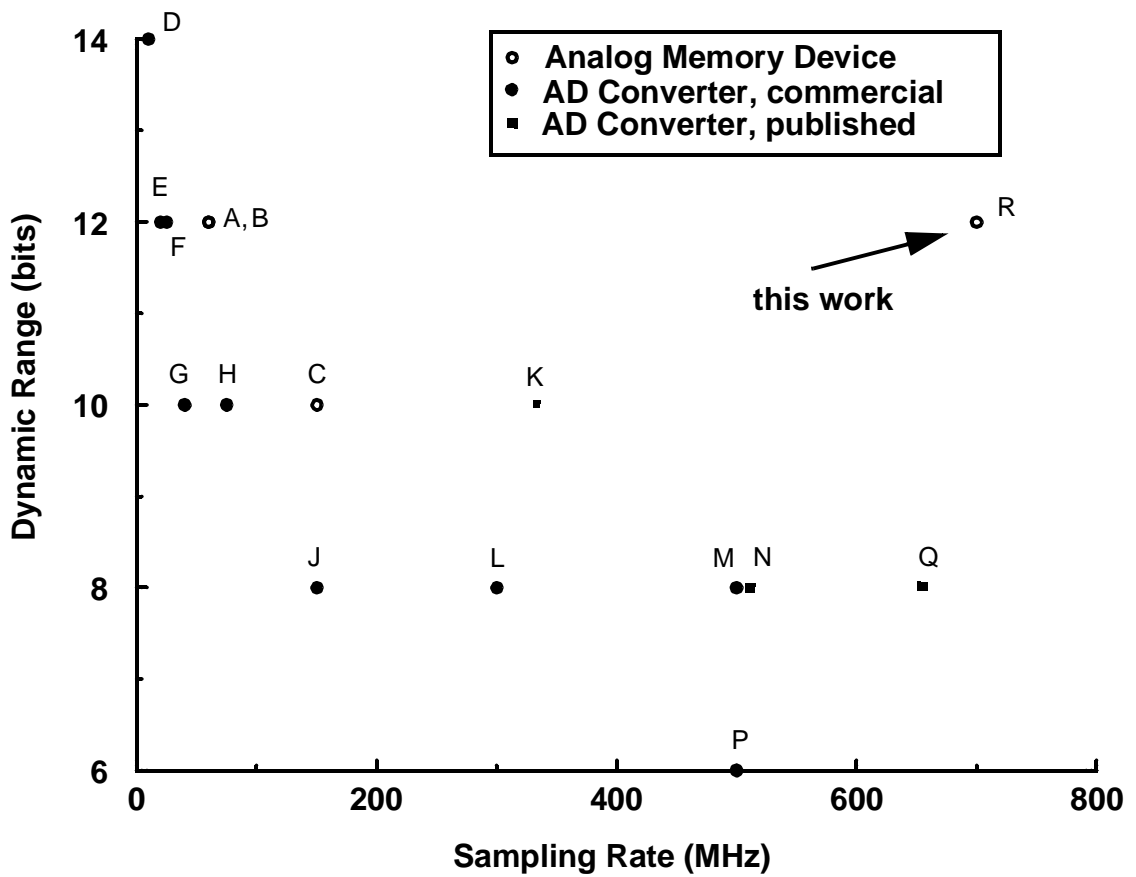


Figure 6.16: Comparison to published analog memories and commercial converters.

Data Point	Component
D	Analog Devices AD9014
E	Analog Devices AD9032
F	Signal Processing Technology SPT7922
G	Signal Processing Technology SPT7824
H	Analog Devices AD9060
J	Signal Processing Technology HADC77100

Table 6.3. Analog memories and commercial converters compared in Figure 6.16.

Data Point	Component
K	[55]
L	Tektronix TKAD20
M	Tektronix TKAD10
N	[56]
P	Analog Devices AD9016
Q	[57]
R	This work

Table 6.3. Analog memories and commercial converters compared in Figure 6.16.

Chapter 7

Conclusions and Suggestions

7.1 Conclusions

A wide range of data acquisition applications require the recording of analog waveforms at a high rate and with high resolution. In acquisition systems employed for the recording of pulse echo phenomena (radar, lidar, ultrasonics, non-destructive material or medical testing), for pulse shape recording (high-energy physics experiments, accelerator diagnostics), and for laboratory instrumentation (oscilloscopes, transient digitizers), the analog waveforms need only be captured for a limited period of time; a continuous digitization is not required.

Primarily three approaches are used to record fast analog waveforms: high-speed analog-to-digital converters, charge coupled devices, and switched-capacitor analog memories. Analog-to-digital converters are presently limited to a dynamic range of at most 8-bits for sampling rates above 100 MHz. The power dissipation and cost of such fast ADCs prohibit direct digitization solutions for most acquisition systems with a large number of signal channels. High-speed charge coupled devices are expensive and typically require elaborate clocking circuitry that generally dissipates considerable power. Furthermore, a large dynamic range is hard to achieve at high sampling rates using CCDs. This research has therefore concentrated on switched-capacitor analog memories. Published analog

memory circuits with a dynamic range of more than 10 bits are presently limited to sampling frequencies of 150 MHz.

The goal of this research was to investigate analog memories for waveform sampling at several hundred MHz while maintaining a dynamic range of 12 bits. A great deal of effort was devoted to optimizing the analog memory architecture and circuit implementation for uniformity of memory cell responses within a channel. This is especially important in high-energy physics signal acquisition systems, where analog waveforms of thousands of channels are recorded. In such applications it is especially important to minimize the complexity of dc and ac calibration and correction procedures, as well as the number of calibration constants needed to correct the data.

Following an examination of the characteristics of MOS switches and capacitors, this work has analyzed their performance in a number of sample-and-hold configurations. Expressions for the error voltages from switch charge injection were derived for circuits wherein the sampling capacitance is not large compared to the parasitic capacitances associated with the sampling switch. It was analytically shown that the sampling switch must be inserted in the signal-return path so as to eliminate cell-specific gain and sampling time errors that are dependent on the input signal level.

Current analog memories exhibit one of two drawbacks: input signal dependent pedestal voltages and sampling times, or memory cell gains that are directly related to the sizes of the sampling capacitances. Based on the results obtained from the investigation of the sample-and-hold circuits, an analog memory architecture was proposed that eliminates both drawbacks. The transfer function of this memory was derived and then verified by measurement results obtained from experimental integrated circuit implementations. The measured gain uniformity across a channel was better than 13 bits, which indicates that the memory cell gain is insensitive to the absolute size of the sampling capacitance. It was also shown that the memory cell pedestal voltages are independent of the input signal voltage and that the cell specific pedestal voltages can be cancelled by a simple subtraction procedure.

Each channel of the analog memory incorporates an on-chip amplifier for readout. Results from simulation and experiment show that the folded-cascode amplifier circuit is well-suited for use in this application. An open-loop gain in excess of 70 dB was obtained

at a power dissipation of 400 μ W. The output voltage range of such an amplifier is a good match to the voltage range of the analog memory cells.

Commonly a shift register or, for high-speed operation, banks of inter-leaved shift registers are used for write addressing in an analog memory. At high sampling speeds, the variations in cell-to-cell sampling times due to the sensitivity of on-chip delays to the fabrication process, the temperature, and the power supply levels are considerable, and extensive ac timing correction procedures are required. In addition, a high-speed sampling clock must be provided to the circuit. This thesis proposed the use of an inverter delay chain for write control, which avoids the need for a high-speed external clock and optimizes the uniformity of the cell-to-cell sample periods across a channel. This write control circuit is insensitive to variations in the fabrication process, temperature, and supply levels because a servo feedback circuit is used to adjust the sampling rate. Furthermore, the high-speed write signals are confined to a small area on the die, and perturbations from external clocks that otherwise must be distributed across the entire chip are avoided.

A 2-channel x 32-cell analog memory for use in a beam position monitoring system was fabricated in a 2- μ m CMOS technology with poly-poly capacitors, and operated at sampling rates as high as 700 MHz. Its measured cell-to-cell sampling time variation is 20 ps. The measured nonlinearity is 0.03% for a 2.5 V input range, and the cell-to-cell gain matching is 0.01% rms. The uniformity of the individual memory cell responses across the whole input voltage range exceeds 12 bits after a simple cell offset subtraction procedure. The dynamic range of the circuit is 13 bits, and the peak signal-to-(noise+distortion) ratio for a full-scale 21.4 MHz sine wave sampled at 700 MHz is 60 dB. The power dissipation for one channel operated from a single +5 V supply is 2 mW. The memory has been optimized for high-energy physics applications where, in general, different classes of signals covering a wide dynamic range must be processed in a channel, but where each class of signals has a limited inherent accuracy. For each class of signals it is thus sufficient to have a peak SNDR that is lower than the dynamic range of the channel.

The proposed analog memory is a viable alternative to real-time analog-to-digital converters in applications where continuous acquisition is not required. The power dissipation of the circuit is orders of magnitude below typical of commercial monolithic

converters, which are presently limited to a dynamic range of 8 bits for sampling rates exceeding 100 MHz.

7.2 Future Work

A number of ideas developed in the course of this research appear to merit further investigation.

- The integration of an analog-to-digital converter with the analog memory on a single die would enable an implementation of an on-chip digital correction circuit, as depicted in Figure 2.3. An analog-to-digital waveform converter with an accuracy and a dynamic range of 12 bits at sampling rates of several hundred MHz could then be realized on a single chip.
- The maximum sampling rate of the analog memory is limited by the delays of the inverters in the write control circuit, as explained in Section 4.3. The increase in speeds achievable in more advanced CMOS technologies could be leveraged to increase the sampling rate. It should be possible to attain sampling speeds of 2 GHz in submicron technologies.
- The input capacitance of the analog memory varies during the write phase. This capacitance must therefore be driven by a low output-impedance buffer to avoid signal distortion at high input frequencies. The use of BiCMOS technology might allow the integration of such a unity-gain buffer with the analog memory.
- The proposed analog memory architecture employs a common input switch and was optimized for short record lengths. Some applications (e.g. oscilloscopes) call for a large number of memory cells in a channel. A single-channel memory with up to several thousand memory cells is feasible, limited by the physical chip size. However, to achieve a high input bandwidth in such a channel, it may be necessary to replace the common input switch with cell-specific input switches.
- The analog memory introduced in this thesis is single ended. A differential architecture may result in a circuit with superior dynamic range. However, the effects of a differential implementation on the cell-to-cell response uniformity must be investigated.

Appendix A

Switch Charge Injection

Commonly, the error voltage on a sampling cell capacitor that results from switch charge injection (the pedestal voltage) is analyzed under the assumption that the sampling capacitance is large compared to the oxide capacitance of the sampling switch [36]. Since this assumption is not valid for high-bandwidth switched-capacitor cells, an expression for the pedestal voltage in such cells is derived in this Appendix.

Shown in Figure A.1 is a switched-capacitor memory cell with sampling capacitance C_S and transistor M . The transistor is inserted in the signal return path, as described in Chapter 4. Also included in the figure are parasitic capacitances associated with the sampling switch. C_o is the gate oxide capacitance, C_p is the parasitic capacitance to ground, and C_{ov} is the gate overlap capacitance. V_{in} and V_D are assumed to be constant potentials. For this analysis a single-lump model [36] of the transistor is used. The transistor node connected to C_S is defined as source since the voltage at this node is assumed to be equal or less than V_D during the sampling process. The pedestal voltage can be analyzed in a similar fashion for a circuit where the drain and source terminals are interchanged.

The transistor is turned off by changing the gate voltage, V_G , from the high voltage level, V_H , to the low level, V_L . The gate voltage is assumed to be a ramp function with a slope U ,

$$V_G = V_H - Ut. \quad (\text{A.1})$$

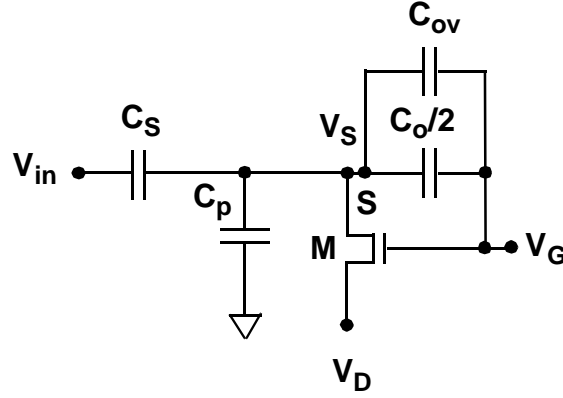


Figure A.1: Schematic of the switched-capacitor cell.

As long as the transistor is in the strong inversion region ($V_H \geq V_G \geq V_S + V_T$), its drain-to-source current can be described as [49]

$$I_{DS} = \beta \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}, \quad (\text{A.2})$$

where $V_{DS} = V_D - V_S$ is the transistor drain-to-source voltage, $V_{GS} = V_G - V_S$ is the transistor gate-to-source voltage, V_T is the threshold voltage, $\beta = \mu_n C_{ox} W/L$, μ_n is the electron mobility in the channel, C_{ox} is the oxide capacitance per unit area, and W and L are the channel width and length of the transistor, respectively. (A.2) can also be written as

$$I_{DS} = \beta \left(V_{GD} - V_T + \frac{V_{DS}}{2} \right) V_{DS}, \quad (\text{A.3})$$

where V_{GD} is the transistor gate-to-drain voltage. For small drain-to-source voltages (A.3) can be approximated by

$$I_{DS} = \beta (V_{GD} - V_T) V_{DS}. \quad (\text{A.4})$$

From the Kirchhoff's Current Law at node S in Figure A.1,

$$C_{eq} \frac{dV_S}{dt} = - \left(C_{ov} + \frac{C_o}{2} \right) U + I_{DS}, \quad (\text{A.5})$$

where

$$C_{eq} = C_S + C_{ov} + C_o/2 + C_p. \quad (\text{A.6})$$

The solution for this differential equation can be derived with the general solution [58, 59, 60]

$$V_S - V_D = e^{x^2} (A + B \operatorname{erf}(x)) , \quad (\text{A.7})$$

where

$$\operatorname{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-u^2} du . \quad (\text{A.8})$$

Differentiation of (A.7) yields

$$\frac{d}{dt}(V_S - V_D) = \left(2x(V_S - V_D) + B \frac{2}{\sqrt{\pi}} \right) \frac{dx}{dt} . \quad (\text{A.9})$$

If (A.2) and (A.9) are inserted into (A.5),

$$C_{eq} \left(2x(V_S - V_D) + B \frac{2}{\sqrt{\pi}} \right) \frac{dx}{dt} = - \left(C_{ov} + \frac{C_o}{2} \right) U + \beta (V_{GD} - V_T) V_{DS} . \quad (\text{A.10})$$

The variable x is now set to

$$x = \sqrt{\frac{\beta U}{2C_{eq}}} \left(t - \frac{V_H - V_D - V_T}{U} \right) . \quad (\text{A.11})$$

Inserting x into (A.10) and with the boundary condition that $V_S = V_D$ at $t = 0$ yields

$$B = - \frac{C_{ov} + \frac{C_o}{2}}{C_{eq}} \sqrt{\frac{U \pi C_{eq}}{2\beta}} . \quad (\text{A.12})$$

Inserting B into (A.7) with the above boundary condition yields

$$A = \text{Berf}\left(\sqrt{\frac{\beta}{2UC_{eq}}}(V_H - V_D - V_T)\right). \quad (\text{A.13})$$

The transistor turns off when the gate voltage in (A.1) falls to a threshold voltage above the source/drain potential. At that time, $t_1 = (V_H - V_D - V_T)/U$, variable x in (A.11) is zero. The voltage difference $(V_S - V_D)$ in (A.7), defined as the voltage V_{pA} , is then

$$V_{pA} = A. \quad (\text{A.14})$$

Inserting (A.12) and (A.13) in (A.14) yields

$$V_{pA} = -\frac{C_{ov} + \frac{C_o}{2}}{C_{eq}} \sqrt{\frac{\pi UC_{eq}}{2\beta}} \text{erf}\left(\sqrt{\frac{\beta}{2UC_{eq}}}(V_H - V_D - V_T)\right), \quad (\text{A.15})$$

where C_{eq} is defined in (A.6).

After the transistor turns off ($V_G \leq V_S + V_T$), only the gate overlap capacitance contributes to the pedestal voltage, and with the approximation that $V_S \approx V_D$

$$V_{pB} = -\frac{C_{ov}}{C_S + C_{ov} + C_p} (V_D + V_T - V_L). \quad (\text{A.16})$$

The total pedestal voltage V_p after turn-off of the sampling switch is then

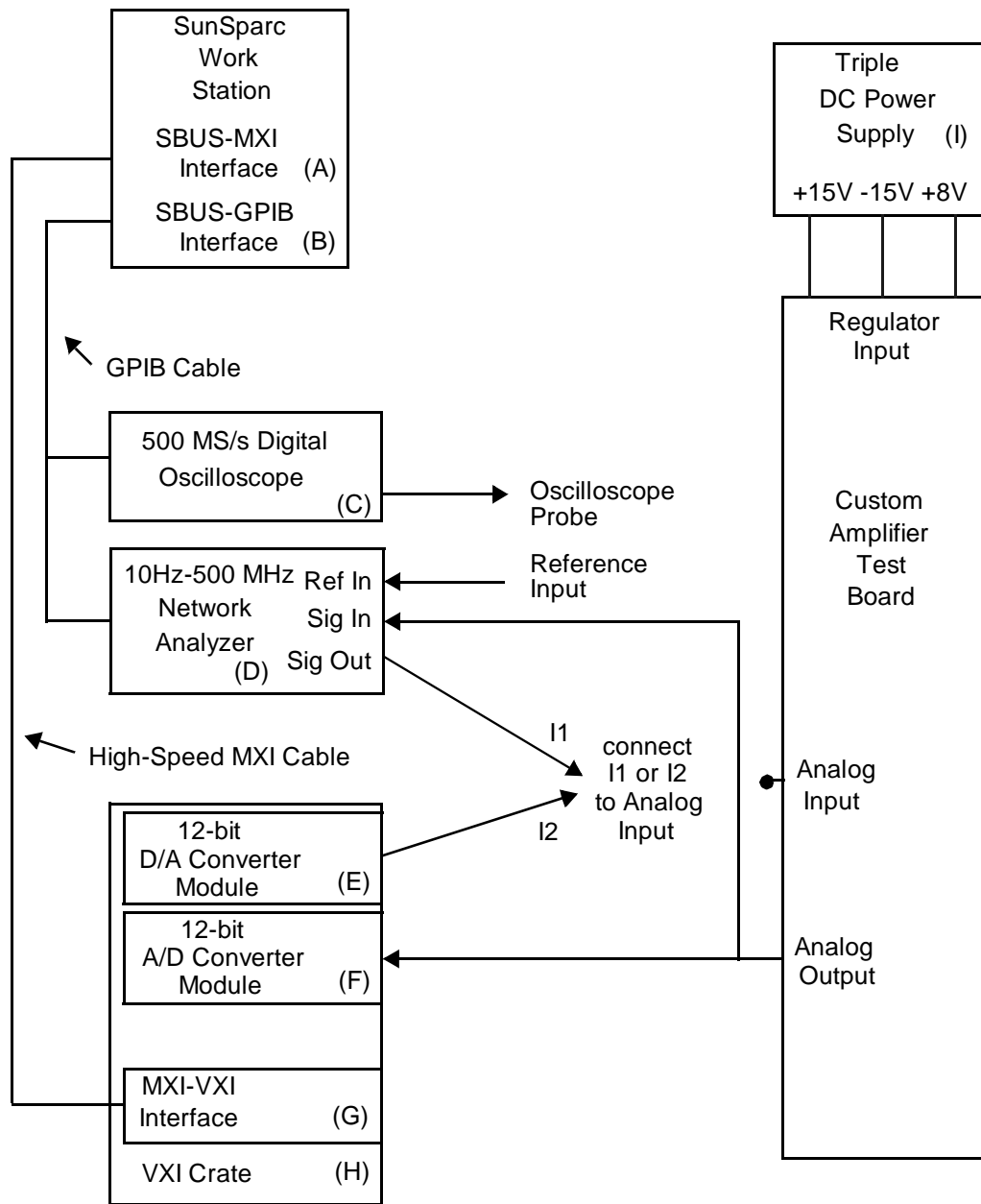
$$V_p = V_{pA} + V_{pB}. \quad (\text{A.17})$$

Appendix B

Amplifier Test Setup

This appendix describes the circuit configurations and the instruments used to characterize the performance of the folded-cascode operational amplifier. A block diagram of the measurement setup is shown in Figure B.1, and the instruments are identified in Table B.1. The amplifier is mounted on a custom printed circuit board together with supporting circuitry such as commercial amplifiers, resistors, capacitors, and voltage regulators. Acquisition of the measured data is controlled by a workstation via two SBUS interfaces, one to GPIB [61] and the other to MXI [62]. The following two VXI [63] modules are controlled via the high-speed MXI bus: the digital-to-analog converter module provides the dc voltages for the performance measurements, and the analog-to-digital module records the responses from the amplifier. With these modules dc parameters as input and output voltage ranges, linearity, and the input offset voltage can be measured. The frequency response of the device under test (DUT) is characterized by means of a network analyzer via the GPIB. The graphical LABVIEW [64] data acquisition software is used to control the instruments and process the data.

The test board comprises circuitry to test the DUT in two basic amplifier configurations, as a voltage follower and as a unity-gain inverter. Figure B.2 shows the follower circuit with a commercial high input-impedance (FET) operational amplifier in the feedback. This amplifier serves to drive the cable and the resistive load of the test instrumentation. Measurement errors from this amplifier can be neglected, since its performance with

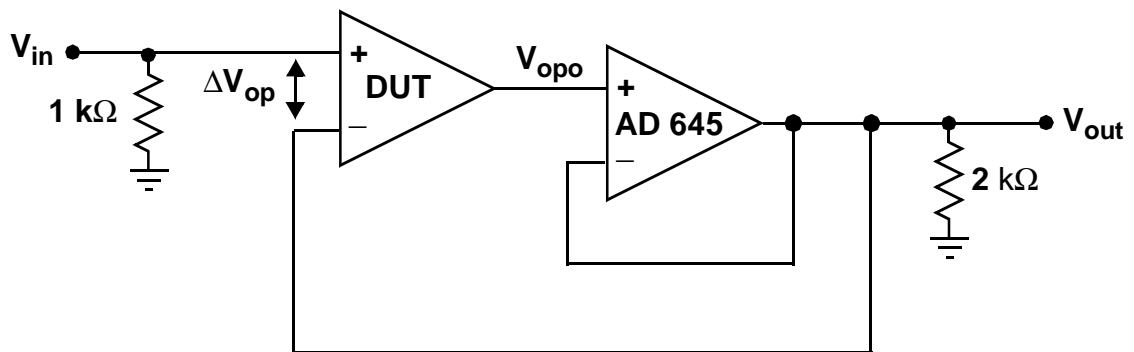


All connections Coax RG174 unless noted otherwise

Figure B.1: Experimental setup.

- A: National Instruments SB/MXI Interface, VXI-SB2020
- B: National Instruments GPIB-SPRC-B Interface
- C: Hewlett-Packard 2440 500Ms/S Digital Oscilloscope
- D: Hewlett-Packard 4195A Network Analyzer
- E: Hewlett-Packard E1328A 4-Channel D/A Converter
- F: Hewlett-Packard E1430A A/D Converter
- G: National Instruments MXI/VXI Mainframe Extender
- H: National Instruments VXI-1000 Mainframe
- I: Power Design TP340 Linear Triple Power Supply

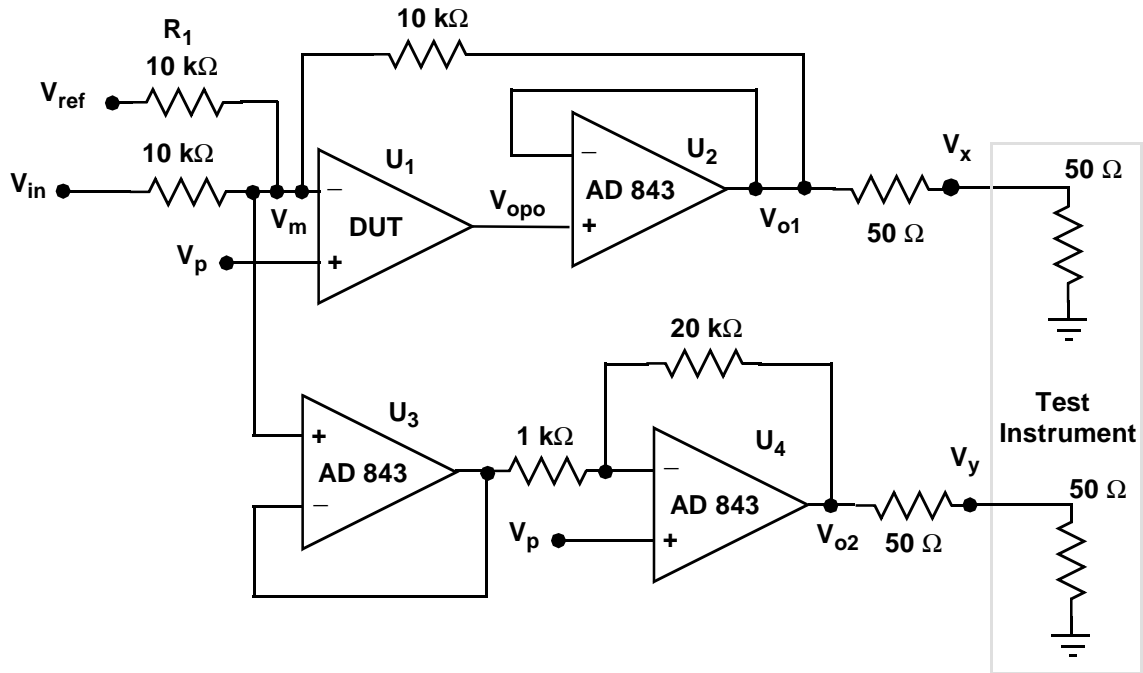
Table B.1: Test setup equipment list.



Note: Power supply and bypassing not shown.
 AD 645: Open-loop gain: 130 dB
 Offset voltage: 0.1 mV

Figure B.2: Test circuit with DUT in follower configuration.

respect to open-loop gain, linearity, voltage range, and offset voltage is considerably better than that of the folded-cascode CMOS amplifier. The linearity of the test setup without the DUT was determined by digitizing the voltage V_{out} as a function of the input voltage V_{in} applied directly to the noninverting input of the commercial amplifier, V_{oppo} (see Figure B.2). The measured integral nonlinearity was 0.01% over a 3 V voltage range. The offset and gain of the test system were found to be 0.1 mV and unity, respectively.



Note: Supply connections and bypassing not shown
 All resistors 1%
 AD 843: Open-loop gain: 100 dB
 Unity-gain bandwidth: 34 MHz

Figure B.3: Test circuit with DUT in inverter configuration.

Measurements of the transfer curve for the follower circuit yield the values for input offset voltage, dc open-loop gain, and unity-gain buffer voltage range presented in Chapter 5.

The circuit used to measure the dc output voltage range and the ac signal transfer characteristic is depicted in Figure B.3. The DUT is configured in the inverter configuration with a commercial high input-impedance amplifier, U_2 , employed to drive the resistive load and the cable to the test instrument. The amplifiers U_3 and U_4 are used to buffer and amplify the voltage at the inverting input of the DUT, V_m , which simplifies the signal transmission to the 50-ohm input of the test instrument. 50-ohm resistors were added in series with the outputs of amplifiers U_2 and U_4 to decrease the currents required from these amplifiers. The measured voltages V_x and V_y must therefore be multiplied by a factor

of two to obtain the values for V_{o1} and V_{o2} . Voltage V_{ref} is used to adjust the dc output voltage of the DUT. The output voltages of this circuit can be formulated as

$$V_{o1} = 2(V_x) = -(V_{in} + V_{ref} - 3V_p) \quad (\text{B.1})$$

and

$$V_{o2} = 2(V_y) = -20(V_m - V_p) , \quad (\text{B.2})$$

where V_{ref} and V_p are dc reference voltages. The offset voltages in the circuit have been neglected.

The output voltage range of the circuit is limited by the DUT and can be measured by recording V_x as a function of V_{in} . For a constant noninverting amplifier input voltage V_p and with $V_{ref} = V_p$,

$$V_{o1} = 2(V_x) = 2V_p - V_{in} . \quad (\text{B.3})$$

In order to obtain the small-signal ac transfer characteristic of the DUT, the output voltages V_x and V_y are recorded with the network analyzer sine-wave source signal connected to V_{in} . The supply voltage for the DUT in the setup is 5 V, V_p is 2.5 V, and the dc output bias voltage of the network analyzer is 0 V. Dc reference voltage V_{ref} and resistor R_1 in Figure B.3 are used to adjust the dc output voltage of the DUT, V_{opo} , to 2.5 V. Without R_1 the output of the DUT would be driven out of the linear range. When $V_{ref} = 2V_p$ one obtains

$$V_{o1} = V_p - V_{in} , \quad (\text{B.4})$$

The ac gain $G(f)$ of the DUT was measured by applying the sine wave at the input, $V_{in} = A_s \sin(2\pi f_s t + \phi_s)$, and recording the voltages V_x and V_y as functions of frequency f_s . The network analyzer then determines the magnitude and phase shift from these two voltages,

$$G(f) = \frac{V_{o1}(f)}{V_m(f)} = \frac{20V_x(f)}{V_y(f)} . \quad (\text{B.5})$$

Alternatively, voltage V_m can be measured directly with a high-impedance FET probe and the gain determined as follows.

$$G(f) = \frac{V_{o1}(f)}{V_m(f)} = \frac{(-2)V_x(f)}{V_m(f)} . \quad (\text{B.6})$$

As previously mentioned, measurement errors from the commercial amplifiers can be neglected because their open-loop gain and bandwidth are much higher than those of the folded-cascode CMOS amplifier.

Most of the measurement results presented in Chapter 5 are compared to results obtained from circuit simulations. In the simulations the commercial amplifiers were replaced by ideal amplifiers. The transistor models used in the simulations were extracted from devices manufactured in the same fabrication run as the amplifier. The transistor transfer curves were measured, and the transistor models were obtained using the TOPEX [65] extraction and optimization software.

Appendix C

Analog Memory Test Setup

The test setup used to evaluate the performance of the analog memory is described in detail in this appendix. Figure C.1 illustrates the configuration of the instruments for the performance tests, while the instruments are identified in Table C.1. The analog memory was mounted on a custom printed circuit board together with most of the functional blocks needed to operate the circuit. Only low-speed digital input and output ports are required to control the circuit and to read out the measured data. The board can thus be operated at experiment sites without an elaborate high-speed data acquisition system.

For the performance tests reported in Chapter 6, the board was connected to optically isolated digital input and output modules that were placed in a CAMAC [66] acquisition system crate. The test board was mounted in a shielded aluminum box and the power and control signals were transmitted on shielded coax and flat cables so as to minimize noise pickup. The analog input waveforms were generated with a sine-wave signal source, a pulse generator, and a CAMAC D/A converter module, as indicated in Figure C.1. The output of the sine-wave generator was filtered with a passive band-pass filter to attenuate input signal distortion. The unregulated supply voltages for the board, ± 15 V and +8 V, were provided by a triple linear dc power supply, as specified in Table C.1. The measurement system was controlled by a UNIX workstation via an SBUS-GPIB interface; the software used for control and data processing was written in C. The sine-wave fitting program was implemented in the MATLAB [67] matrix data processing environment.

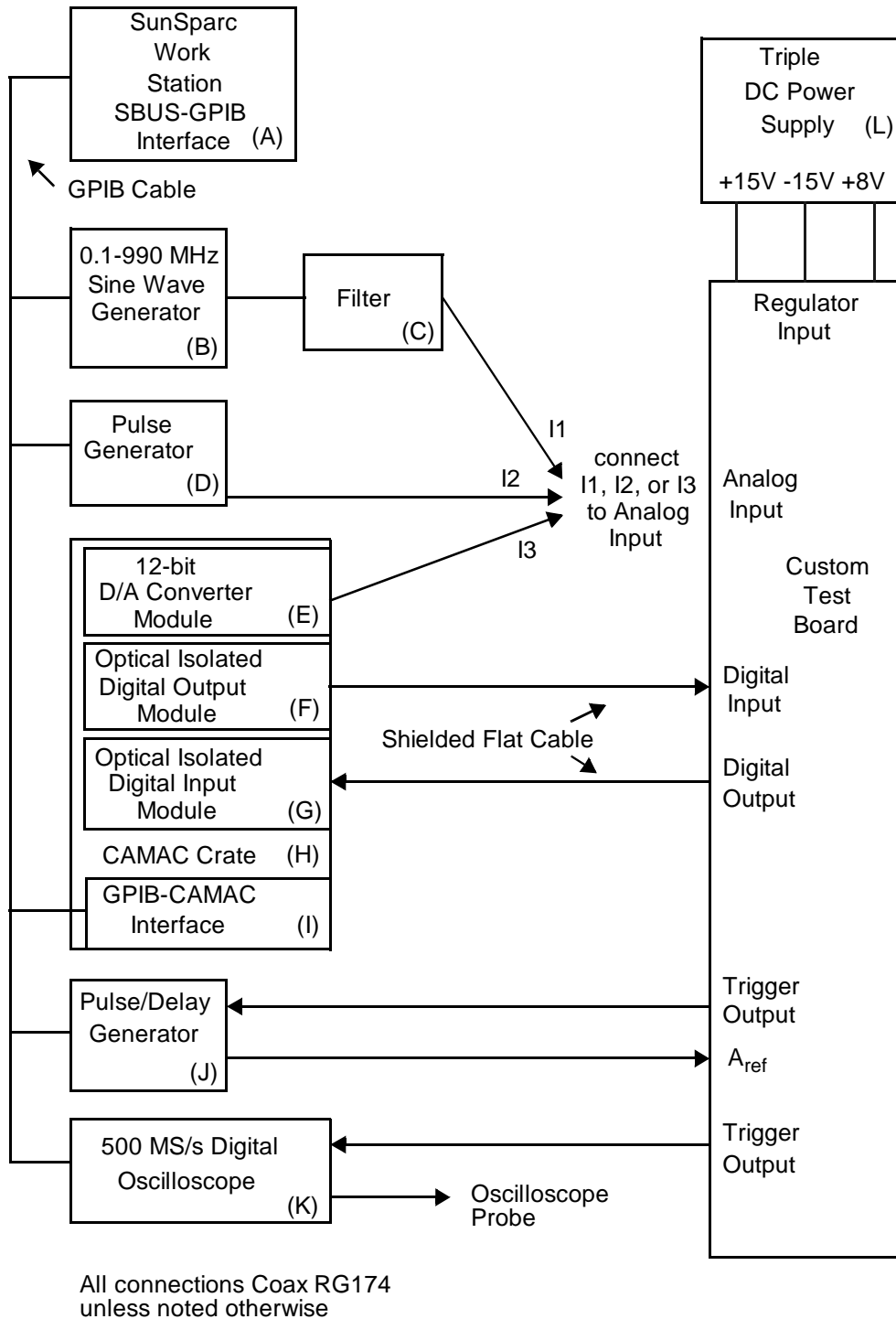


Figure C.1: Experimental setup.

- A: National Instruments GPIB-SPRC-B Interface
- B: Hewlett-Packard 8656B 0.1-990 MHz Generator
- C: TTE Passive Electrical Bandpass Filters (Los Angeles)
- D: Stanford Research Systems DG535 Pulse Generator
- E: Joerger 8 Channel CAMAC D/A Converter Module
- F: BiRa IDOM 48 Channel CAMAC Output Module
- G: BiRa IDIM 48 Channel CAMAC Input Module
- H: Kinectic Systems Model 1525 CAMAC System
- I: LeCroy 8901A CAMAC Controller
- J: Stanford Research Systems DG535 Pulse Generator
- K: Hewlett-Packard 2440 500Ms/S Digital Oscilloscope
- L: Power Design TP340 Linear Triple Power Supply

Table C.1: Test setup equipment list.

The schematic for the custom test board was entered on a workstation using VIEW-LOGIC [68] schematic capture design software, and the board was laid out using the PADS [69] layout editor. A GERBER [70] file representing the layout was then created, and the board was fabricated by a commercial board manufacturing company. The four-layer board measures 15 cm x 25 cm and consists of two signal layers, one power plane, and one split layer for analog and digital ground.

A block diagram of the test board is shown in Figure C.2. Initially, the board is reset and the dc reference and bias voltages on the board (reference voltage section) are set from the workstation via the timing and control section. A waveform acquisition cycle proceeds as follows. The timing and control section receives a START signal from the workstation and generates all the logic signals required to control the signal channel and digital memory sections during the analog memory write and read phases. In the signal channel section, the waveforms applied at the analog input of the board are stored in the analog memory and then readout from the memory and digitized. The output data is then stored in the digital memory section. The entire digitized analog waveform is thus stored in the on-board digital memory. The board is subsequently set into the data transmission mode, and the data stored in the digital memory section are transferred, via the digital

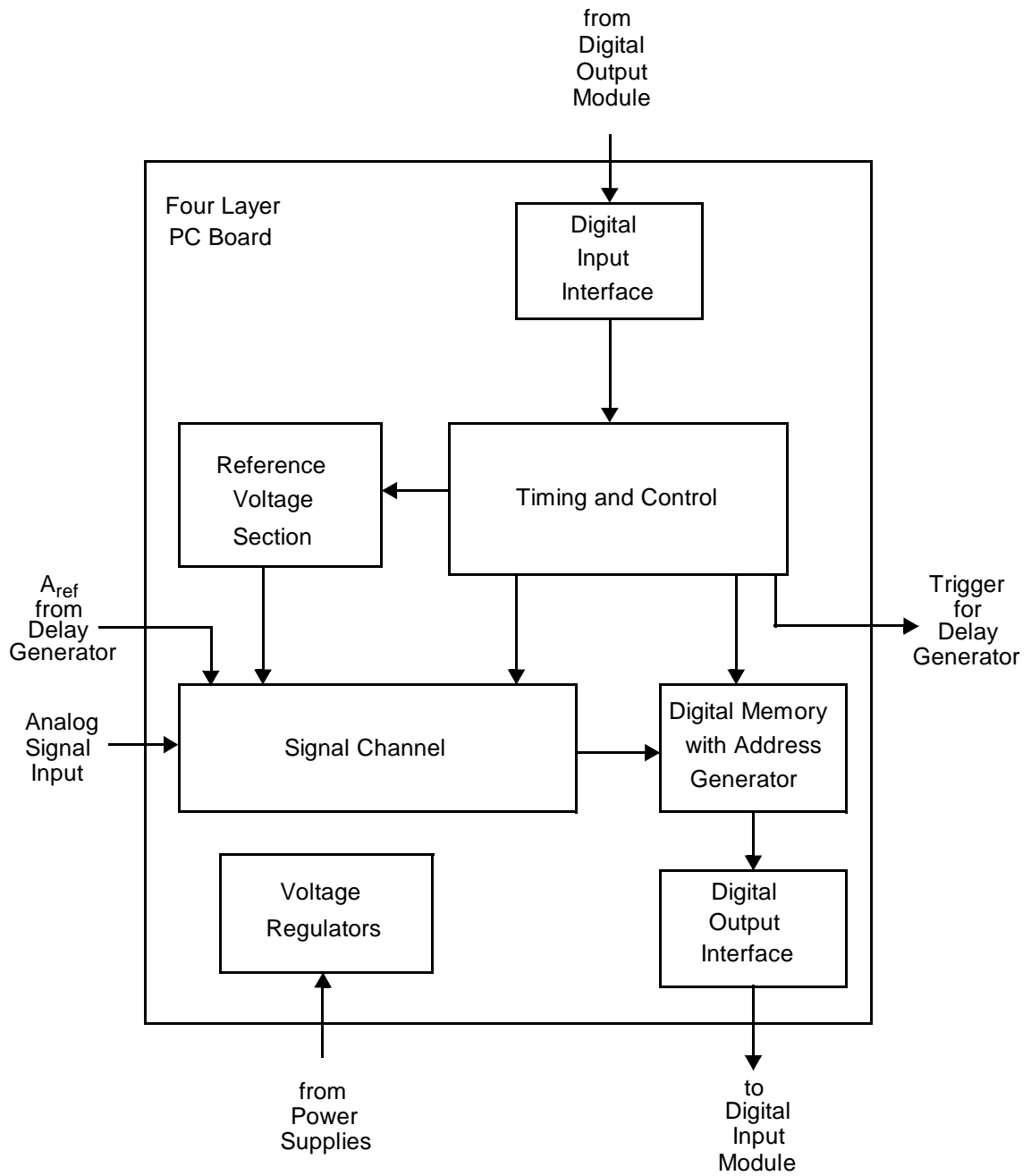


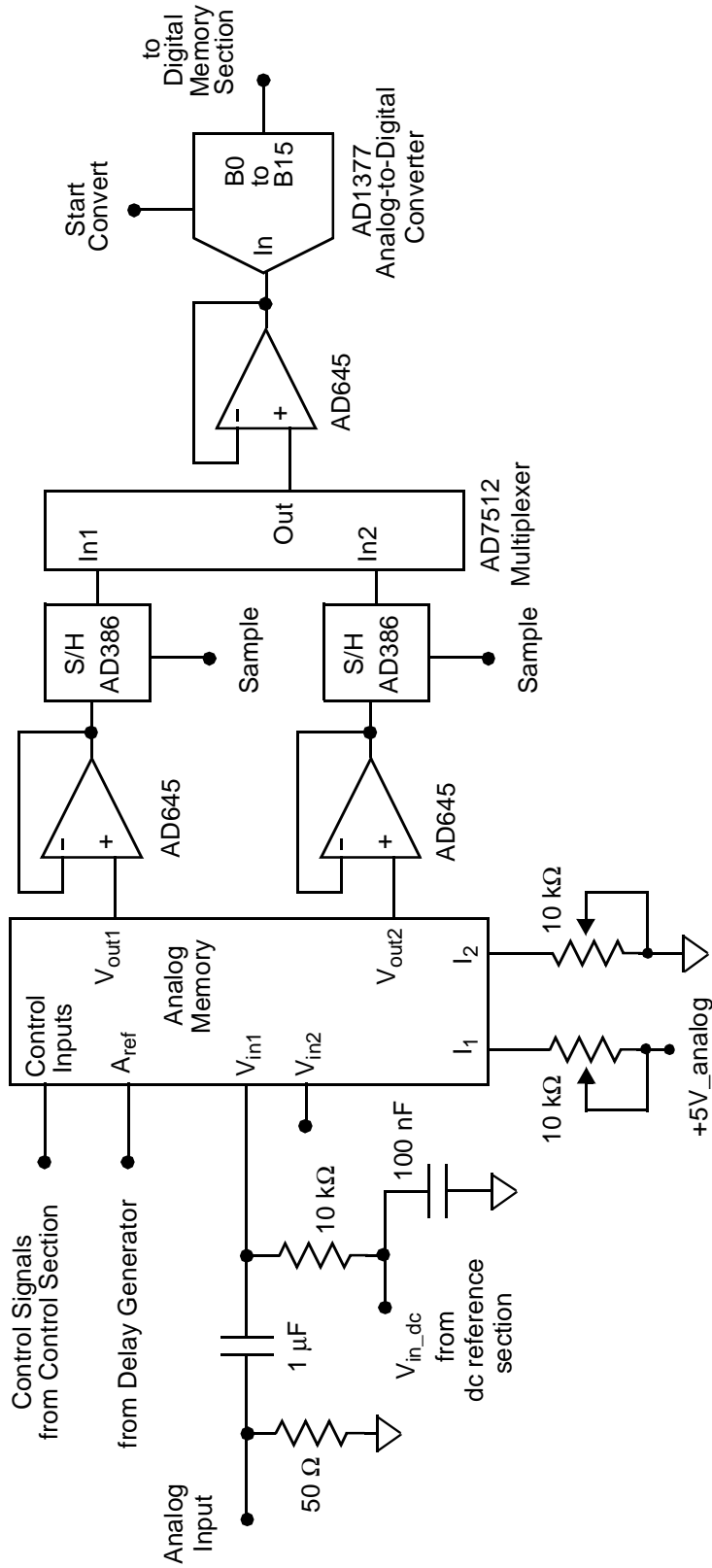
Figure C.2: Block diagram of custom printed circuit board.

CAMAC input module, to the workstation for processing. The digital input and output interface blocks contain connectors along with receiver and driver circuitry, respectively.

Shown in Figure C.3 is the simplified circuit schematic for the signal channel section. The analog signal applied at the input of the test board is ac coupled to the analog memory and a dc voltage, V_{in_dc} , is superimposed via a 10-k Ω resistor. Since this dc voltage can be changed under workstation control, it can be used to generate the dc calibration voltage levels during the calibration phase (see Section 6.3.2). The outputs of the two analog memory channels of the device under test are buffered, sampled, and multiplexed onto the input of a single 16-bit analog-to-digital converter for digitization. Most of the control and timing signals are generated in the control section of the test board. The reference input signal, A_{ref} , used to adjust the sampling rate of the device is generated by a precision pulse delay generator. The magnitudes of the two currents, I_1 and I_2 , in the servo delay feedback circuit (Figure 6.4) are set with potentiometers. The equivalent load capacitance at the output of the analog memory is 3 pF, which accounts for its package capacitance and the input capacitance of the AD 645 amplifier (1 pF).

The digitized data read out from the analog memory is latched in two 8-bit registers and transferred into a static RAM, as shown in Figure C.4. Two counter chips are employed to generate the memory address, which is reset and incremented by the timing and control section of the test board. After the analog information from the analog memory is digitized and stored in the digital memory, the data is transferred to the workstation for processing via the digital CAMAC input module. The registers used to latch the converter output bits must be tri-stated while the data is transferred, since the memory data bus is bidirectional.

Shown in Figure C.5 are the main components of the timing and control block, a programmable array logic device (PAL), a programmable micro sequencer, a latch, and a 32-MHz clock generator. The latch is used to synchronize the START signal from the CAMAC output module for the sequencer. After a START signal is received, the sequencer steps through the programmed logic states and provides the timing and control signals for the board. One of the sixteen control output signals of the sequencer is used to trigger an external delay generator that provides the reference pulse A_{ref} , as shown in Figure C.1. The PAL is employed to decode control signals from the output module used



Note: Power and ground connection and bypassing not shown.

Figure C.3: Signal channel section.

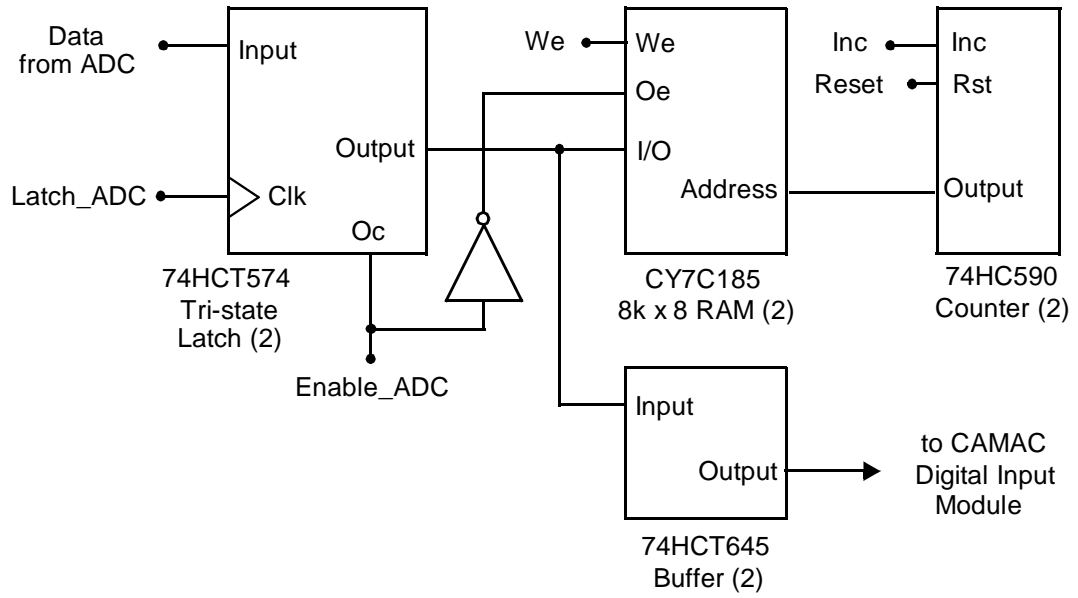


Figure C.4: Digital memory section.

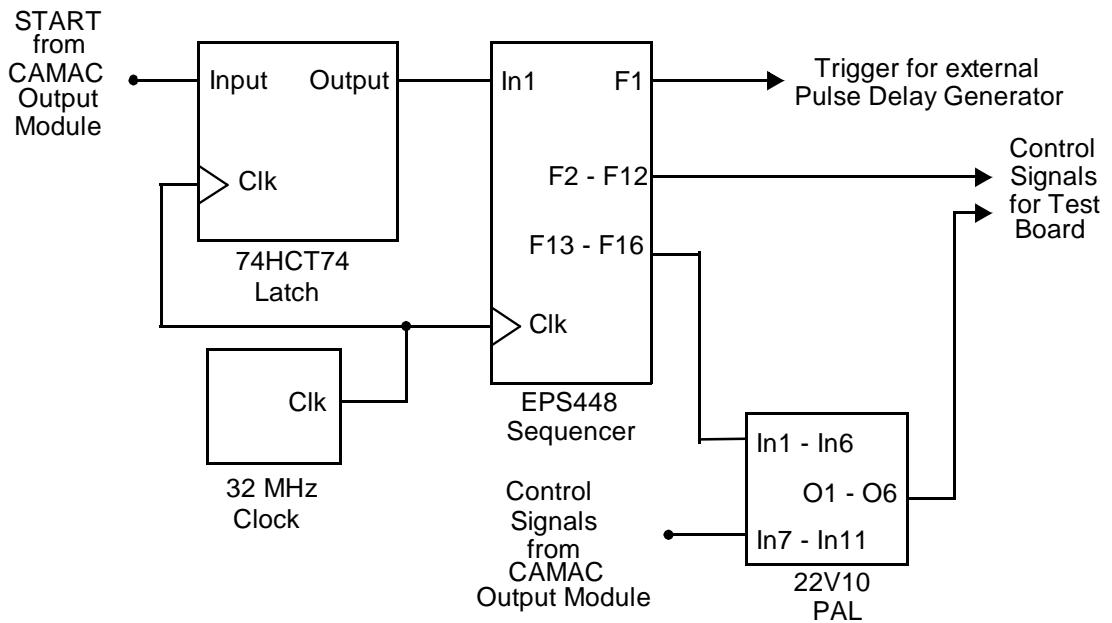
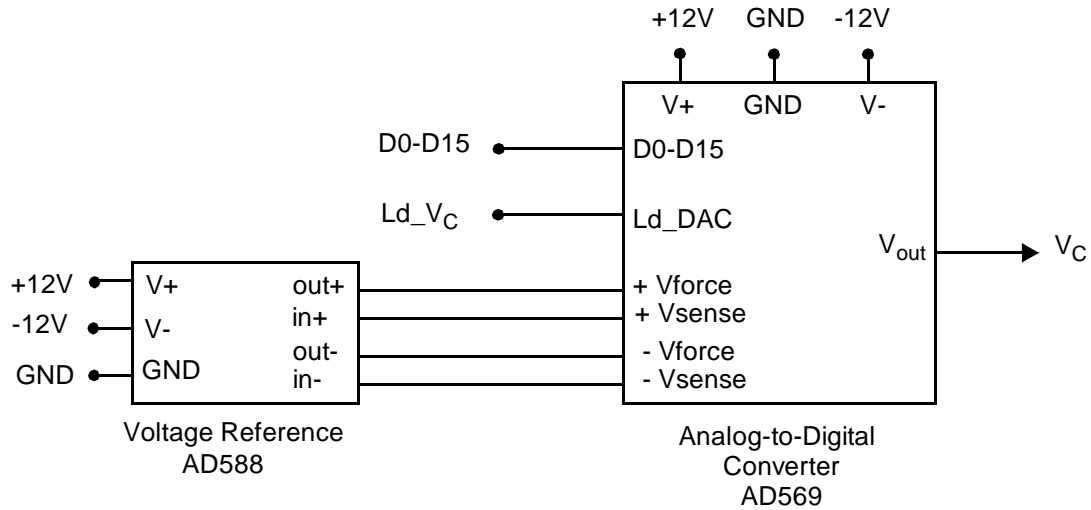


Figure C.5: Timing and control circuit.



Note: +/- 12 V bypassed with 10 μ F and 0.1 μ F capacitors.

Figure C.6: Digital-to-analog conversion circuit.

to select and load the digital-to-analog converters in the dc reference section. The TTL output levels of the sequencer and of the PAL are translated to CMOS logic levels by means of 74ACT04 inverter components (not shown). The codes for the PAL and the programmable sequencer devices were written using ABEL [71] and ALTERA [72] design software, and the components were programmed by means of a DATA I/O [73] programming system.

The dc reference voltages for the analog memory circuit, the input reference voltage V_C , the input offset voltage V_{in_dc} , and the amplifier common-mode voltage V_B are generated by three on-board digital-to-analog converters. Figure C.6 illustrates the circuit that generates voltage V_C . The digital 16-bit input data word, D0 to D15, from the CAMAC output module is connected to all the converters and is loaded by applying the appropriate DAC load control signal (e.g. Ld_V_C).

The supply voltages for the circuits on the board, ± 12 , +5 V_{analog} , and +5 $V_{digital}$ are regulated with four commercial regulators. The circuit that regulates the +12 V voltage from the externally supplied +15 V is shown in Figure C.7. The input and output of the regulator are filtered by means of an inductor and capacitors to reduce noise. The power

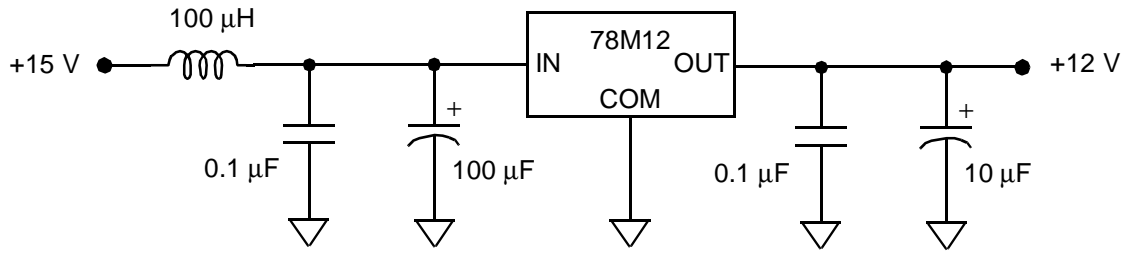


Figure C.7: Voltage regulator circuit.

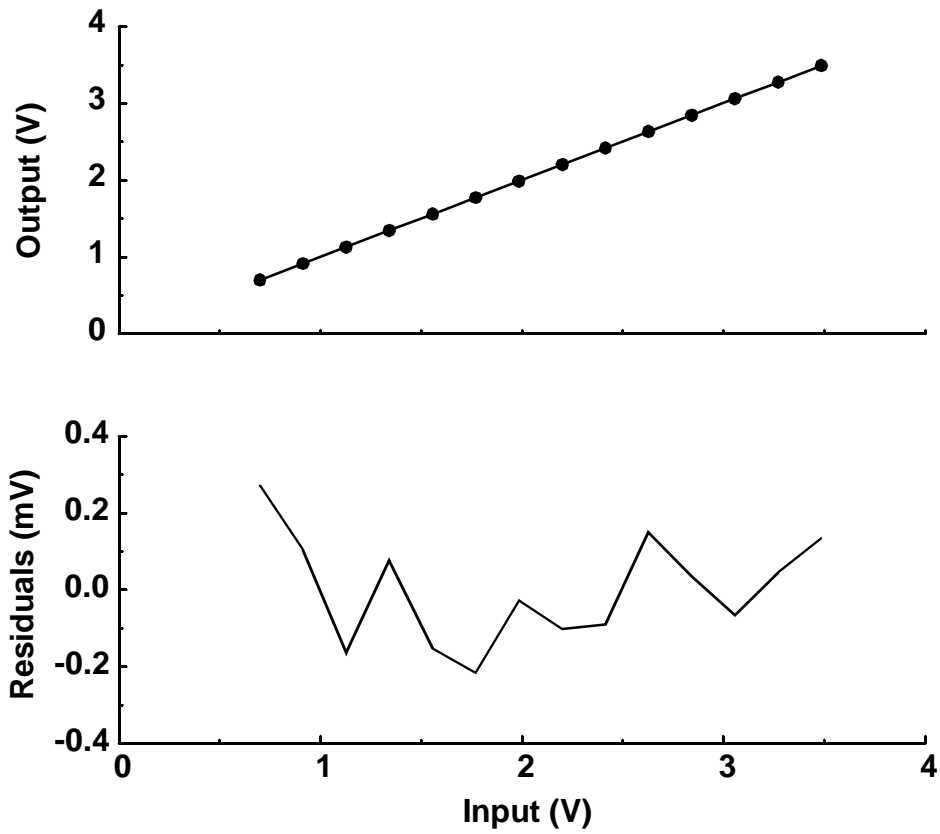


Figure C.8: Upper: Output voltage plotted as a function of input voltage. Lower: Deviations from a linear fit.

for the analog and digital components are separate, as is the ground, to minimize feed-through from the digital signals to the analog circuits. The grounds are tied together at the analog-to-digital converter in the signal channel section.

The rms noise and linearity of the test setup was measured with the analog memory circuit, shown in Figure C.3, removed. The input V_{in1} was shorted to the output V_{out1} , and repeated measurements were performed with various input dc voltages V_{in_dc} . Figure C.8 illustrates the linearity of the measurement setup. The integral nonlinearity is 0.01% and the measured rms noise is 70 μV .

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