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DESIGN OF BEAM POSITION AND CHARGE MONITORING CIRCUITS FOR THE STANFORD TWO-MILE ACCELERATOR

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I. INTRODUCTION

An important problem in the Stanford two-mile accelerator is to determine accurately the transverse position of the electron beam within the accelerating structure. Ideally, the electron beam can be collimated to have a diameter of a few millimeters, while its maximum transverse displacement is limited by the waveguide disc aperture to about $\pm$ 10 millimeters. Optimum transmission is assured when the beam is centered in the waveguide, coincident with the maximum of the rf field.

Generally speaking, a short linear accelerator can be sufficiently well aligned that steering is required only during injection of the beam into the accelerating structure. Beyond this point, the transverse forces due to stray electric and magnetic fields can be sufficiently reduced using conventional shielding techniques that their effect on the beam is negligible.

In a machine two miles long, however, not only is the physical alignment problem severe, but stray fields, including the earth's magnetic field, can cause significant misalignment of the beam. As a result, even though elaborate shielding, degaussing, and alignment techniques are employed, a system for monitoring and steering the beam is considered essential.

A second aspect of beam monitoring is to accurately measure the charge on a pulse-to-pulse basis. The measurement should be accurate enough to detect small losses in charge along the length of the accelerator, of the order of 1% or less.

The basic sensing devices in use are a microwave position monitor and a ferrite toroidal current monitor. Both devices produce video outputs of the same duration as the electron beam. To transmit these signals directly to the

Central Control Room (CCR) from a large number of points along the machine would be extremely difficult and costly. The alternative taken has been to develop a system in which the video pulses are processed locally into a form suitable for transmission to the CCR.

A. Basic Requirements

Three main difficulties must be surmounted in the design of the position monitoring electronics. First, the system must operate reliably over at least a 60-dB dynamic range. This is because the beam consists of a 360-pps pulse train, in which two consecutive pulses can vary in amplitude between 1 and 100 mA, and in duration between 0.2 and 2 μsec. Hence, because the circuit determines the position of the center of charge of the beam using an integrating technique, the range is seen from the charge per pulse to be 1000:1 or 60 dB.

The second difficulty concerns the fact that in the multiple beam mode of operation, as many as six interlaced beams may be present at repetition rates between 1 pps and 360 pps. This requires that the electronics process each pulse independently; and further, that a maximum-charge pulse followed by a minimum-charge pulse will cause no cross-talk from the first to the second interval.

Thirdly, since the entire accelerating portion of the machine is operated from a single Central Control Room (CCR), the position information must be derived in a form suitable for telemetering, on a baseband system, over distances up to two miles.

The position monitoring electronics to be described accepts the video outputs from a microwave position monitor, and derives outputs proportional to

$\bar{x}$ and $\bar{y}$ displacement, where $\bar{x}$ and $\bar{y}$ are average displacements referred to an origin at the waveguide central axis. At the same time, a signal proportional to the logarithm of charge ($\ell n\ Q$) is obtained. The utility of the $\ell n\ Q$ signal is that consecutive beams of widely differing charge can be displayed on the same scale. On the other hand, the signal inherently is not a particularly accurate measure of charge.

To measure the charge more accurately than can be done using the microwave sensor, a ferrite toroid is used as the basic detector. The output, which illustrates the time-profile of beam current, is integrated to 1% accuracy on a pulse-to-pulse basis; the resulting signal is then transmitted to the CCR via an FM hardwire telemetry link. The FM system short-term drifts are much less than 1% over a restricted dynamic range. In order to operate at all times within this range, it is necessary to provide remote gain switching at each sector to cover the basic 60-dB range of charge. The main design difficulties with this portion of the electronics are (1) to obtain a wide dynamic range and very low noise in a relatively high-noise environment, and (2) to minimize cross-talk from one pulse interval to the next when, for high gain settings, the amplifier may be overdriven by 1000 times in the first interval.

B. Beam Monitoring System

Figure 1 is a block diagram of the main components located in a drift section, and their interconnection to the display and controls at the CCR. There are 30 such drift sections, spaced at 333-foot intervals along the accelerator. The system operates as follows: Upon passage of a beam pulse, the three microwave cavities produce rf pulses proportional to beam intensity i(t), intensity times horizontal displacement ix(t), and intensity times vertical

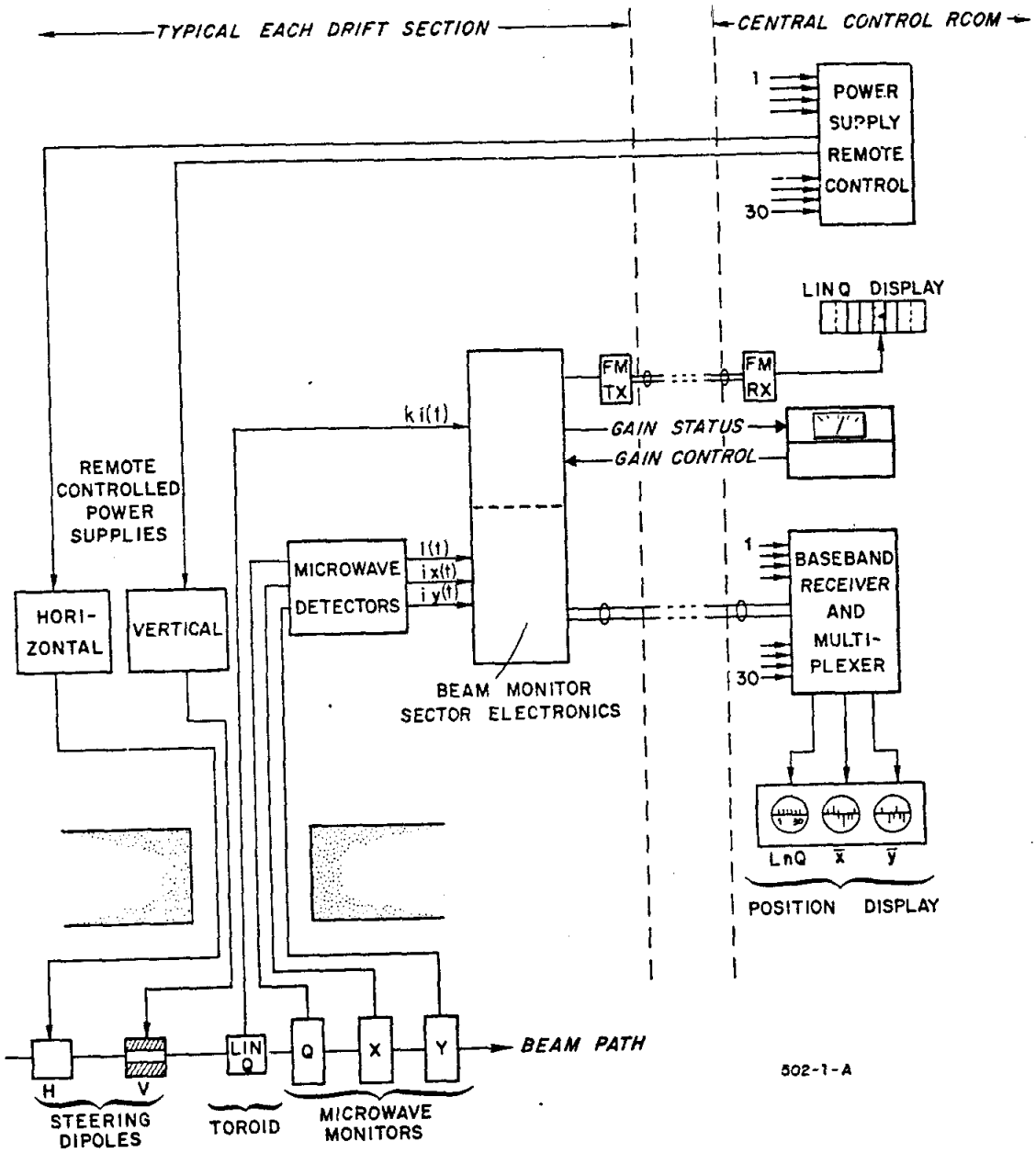


FIG. 1- BEAM STEERING SYSTEM

displacement iy(t). The current-proportional signal, i(t), is used as a reference in a microwave mixer. The ix(t) and iy(t) rf signals exhibit a phase reversal at the geometric center of the cavity; hence the phase-sensitive detector produces bipolar video outputs proportional to positive or negative values of displacement. These outputs are, of course, proportional to beam intensity as well.

The video outputs are processed in the position monitoring electronics to yield $\ell n\, Q$, $\bar{x}$, and $\bar{y}$ in serial form, where Q is the total pulse charge, and $\bar{x}$ and $\bar{y}$ are average displacements. This serial output is sent by a baseband telemetry system to a multiplexer at the CCR, together with similar signals from the other drift sections.

The multiplexer first samples each of the 30 $\ell n\, Q$ signals, then $\bar{x}$, and finally $\bar{y}$; each group of signals is channeled into a separate oscilloscope. To display multiple-beam information, each oscilloscope has six separate traces. Beam pattern signals are provided to route each set of multiplexer outputs to the appropriate trace of each display.

Thus, the CCR operator has before him a profile of the logarithm of beam intensity, horizontal position $\bar{x}$, and vertical position $\bar{y}$, for the entire machine. In close proximity are the controls for the steering dipole power supplies located at each sector. By adjusting currents in the horizontal and vertical steering dipoles of a particular sector, the beam can be deflected left or right, up or down, in the following sectors. The operator adjusts the steering so as to minimize the position outputs of each monitor, which should simultaneously maximize the amount of beam current through the machine.

Passage of the beam pulse also induces at the output of the toroidal current monitor a voltage proportional to i(t). This signal is integrated,

transmitted to CCR via the FM telementry link, sampled, and displayed in a row of 30 slide-back dc voltmeters. The gain of the system is controlled from the CCR; the gain setting is indicated on a separate meter. All units are set to have the same gain so that the slide-back display gives a direct sector-to-sector comparison of the average current or charge.

For multiple beam operation, it is necessary to multiplex the meter display using pattern identification information, in order to read the charge in any one beam. At the present time this multiplexing is not done; hence the gain must be set to accommodate the largest beam and, if every pulse is sampled, the meters will indicate the average beam charge at each sector.

Before discussing the detailed operation of the electronics unit, the fundamentals of the microwave and video sensors will be briefly described.

C. Microwave Position Monitors

The following is a condensation of a detailed description of the microwave position monitors given by Brunet et al.[1] The basic sensor is a TM_{120} cavity, which has the field, power, and phase distributions shown in Fig. 2.

For the case of interest, i.e., a short filling time, maximum efficiency, and $Q_L << Q_o$, the cavity losses are negligible and

$$P_{out} \approx P_b = \frac{4}{\pi} Q_L \sin^2 \theta \frac{b}{a} \frac{\lambda_g}{\lambda_o} \eta I_o^2 \qquad (1)$$

where P_{out} is the output power,

P_b is the power coupled from the beam,

Q_L is the loaded Q,

Q_o is the unloaded Q,

a, b are cavity dimensions,

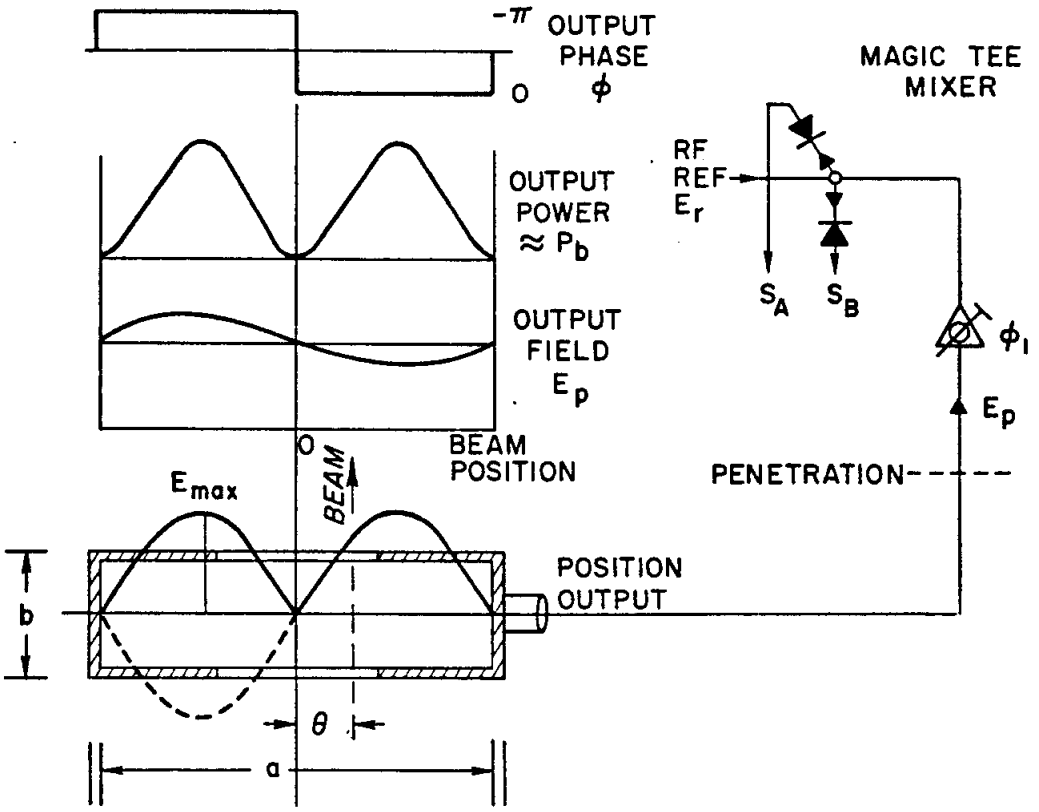


FIG. 2-TM 120 CAVITY MONITOR[1]

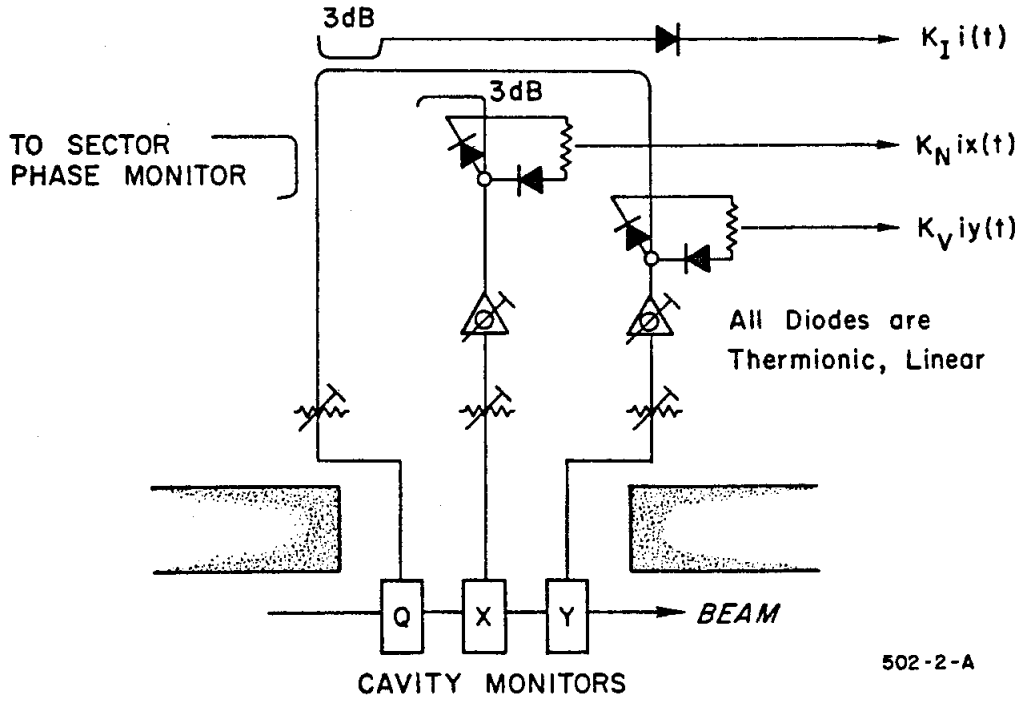


FIG. 3- MICROWAVE MONITOR SYSTEM[1]

λ_g, λ_o are the guide and free space wavelengths,

η is the free-space impedance, and

I_o is the beam current.

It is apparent that for beam displacements of much less than a wavelength, sin θ is linearly related to the position. Also, note that the phase of P_{out} reverses as the beam crosses the center of the guide. Hence, by supplying a fixed-phase reference signal E_r to one input arm (A) of a magic-tee mixer, and $E_p \propto \sqrt{P_{out}}$ to the other arm (B), one obtains rf outputs of

$$E_A^2 = 1/2\ (E_r^2 + E_p^2 + 2E_rE_p \cos \phi) \tag{2}$$

$$E_B^2 = 1/2\ (E_r^2 + E_p^2 - 2E_rE_p \cos \phi) \tag{3}$$

The phase shifter ϕ_1 is adjusted to make $\phi = 0^o$ for the positive direction of displacement; hence

$$kE_A = \frac{k}{\sqrt{2}}\ (E_r + E_p) \quad \text{and} \quad kE_B = \frac{k}{\sqrt{2}}\ (E_r - E_p)$$

are the linear detector outputs. The output difference is

$$S_A - S_B = k\ (E_A - E_B) = \sqrt{2}\ kE_p \quad \text{for } 0^o \tag{4}$$

and

$$S_A - S_B = -\sqrt{2}\ kE_p \quad \text{for } 180^o\ . \tag{5}$$

(Actually, one reversed diode is used and the outputs are summed.)

Further, since $E_p \propto \sqrt{P_{out}}$, and $\theta = \frac{2\pi x}{\lambda_g}$ for the horizontal case, then from Eq. (1)

$$E_p = \sqrt{K}\ I_o \sin \frac{2\pi x}{\lambda_g} \approx \frac{2\pi}{\lambda_g} \sqrt{K}\ I_o x \tag{6}$$

for small values of x.

Thus the diode output difference indicates both the amplitude and direction of the displacement. Note also the linear dependence on I_o; the purpose of the subsequent electronics is to remove this dependence to obtain signals which are functions of position only.

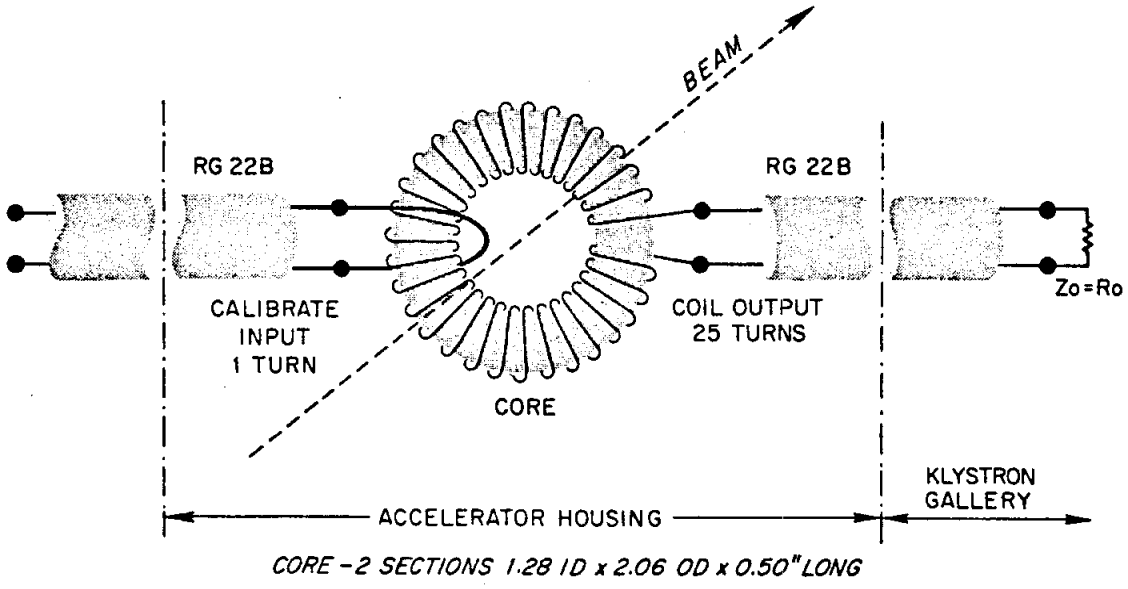
The complete microwave system at each drift section is shown in Fig. 3. The reference signal is obtained from a separate cavity which was designed as a sector phase monitor.[2,3] The signals from all three cavities are transmitted on coaxial cables from the underground Accelerator Housing to the Klystron Gallery above, a total cable run of about 50 feet. The mixers are in a separate chassis known as the Beam Position Monitor RF Detector.

The position monitor rf outputs are drift-free in the sense that a zero output is obtained for zero displacement from the cavity center. However, because the rf reference signal biases the diodes into a linear region and the position signals cause small variations about the operating point, the diodes must be matched and stable over a wide range of beam currents, or erroneous position indications will result. This is in practice the chief limitation to resolution in the microwave system.

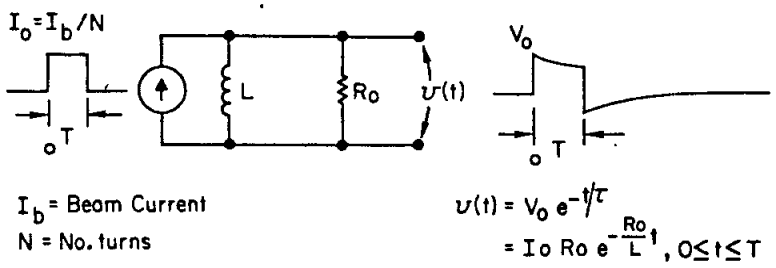
D. Toroidal Current Monitor

The toroidal current monitor is a simple ferrite-core current transformer as shown in Fig. 4a. The main winding consists of 25 turns of bare copper wire; a separate one-turn winding is provided for use in calibrating the system.

Passage of a beam pulse induces a signal which is proportional to the beam current i(t). The practical equivalent circuit is shown in Fig. 4b. The signal is transmitted to the Klystron Gallery on a twinaxial 95-ohm line, terminated in its characteristic impedance. Therefore, the toroid sensitivity,



(a) TOROID MONITOR



(b) EQUIVALENT CIRCUIT

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FIGURE 4 — TOROIDAL CURRENT MONITOR

neglecting losses, is

$$S = \frac{V_o}{I_o} = \frac{1}{N} R_o = \frac{95}{25} = 3.8 \text{ mV/mA}$$

Differences in the efficiency of the magnetic coupling and line-loss will cause this value to vary slightly in different units.

The time response to a square pulse of beam current, shown in Fig. 4b, is seen to have a droop given by

$$v(t) = V_o e^{-t/\tau}$$

where

$\tau = L/R_o$

L = inductance of the toroid

R_o = terminating resistance

For the particular core material used, Ferroxcube C2, the inductance lies in the region of 1 - 2 mH. For L = 1 mH, the droop on a 2-μsec beam pulse is approximately 20%. The output coupling transformer at the end of the balanced line causes another 2% - 3% droop. Obviously, for accurate integration, droop compensation must be provided. This is performed in the video preamplifier.

An additional problem is that the permeability μ of the core material changes with temperature. Hence, for high accuracy, the toroid must remain in a stable thermal environment, or the droop compensation will become uncalibrated. Thermal stability of the inductance of the sensor is entrusted to the fact that the drift section is mechanically coupled to waveguide sections which are temperature-controlled by a water cooling system.

The undesirable aspect of droop compensation is that each preamplifier must be matched to a particular toroid. Also, because the droop is large, the compensation is more difficult. The alternative is to increase L with more turns ($L \propto N^2$), but this costs in sensitivity, since $S \propto \frac{1}{N}$. It appears that the value of $N = 25$ is near the optimum. The most significant improvement would result if a much higher permeability core material could be used; however, because the material must be highly radiation-resistant, the choices are very limited.

II. POSITION MONITORING CIRCUITS

A. Functional Description[4]

The operation of the position monitoring circuits is as follows (see Fig. 5): At the beginning of the 360-pps machine interval, which we shall call t_o, a trigger pulse from a sector trigger generator (STG) initiates a timing cycle within the block called "ℓnQ, x and y timing." This trigger pulse precedes the accelerator beam pulse by a fixed interval of approximately 2.0 μsec.

The timing circuits produce outputs which serve three basic functions: (1) The outputs operate gates, which open to allow the Q, x and y input pulses to charge integrating capacitors, and then close to isolate the charge there; (2) they gate the integrated x and y signals, as well as a switched gain amplifier, in order to obtain a final output in serial form; and (3) they actuate clamps which restore all integrating, sampling, and coupling capacitors before the arrival of the next beam pulse at t_o + 2.78 μsec. The outputs are depicted as G_1, a delayed 2.5-μsec gate pulse; G_x and G_y, 550-μsec x and y serial gates; and C_1 and C_2, 300-μsec clamp pulses.

The circuit operation is as follows: First, the delayed gate G_1 simultaneously opens each of three integrators in coincidence with the arrival of the beam pulse. The integrators are passive RC circuits having a nominal linearity of 5% for the widest pulse. After the gates close, charges are isolated on the three capacitors which are proportional to $\int_0^T i(t)dt$, $\int_0^T (ix)(t)\,dt$ and $\int_0^T (iy)(t)\,dt$. These signals are proportional to Q, $Q\bar{x}$, $Q\bar{y}$, respectively.

The output of the Q integrator is direct-coupled to a logarithmic amplifier, the output of which rises to a value given by CℓnQ. The voltages proportional

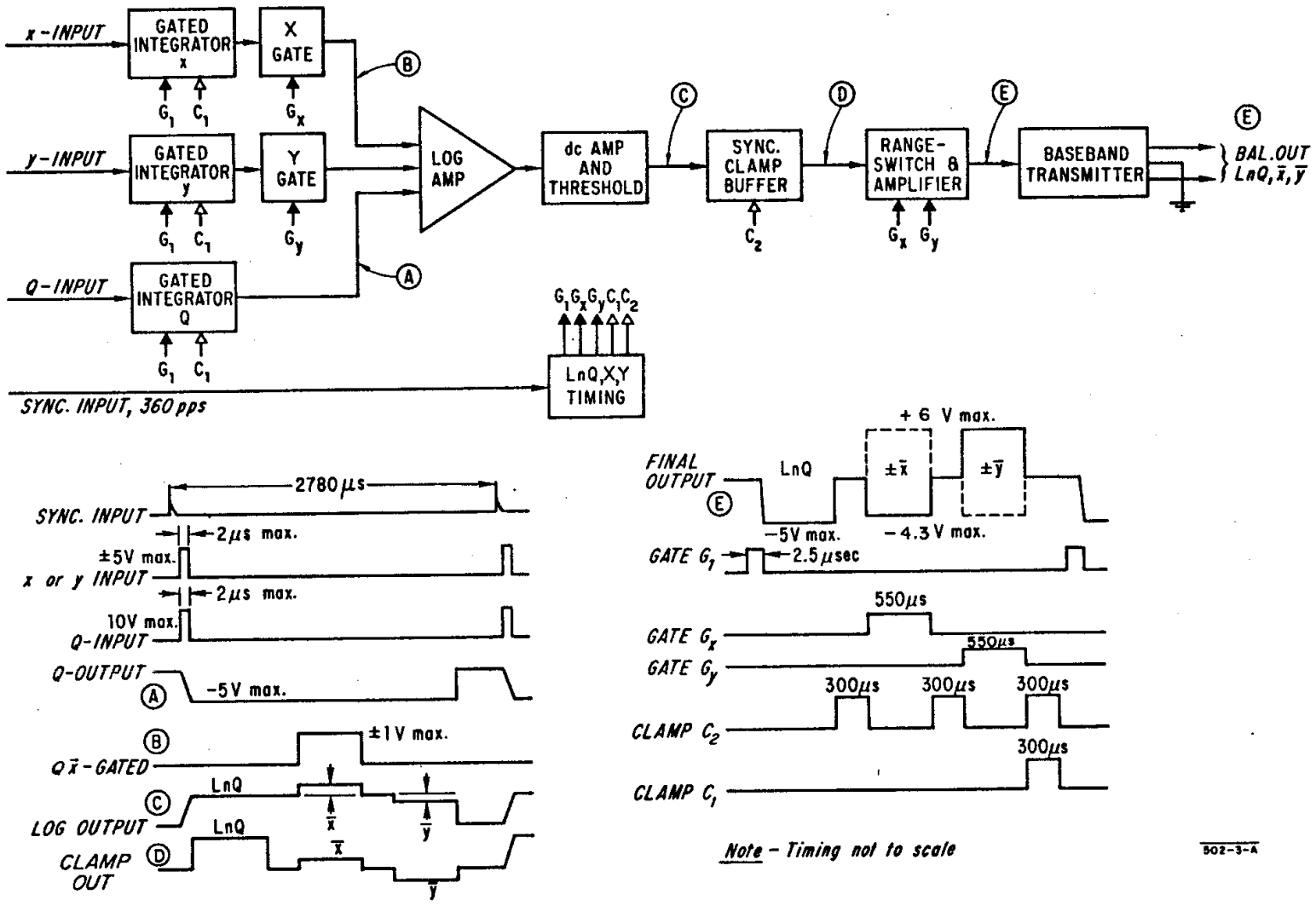


FIG. 5 — SYSTEM BLOCK DIAGRAM

to $Q\bar{x}$ and $Q\bar{y}$ are connected through gates and summing resistors to the amplifier input. At a time $t_o + 850\ \mu sec$, $Q\bar{x}$ is gated in for 550 μsec. During this time the amplifier output rises to $C\ell n(Q + Q\bar{x})$. At $t_o + 1400\ \mu sec$ the x-gate closes and the output drops back to $C\ell nQ$. At $t_o + 1700\ \mu sec$, $Q\bar{y}$ is gated in, and the amplifier output settles at a new level given by $C\ell n(Q + Q\bar{y})$. At $t_o + 2250\ \mu sec$, clamps are actuated to erase the charge contained in the integrating capacitors, and the amplifier output drops to zero.

A position signal is derived from the logarithmic waveform, using the following approximations:

$$\ell n(Q \pm Q\bar{x}) - \ell nQ = \ell n(1 \pm \bar{x}) \approx \pm \bar{x}, \text{ and}$$

$$\ell n(Q \pm Q\bar{y}) - \ell nQ = \ell n(1 \pm \bar{y}) \approx \pm \bar{y},$$

$$\text{where } \bar{x},\ \bar{y} \ll 1.$$

Thus, if $Q\bar{x}$ and $Q\bar{y}$ are constrained to be small excursions about the value of Q, the output of the logarithmic amplifier essentially yields ℓnQ, $\bar{x}$ and $\bar{y}$.

Following the logarithmic amplifier is a synchronous clamp which performs the following sequence of operations: It passes ℓnQ for 550 μsec, then clamps the ℓnQ level to ground; passes $\bar{x}$ for 550 μsec, reclamps to ground; passes $\bar{y}$ for 550 μsec, and again clamps to ground. The resultant output is ℓnQ, $\bar{x}$ and $\bar{y}$ in serial form, where the $\bar{x}$ and $\bar{y}$ outputs are very small compared with ℓnQ. Next, a gated attenuator equalizes all three pulses to approximately the same level, after which the pulses are amplified to make ℓnQ for I = 100 mA, 2 μsec (Q = 200 nC) equal to 5 volts maximum. Because of the logarithmic approximation, the position outputs are larger than ℓnQ in the positive direction, and smaller in the negative direction, for equal

amplitude input pulses (ℓnQ is negative at the output of the final amplifier). This point is discussed in detail in Section II. B.

The final output is buffered in a unity-gain baseband transmitter, which drives a transformer-coupled, 600-ohm standard telephone line. With this arrangement, either polarity of output at the receiving end can be achieved simply by reversing the transformer leads.

B. Circuit Design Details

The discussion of design details will concentrate on those circuits which are somewhat unique, or where the limitations of certain devices or components are important. In the case of straightforward circuits, such as the timing circuits, the general operation only will be discussed.

1. Gated Integrator and Buffer

a. Operation. The complete circuit diagram for the gated integrator and buffer for X and Y signals is shown in Fig. 6a. The Q integrator differs mainly by the addition of a $\times 5$ amplifier, as shown in Fig. 6b.

The circuit operation of Fig. 6a is straightforward: Transistor Q1 is opened for 2.5 μsec to admit i_x or i_y; the signal charges the capacitor while Q1 is on. Q3 is a high-input-impedance, field-effect transistor (FET) which draws no appreciable charge from the capacitor. Q3, Q4, and Q5 form a $\times 1$ buffer, the output of which is ac-coupled to a resistive load at the input to the logarithmic amplifier. The load is shown as a fixed resistor to a virtual ground point.

As C_1 charges, the buffer output, and hence V_o, follows the input. As the charge on C_1 is held, current flows from C_2 into the resistive load, and V_o begins to decay to zero. Hence, to obtain a flat top on the output pulse,

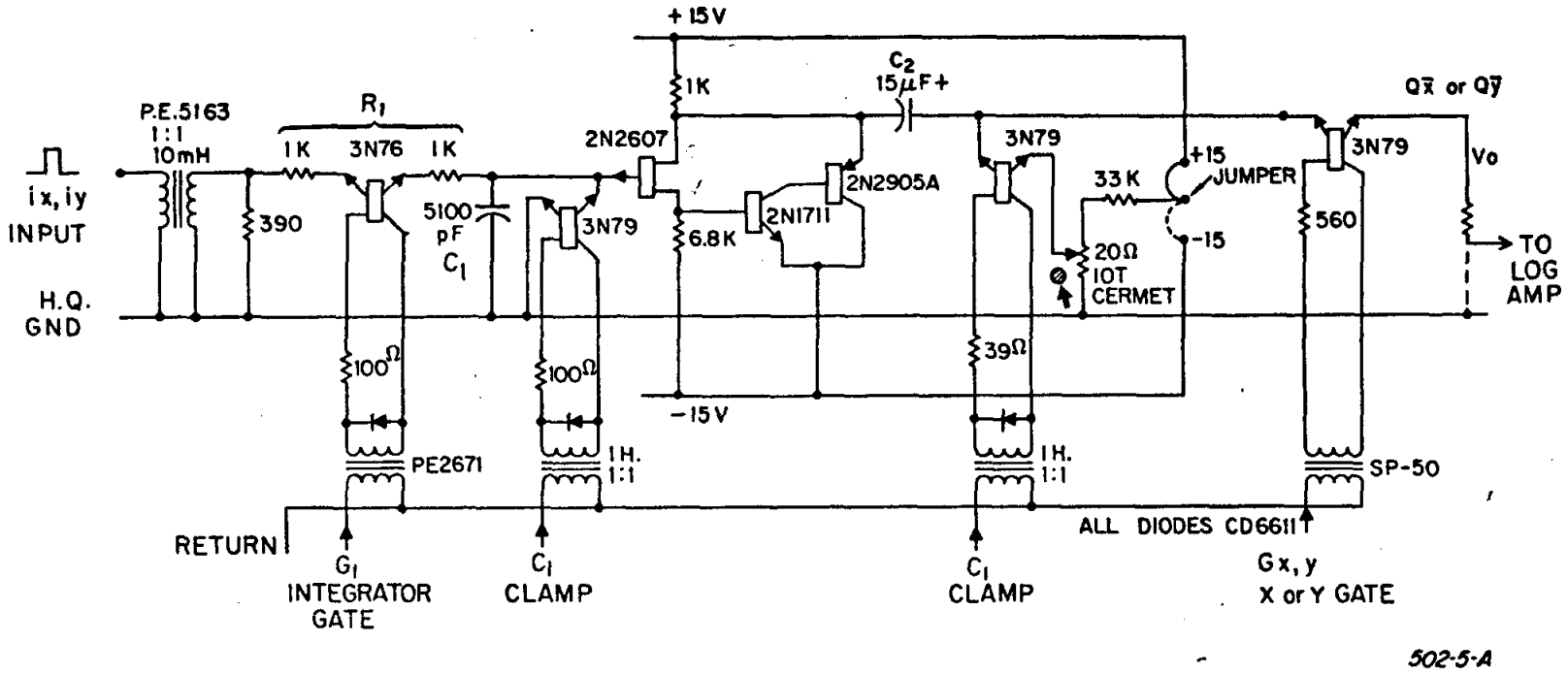


FIGURE 6 (a) — GATED INTEGRATOR AND BUFFER (X AND Y).

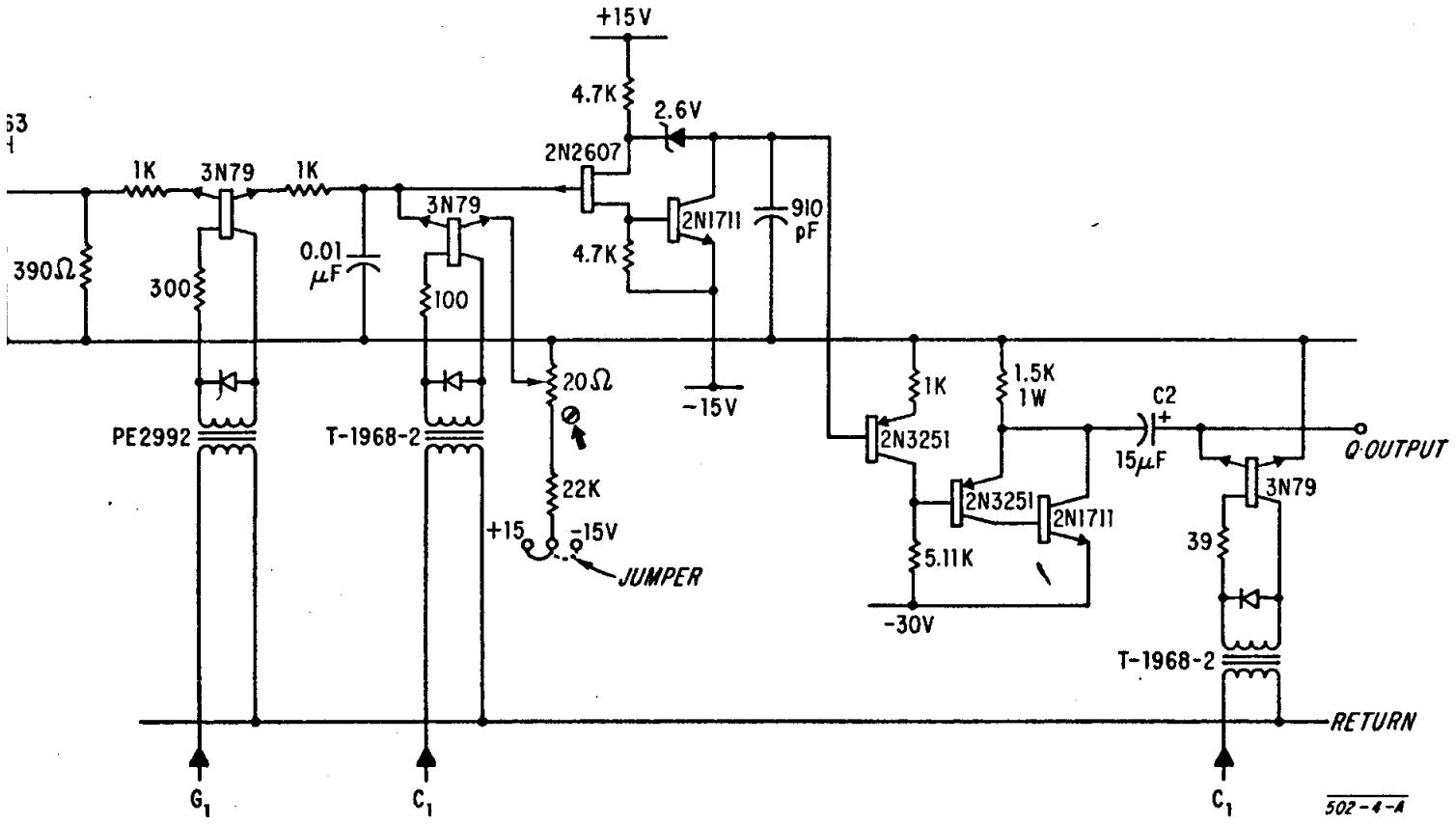


FIG. 6(b)-GATED INTEGRATOR AND BUFFER (Q)

the time constant $C_2 R_2$ must be chosen long compared with the hold period of 2.25 msec. At the end of the hold period, Q2 and Q6 are actuated to restore C_1 and C_2 respectively to their initial conditions, i.e., zero volts on C_1, and a negative voltage V_{gs} on C_2. The input, output and gating waveforms are illustrated in Fig. 5.

b. Design Criteria. Two main compromises must be made in the design of this circuit. First, the gate and clamp transistors, Q1, Q2, and Q6, exhibit small voltage offsets which are in general of the order of 1 mV or less and which vary from unit to unit. Hence, for the required dynamic range of 60 dB, it is necessary to develop at least 1 volt on the integrating capacitor for the maximum input signal. At the same time, the RC must be selected to give a particular integration accuracy, and therefore a particular input amplitude is required to develop the 1-volt signal. Fortunately, 5- to 10-volt input signals are available from the microwave monitors, which allows direct connection to a 5% or 10% integrator without preamplification.

The integrator values are chosen as follows (see Fig. 6a): For a rectangular input pulse of ±5 volts, 2 μsec, from a zero-impedance source, an integrator output of ± 1 volt is realized using an RC of approximately 5 times the pulse width; i.e., RC = 10 μsec. The accuracy of integration is a nominal 10%.

The value of R_1 is chosen to be large compared with the on-resistance of the series switch Q1, so that the latter has negligible effect in determining the integration accuracy and stability. The values chosen were $R_1 = 2k\,\Omega$, $C_1 = 5100$ pF.

Some additional details and their effect on integration accuracy will be discussed in the next subsection.

The second compromise concerns the choice of the output coupling values C_2 and R_2. The following calculations illustrate this point.

First of all, a particular current must be supplied by the buffer into R_2, to establish the operating point of the logarithmic amplifier. This will be explained more fully in the Section II. B. 2; for now, suffice it to say that the Q buffer must supply 0.5 mA when delivering maximum output, and the X and Y buffers, $\frac{0.5}{3}$ or 0.167 mA. For the 1-volt output of the X and Y buffers, then, R_2 must be chosen as $1/0.167\ (10^{-3}) = 6\ k\Omega$. The nearest 1% value of 6.2 kΩ was used.

Next, consider that the maximum allowable droop due to the RC coupling is about 2% for the 2.25-msec hold period (the reasons for this restriction will become apparent in Section II. B. 2). This dictates $R_2 C_2$ as follows:

$$R_2 C_2 = 50 \times 2.55\ (10^{-3}) = 0.127 \text{ sec}$$

$$\therefore\ C_2 = \frac{0.127}{6.2(10^3)} = 20.5\ \mu F\ .$$

Finally, C_2 must satisfy one more requirement: With the minimum resistance of Q6 being about 3 ohms for a 50-mA drive pulse, it must be possible to restore C_2 within the allocated 300 μsec:

$$C_2\ (\text{max}) \times R_6 = \frac{300 \times 10^{-6}}{7}$$

i.e., in seven time constants, restoration is assured to within 1 part in 1000 of the maximum change in the voltage on C_2. This is a conservative approximation which results in $C_2\ (\text{max}) = 14.3\ \mu F$. The actual value chosen

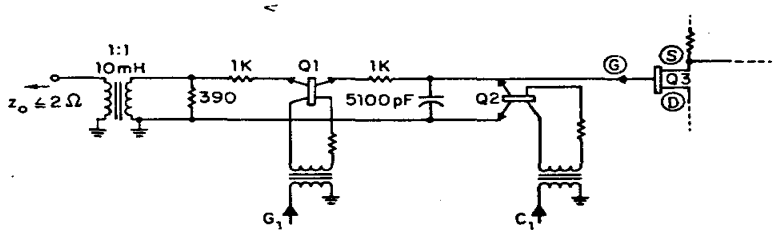
was 15 μF, which results in a droop on the $Q\bar{x}$ and $Q\bar{y}$ outputs of 2.8% over the total hold period.

From the previous calculations, note that the X and Y buffers are just able to supply the required currents within the acceptable value of droop. However, the Q buffer must supply three times this current with less than 2% droop which requires, for the same output voltage, a smaller R_2 and larger C_2. But if we make C_2 larger, clamping becomes more difficult; hence we must introduce more gain into the Q buffer so that a larger R_2 can be used. Using a gain of 5, the output is 5 volts maximum instead of 1 volt, the required 0.5 mA can be achieved with $R_2 = 10\ k\Omega$, and with C_2 still at 15 μF, the total droop is 1.67% in the 2.25-msec hold period.

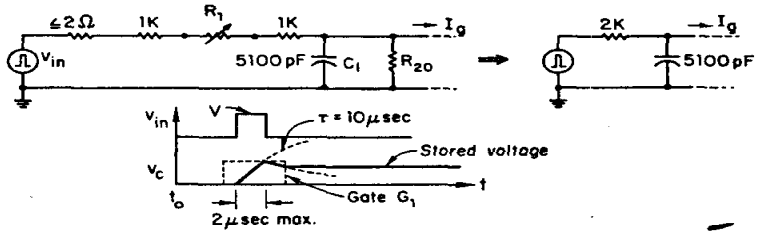
c. Gated Integrator Details. The maximum current through the switch Q1 (Fig. 7a) is $\frac{5V}{2k\Omega} = 2.5$ mA for the X and Y circuits, and $10V/2k\Omega = 5$ mA for the Q integrator. The switch must be driven with at least 10 mA to assure that its on-resistance is reasonably constant for all possible signals. The variation of resistance R_{on} with drive I_b (Ref. 5) is shown in Fig. 8a. Above 10 mA, the resistance is below 5 ohms. However, too large a drive current should not be used, because the offset-voltage is less predictable. A detailed analysis of the dc characteristics of the chopper is given in Ref. 5.

During the gating of the beam-induced signal, the circuit of Fig. 7b applies. Measurement has shown that the leakage currents through R_{10} and R_{20} are negligible for voltages of 2 volts or less, in comparison with I_g, the FET gate leakage current. Thus, the circuit reduces as shown.

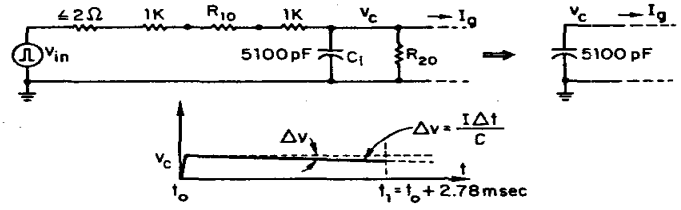
During the charging period depicted by Fig. 7b, I_g can be neglected. The peak voltage developed on the capacitor is $v_o = V(1 - e^{-t/\tau})$



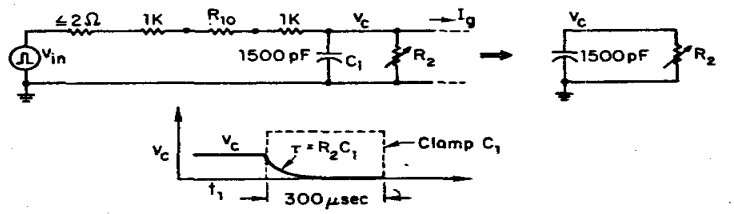
a) COMPLETE CIRCUIT



b) Q1 ON, Q2 OFF



c) Q1 OFF, Q2 OFF



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d) Q1 OFF, Q2 ON

FIG. 7—GATED INTEGRATOR EQUIVALENT CIRCUITS.

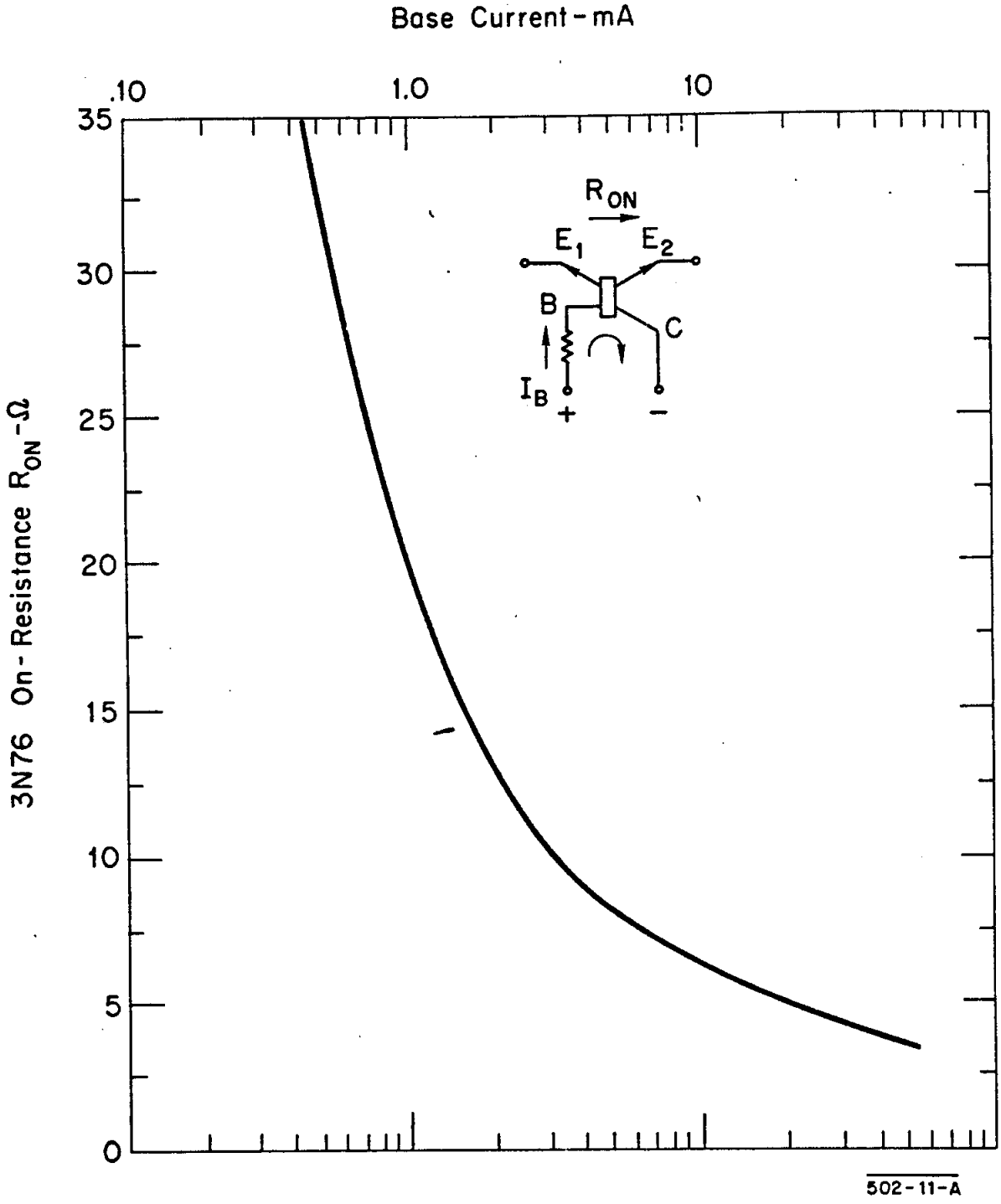


FIG. 8(a) – 3N76 RESISTANCE vs BASE CURRENT

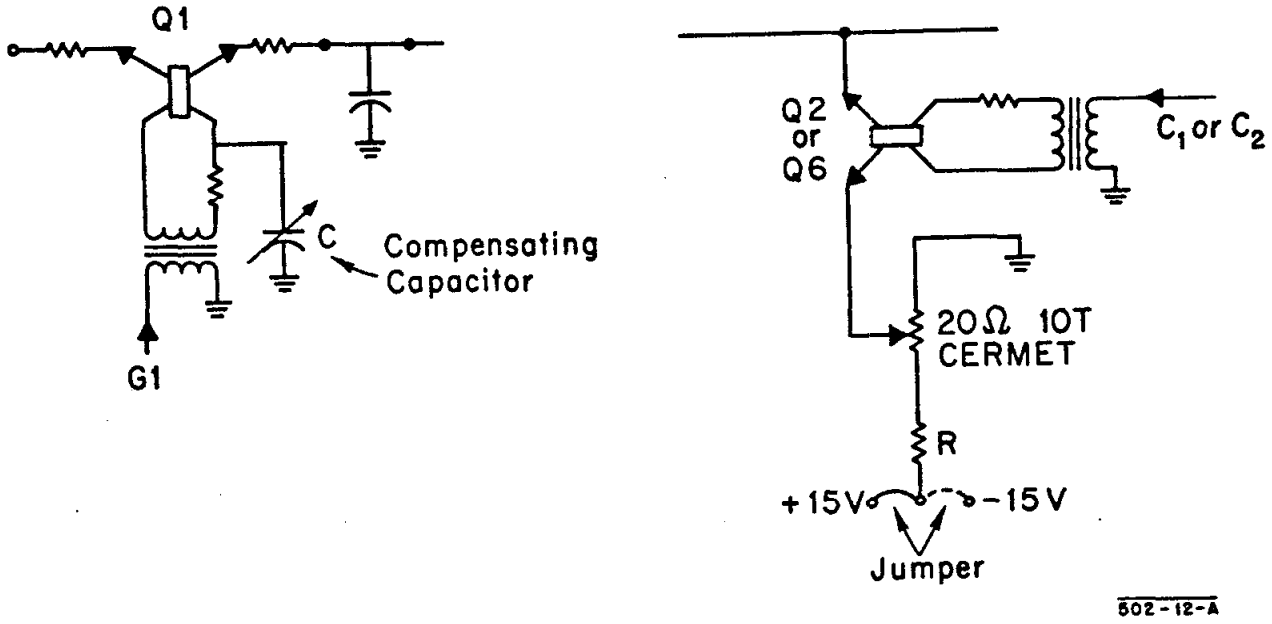


FIG. 8(b) - INTEGRATOR OFFSET COMPENSATION

where t = pulse width = 0.2-2 μsec

τ = integrator time constant .

The initial slope of the ramp is

$$\left.\frac{dv_o}{dt}\right|_{\substack{v_o = 0 \\ t = 0}} = \frac{d}{dt} V_i (1 - e^{-t/\tau})$$

$$= V_i \left(\frac{1}{RC}\right) e^{-t/\tau}\Big|_{t=0}$$

$$= \frac{V_i}{RC} \rightarrow \frac{1}{RC} \quad \text{for a unit step.}$$

The deviation from linearity, ϵ, at the end of T seconds is

$$\epsilon = \frac{V_i \left(\frac{T}{RC}\right) - V_i \left(1 - e^{-T/RC}\right) \times 100\%}{V_i}$$

$$= \left[-1 + \frac{T}{RC} + e^{-T/RC}\right] \times 100\% \quad .$$

The error as a function of pulse width is shown in the following table:

	Pulse Width T(μsec)	τ = 20 μsec		τ = 10 μsec	
		T/τ	$\%\epsilon$	T/τ	$\%\epsilon$
	0.2	0.01	-0.6	0.02	-1.0
	0.4	0.02	-1.0	0.04	-2.7
Max. beam width	2.0	0.10	-5.0	0.20	-9.0
	4.0	0.20	-7.0	0.40	-17.5
	10.0	0.50	-21.6	1.00	-36.6

Thus, for a 2-μsec maximum pulse width, the maximum error for $\tau = 10\ \mu$sec is -9%, and for $\tau = 20\ \mu$sec, -5%.

Because the gate width is fixed, there will always be a decay of the peak voltage before Q1 turns off. This results in a greater proportion of charge leaking off for a narrow pulse than for a wide pulse, which introduces another form of error. This topic will be considered later; in the subsequent discussion, it will become apparent that although the absolute accuracy of the ℓn Q signal is significantly affected by this type of error, the comparative accuracy of the system from sector-to-sector is negligibly affected.

During the 2.25-msec hold period, Fig. 7c applies. The leakage current I_g is determined by the fixed bias, $V_{gs} \approx -3$ volts. Since in the source-follower configuration V_{gs} is constant, I_g is also constant; a typical measured value for the 2N2607 is 1 nA at 50° C.

The 1-nA maximum leakage current to the FET causes an error which is important only at the lowest signal levels. During the hold interval a negative ramp voltage is produced which is given by

$$\Delta V = \frac{\Delta Q}{C} = \frac{I_g \Delta t}{C} \quad .$$

For X and Y buffers,

$$\Delta V = \frac{(1 \times 10^{-9}) \left[2.25\,(10^{-3})\right]}{5100\ (10^{-12})} = 0.44\ \text{mV} \quad .$$

In the worst case, for a Q-input 60 dB below the maximum, this would cause 4.4% droop. This is not important because a threshold is set to reject any input below -60 dB; however, this leakage is a definite limitation to extending the dynamic range of the system.

At $t_o + 2.25$ msec, Q2 is actuated and the circuit of Fig. 7d applies. Since R_2 is about 5 ohms, the decay time constant is

$$R_2 C_1 = 5(5100)\ 10^{-12} = 25.5 \text{ nsec} \quad .$$

Thus, the hold capacitor C_1 is restored essentially instantaneously compared with the output coupling capacitor C_2.

d. High Input Impedance Buffer Design. The equivalent circuit derivation and expressions for gain and output impedance are illustrated in Fig. 9a. For the circuit used, the following values apply:

$$R_s = 1.5k\Omega,\ R_o = 6.8k\Omega,\ re_1 = 250 \text{ ohms at } 0.1 \text{ mA},$$
$$\beta_1 = 35 \text{ (2N1711)},\ \beta_2 = 100 \text{ (2N2905A)},$$
$$gm = 330\ (10^{-6}) \text{ (2N2607)} .$$

This gives $gm\ h'_{fe} R_s = 760$, from which

$$Av = \frac{760}{1 + 760} \approx 1 - \frac{1}{760} = 0.99869$$

$$Z_o = \frac{1500}{1 + 760} = 1.97 \text{ ohms} \quad .$$

The circuit shown applies only to very low-frequency signals, since the parallel input capacitance of about 3 pF has not been included. The equivalent input resistance of the FET is determined mainly by the gate-source leakage current I_{gs}. Since I_{gs} is fixed by V_{gs}, and V_{gs} is constant in this circuit, then

$$R_{in} = \frac{V_{in}}{I_{gs}}$$

Thus R_{in} varies with V_{in} as shown in Fig. 9b.

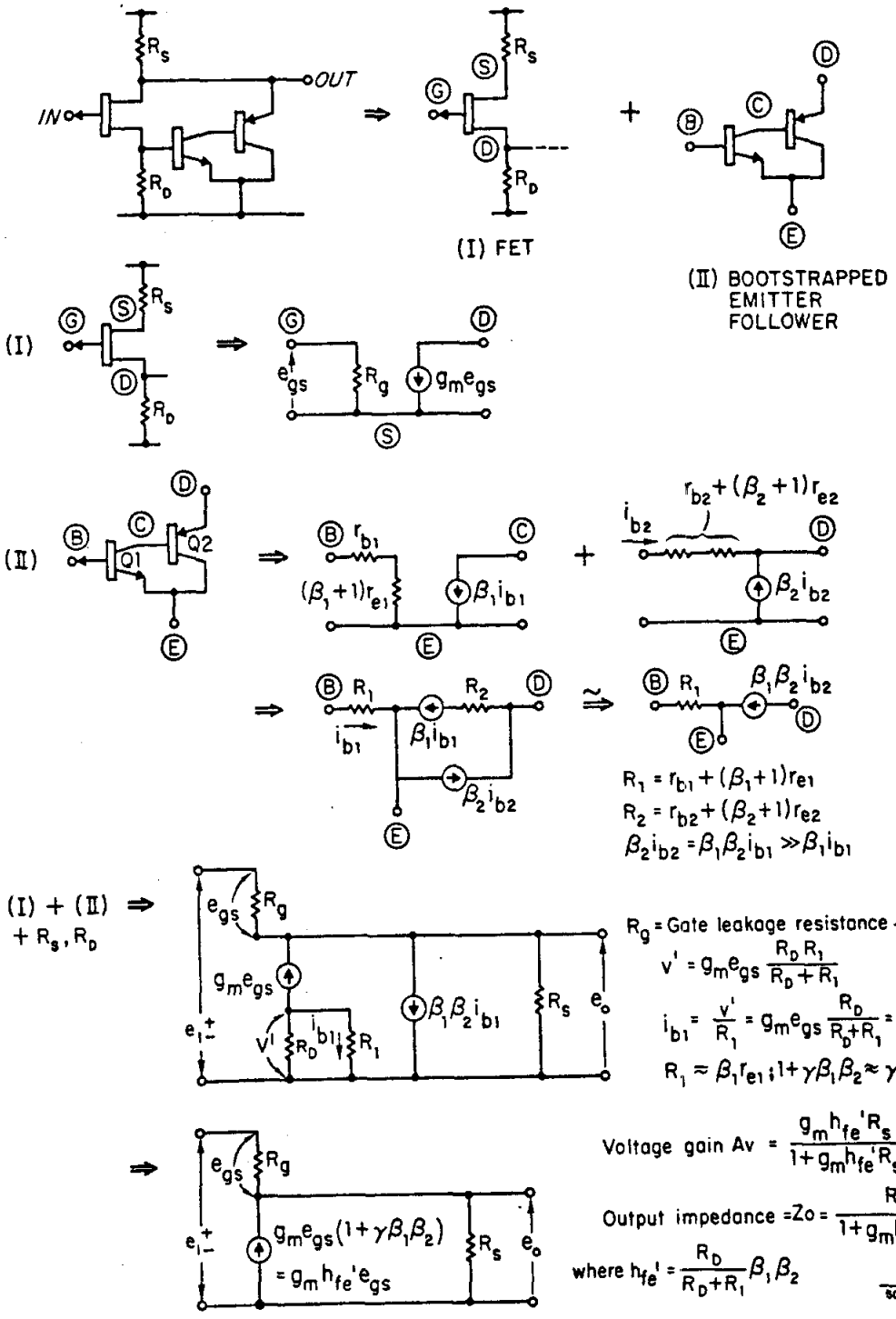
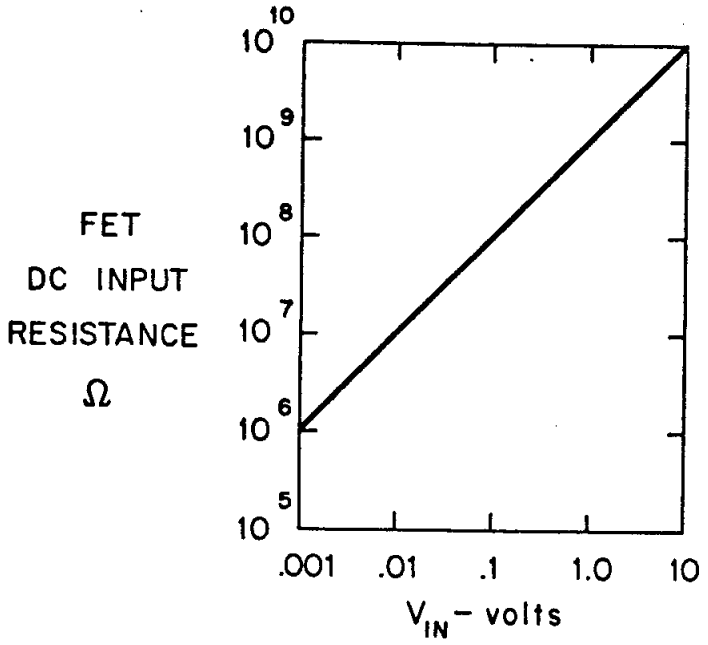


FIG. 9(a)-DERIVATION OF BUFFER EQUIVALENT CIRCUIT



DC $R_{IN} = \frac{V_{IN}}{I_{gs}}$

I_{gs} = gate-source leakage
= 1 nA @ V_{gs} = -3V

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FIG. 9(b) – FET INPUT RESISTANCE

e. Offset Compensation. An important factor which has not yet been mentioned concerns the operation of the 2.5-μsec gate transistor Q1 of Fig. 6a. When driven with a fast-rising pulse, momentary currents are induced in both emitters even with no signal present. These currents decay to zero in 50-100 nsec. In the case of a sample-and-hold circuit such as that under discussion, a small voltage can be developed on the hold or integrating capacitor. Although for equal rise- and fall-time pulses the net impulse of charge tends to be zero, there is always an imbalance due to storage effects in the transistor and stray capacity of the coupling transformer. The resulting offset levels can easily be a few millivolts; hence some form of compensation is required.

Two forms of compensation are used. A small capacitor connected from base to ground can reduce the offset to essentially zero (Fig. 8b). The effect is not fully understood and is still being studied; however, it appears that the offset is always in the same direction, by an amount depending on the detailed structure of the particular transistor. It is surmised that the capacitor either slows the turn-on and reduces the accompanying emitter transient, or stores a charge during turn-on which adds to the transient during turn-off.

An auxiliary form of compensation is used to provide for variations in transistor characteristics. This involves simply returning the normally-grounded emitter of Q2 or Q6 to a small adjustable bias voltage as depicted in Fig. 8b. In the present case, this is perfectly satisfactory; however, it should be noted that in general, the increase in resistance in the clamp path is undesirable because it increases the time required to restore the hold capacitor.

f. Coupling Capacitor Leakage. A final consideration involves the leakage current in the large output coupling capacitor, C_2 of Figs. 6a and 6b. Generally speaking, leakage current is voltage-dependent and will result in an additional change in the voltage on C_2 during the hold period. Also, the capacitor leakage resistance is somewhat temperature-dependent. Since the buffer maintains a fixed bias of about 3 volts across the capacitor regardless of signal level, a constant leakage current will result.

To maintain the voltage offset produced in this manner during the hold period to negligible proportions, it is necessary to use a high quality, solid electrolyte tantalum capacitor. It has been experimentally verified that even at 70° C, the leakage current in such a unit is below 100 nA at 6 volts bias; hence on a 15-μF capacitor, the voltage offset at the end of 2.25 msec will be only 15 μV.

2. Logarithmic Amplifier

a. Design Criteria. The basis of the logarithmic amplifier is a commercial operational amplifier having the following characteristics:

Open Loop Gain = 5×10^7 (min) at dc

Bandwidth at Unity Gain = 1 MHz

Equivalent Input Noise = 5 μV p-p to 1 cps

10 μV rms 10-1000 cps

Offsets - Voltage = $\pm$ 20 μV max, adjustable to zero

Current = $\pm$ 20 pa max, adjustable to zero

Output = 5 mA $\pm$ 26 volts

Output Z = 10 ohms open loop

Temperature Range = 0° to 55° C

A logarithmic response employing diodes is very easily implemented using such an amplifier; the complete circuit is shown in Fig. 10a. The main considerations are twofold: First, a diode must be found having a voltage - ℓn (current) characteristic which is linear over at least 3 decades of current; second, the maximum gain which can be achieved is restricted by bandwidth requirements.

In addition, one must stabilize the diode against ambient temperature variations, and simultaneously, must maintain the thermally-generated diode leakage current below the lower limit of the input current dynamic range. Obviously, current and voltage variable offsets in the amplifier itself should be negligible.

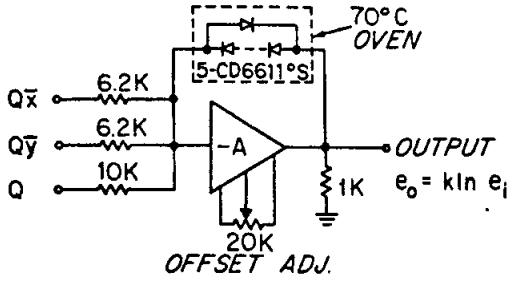
b. Transfer Function. Consider the simplified circuit of Fig. 10b. R_f is shown as a variable since the diode resistance r_d varies with current. Neglecting capacitance across the diodes, and assuming that current into the amplifier from the summing junction is zero (both excellent approximations), the analysis is straightforward:

Equating currents,

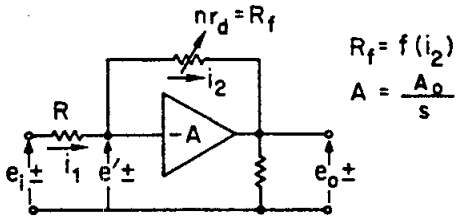
$$\frac{e_1 - e_i}{R_1} = \frac{e_i - e_o}{R_f}$$

$$e_o = -Ae_i$$

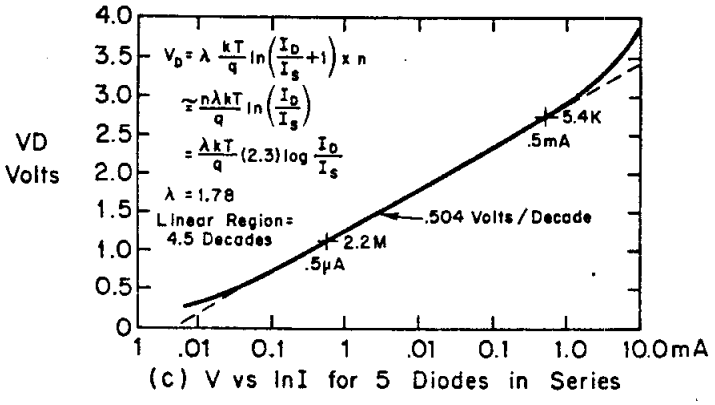
$$\therefore \quad \frac{e_1 + \frac{e_o}{A}}{R_1} = \frac{\frac{-e_o}{A} - e_o}{R_f}$$



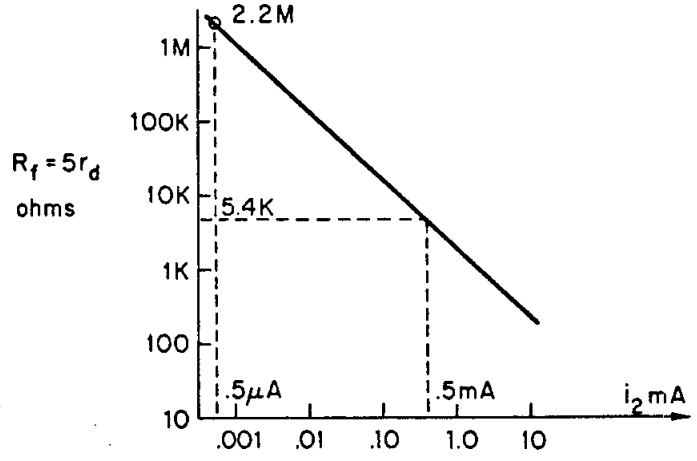
(a) Schematic



(b) Equivalent Circuit



(c) V vs lnI for 5 Diodes in Series



(d) Diode Resistance vs Input Current

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FIG. 10 - LOGARITHMIC AMPLIFIER

Hence

$$e_o = \frac{-e_1}{\left\{\frac{R_1}{R_f} + \frac{R_1}{AR_f} + \frac{1}{A}\right\}}$$

If $A \rightarrow \infty$, the expression is the familiar ideal case,

$$e_o = - e_1 \frac{R_f}{R_1}$$

With a dc gain of 5×10^7, the closed-loop gain is accurate to $< 1\%$, at low frequencies, for gains up to 5×10^5. The practical limitation to high gain is therefore determined by the required bandwidth, since the gain-bandwidth product is only 1 MHz.

c. Stability and Gain-Bandwidth. Assuming that over the frequency range of interest, the diodes can be represented by a pure resistance, then the amplifier is absolutely stable. That is to say, the gain function is well represented by

$$G(s) = \frac{R_f/R_1}{1 + s\tau}$$

where $\tau = (R_f/R_1 + 1)/A_o$, and $1/\tau = \omega = 2\pi(10^6)$ for $R_f/R_1 = 1$.

For the present case, it will be seen that the maximum diode resistance for a single diode is ≈ 100 kΩ; hence, for a capacitance across the junction of 1 pF,

$$f_{hi} = \frac{1}{RC} = \frac{1}{10^5 \times 10^{-12}} = 10^7 \text{ Hz}$$

which is an order of magnitude higher than the unity-gain bandwidth of the amplifier, and several orders higher than the maximum practical bandwidth. Hence, the system can be treated as a single-pole function.

The resistance R_f is derived from the diode equation as follows:

$$I_d = I_s \left(\exp \frac{qv}{\lambda kT} - 1\right)$$

where I_d is the diode current

I_s is the reverse saturation current

v is the diode voltage

q is the electron charge

k is Boltzmann's constant

T is the absolute temperature

λ is a factor which accounts for the transition region recombination in the junction[6]

For the silicon diodes being considered, I_s is approximately 36 pA at 70°C; since this is about 4 orders of magnitude below the minimum signal current, the expression can be written as

$$I_d \approx I_s \exp \frac{qv}{\lambda kT}$$

Hence,

$$\ell n \left(\frac{I_d}{I_s}\right) = \frac{qv}{\lambda kT}$$

$$\therefore v = \frac{\lambda kT}{q} \ell n \left(\frac{I_d}{I_s}\right)$$

The equivalent diode resistance thus becomes

$$r_d = \frac{v}{I_d} = \frac{\lambda kT}{qI_d} \ell n \left(\frac{I_d}{I_s}\right)$$

From experiment, λ is found to be 1.78 for the diodes used; k, T, and q are known; and, as stated above, I_s is calculated from a point on the forward

characteristic to be 36 pA at 70°C. Note that r_d as defined here is not the incremental diode resistance, which varies simply as $\frac{\lambda kT}{qI_d}$, but rather the large-signal dc resistance.

The total feedback resistance is just r_d times the number of diodes n in series, or

$$R_f = n \frac{\lambda kT}{qI_d} \ell n\left(\frac{I_d}{I_s}\right)$$

The linear range (on a semi-logarithmic scale) of 5 diodes in series is shown in Fig. 10c. The range is seen to extend over 4 to 5 decades of current from a maximum current of about 0.5 mA. For the same 5 diodes, Fig. 10d gives $r_d \cong 5.4\ k\Omega$ at 0.5 mA, and about 2.2M at 0.5 μA, which is a range of 3 decades. Since the input summing resistor for the Q signal is 10 kΩ, the extremes of voltage gain are:

$$I = 0.5 \text{ mA}, \quad G_1 = \frac{5.4\ k\Omega}{10\ k\Omega} = 0.54$$

$$I = 0.5\ \mu\text{A}, \quad G_2 = \frac{2.2\ M}{10\ k\Omega} = 220$$

The minimum bandwidth is thus determined from the gain-bandwidth product:

$$G\beta = 1.0 \text{ MHz} = 10^6$$

$$\beta_{min} = \frac{10^6}{G_2} = \frac{10^6}{220} = 4.55 \text{ kHz}$$

The corresponding rise time t_r is given by the approximation

$$\beta t_r \approx 0.35$$

$$\therefore \quad t_r = \frac{0.35}{4.55 \times 10^3} = 77\ \mu\text{sec}$$

For output signal pulse widths of 550 μsec, this is an acceptable rise time. However, it can be appreciated that to extend the dynamic range of the system, either the speed of operation must be reduced, or an amplifier with a much higher gain-bandwidth product must be employed. This transfers the problem to another area, however: Wider bandwidth operational amplifiers are more difficult to stabilize and hence generally have lower open-loop gain, so the dynamic range would become limited by linearity, rather than bandwidth, considerations.

d. Output Signal Levels. From the previous calculation, the voltage gain of the amplifier varies from 0.5 at maximum signal to 220 at minimum (-60 dB) signal. Therefore,

$$v_o(\text{max}) = 5 \times 0.5 = 2.5 \text{ volts}$$

$$v_o(\text{min}) = \frac{5}{1000} \times 220 = 1.1 \text{ volts}$$

where v_o is a voltage representing $\ell n Q$.

The logarithmic slope is then

$$k(\text{volts/dB}) = \frac{2.5-1.1}{60} = 23.3 \text{ mV/dB}$$

For the maximum input signals, we have currents corresponding to Q and $\pm Q\bar{x}$ or $Q\bar{y}$ of 0.5 mA and $\pm$ 0.16 mA, respectively. The position signal outputs will be proportional to:

$$\ell n(Q + Q\bar{x}) - \ell n\, Q$$

$$= \ell n \left[1 + (Q\bar{x}/Q)\right]$$

$$= \ell n \left[1 \pm (0.16/0.5)\right]$$

$$= \ell n\,(1 \pm 0.32) \rightarrow \ell n\, 1.32 \text{ or } \ell n\, 0.68$$

$$\rightarrow 0.278 \text{ or } -0.385$$

Thus for a position signal in the same direction as Q, the output will be 13.1% below the nominal value (corresponding to 0.32), whereas in the opposite direction, it will be 20.3% above the nominal value. At the output of the logarithmic amplifier, the maximum $Q\bar{x}$ or $Q\bar{y}$ voltages are as follows:

$$+ Q\bar{x},\ \bar{y} \rightarrow + 2.41 \text{ dB} \times 23.3 \text{ mV/dB} = + 56.2 \text{ mV}$$

$$- Q\bar{x},\ \bar{y} \rightarrow - 3.34 \text{ dB} \times 23.3 \text{ mV/dB} = - 77.8 \text{ mV}$$

These maximum voltages of course remain essentially fixed as the Q input is varied over a 60-dB range, since $Q\bar{x}$ and $Q\bar{y}$ (maximum) are always a fixed proportion of Q.

Figure 11a shows the amplifier output for 10–dB steps of the ℓnQ input signals. Details of the position signals are shown in Fig. 11b for maximum ℓnQ input.

e. Linearity. The linearity of the logarithmic characteristic was observed by discharging a capacitor into the input. This produces a voltage of

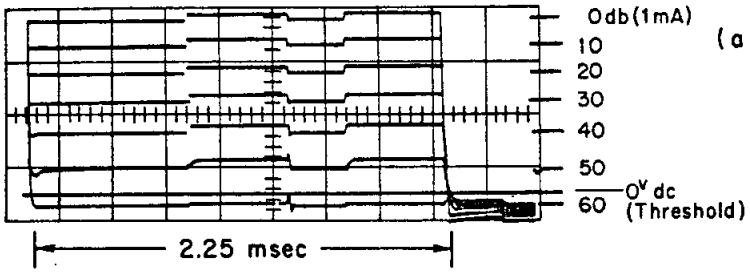
$$v_{in} = v_o e^{-t/RC}$$

and a corresponding output

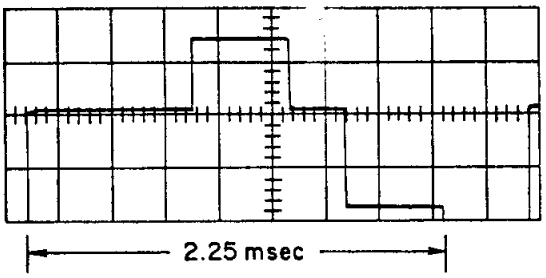
$$v_o = k \ell n\, v_{in} = k \left[\ell n\, v_o - t/RC\right]$$

which decays linearily with time. The input and output waveshapes are shown in Fig. 11c, where it is seen that reasonable linearity prevails over nine time-constants ($\approx$4 decades) of the input signal, down to the noise level of the amplifier.

It is interesting to note that the variation in position signal output amplitude as the input is varied over the 60-dB dynamic range, for a fixed ratio of

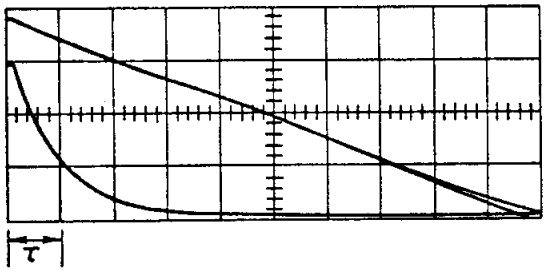


(a) Logarithmic Amplifier Response to 10db Input Steps.



(b) Position Signal Outputs For Maximum Inputs Q @ 0db

Vertical - 50 mV/cm

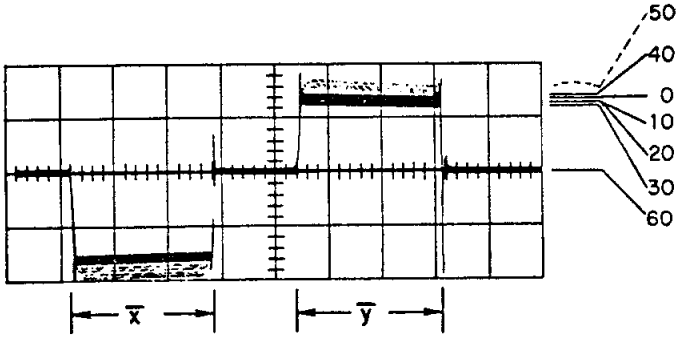


(c) Response to Exponential Input

Top - Output

Bottom - Input

τ = 1cm Horizontal



(d) Position Signal Linearity Output for 10db Steps of Q.

Horizontal = 200 μs/cm

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FIG. 11 - LOGARITHMIC AMPLIFIER LINEARITY

$Q\bar{x}$ or $Q\bar{y}$ to Q, gives a measure of the deviation of the diode characteristic from the ideal. Figure 11d shows $Q\bar{x}$ and $Q\bar{y}$, for a constant simulated $\bar{x}$ and $\bar{y}$, for 10-dB steps over the range. Because the maximum signal represents an average increment of the range of close to 3 dB, the variations shown in Fig. 11d represent nonlinearities of about 0.3 dB. This in turn is equivalent to a deviation in position of about 1 mm on a 10-mm maximum scale.

3. DC Amplifier and Threshold Circuit

a. Function. The dc amplifier and threshold adjustment are shown in Fig. 12. The purpose of this portion of the system, besides amplification, is to eliminate the portion of the waveform of Fig. 11a which lies below -60 dB. It is in this region that (1) transistor clamp offsets become important, (2) the gain of the system becomes high so that noise enters, (3) the logarithmic amplifier bandwidth starts to limit, and, to a lesser degree (4) the diode characteristic becomes distorted. In order to provide a display that will not give completely spurious results at the noise levels, it is necessary to provide a lower threshold; i.e., the system could saturate in trying to normalize noise levels, since the Q, $Q\bar{x}$ and $Q\bar{y}$ signals would no longer bear the required amplitude relationship to each other.

The dc amplifier output is taken through an emitter follower and zener diode, where the zener acts to eliminate the lower portion of the signal. A bias adjustment swings the quiescent voltage of the amplifier output in order to vary the clip level.

b. DC Amplifier Design. The dc amplifier is based on a unique design by Bénéteau[7] which uses planar passivated transistors in a modified Slaughter circuit. In Fig. 12a, the PNP transistor acts as a constant-current source for the NPN and better stabilizes the base-emitter drop. The planar

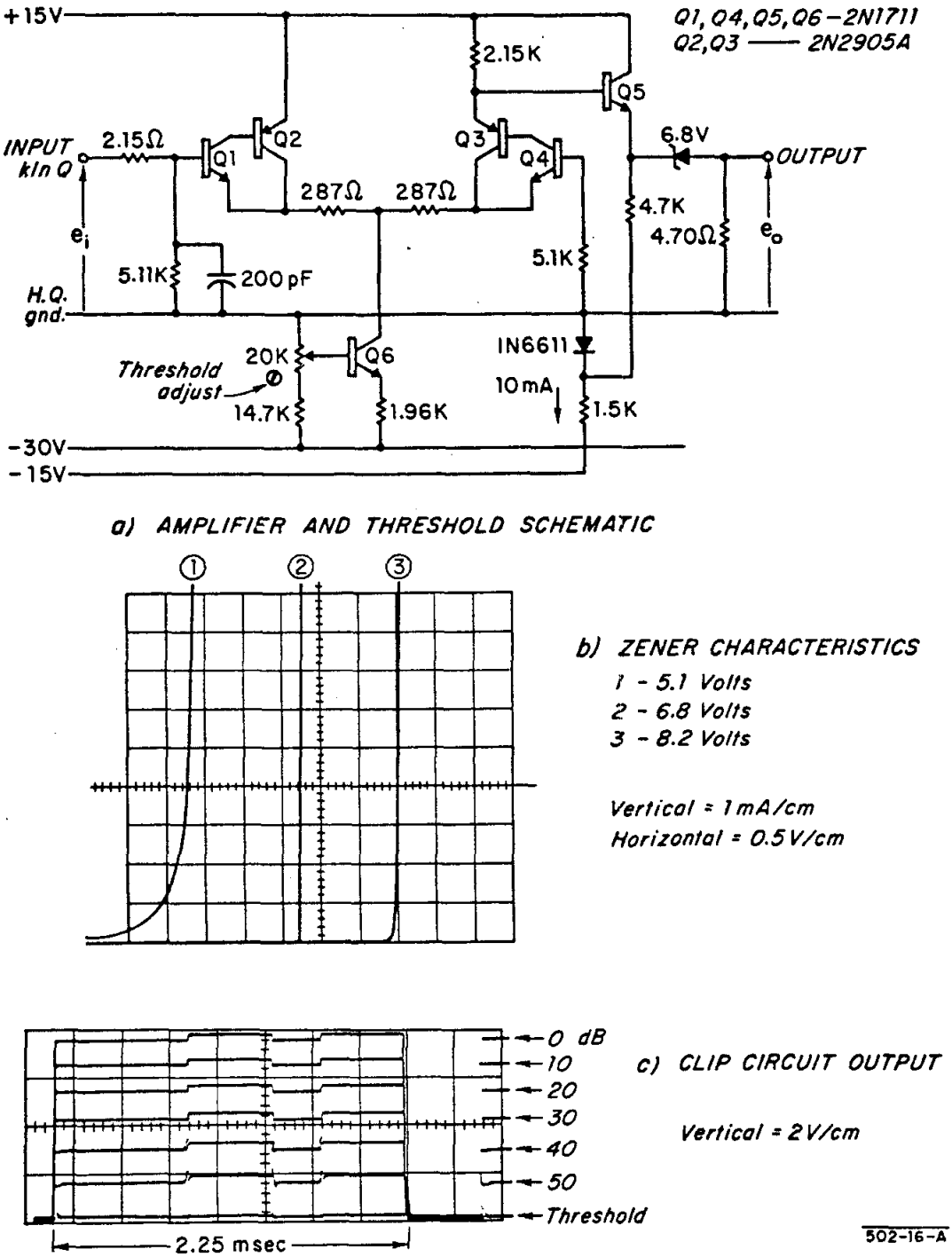


FIG 12—DC AMPLIFIER AND THRESHOLD CIRCUIT

passivated junction is already particularly stable compared with other constructions. An overall temperature stability of 1 mV/^{o}C is achieved. Furthermore, the compound transistor connection results in an equivalent transistor with a β of somewhat less than $\beta_1 \beta_2$, where 1 and 2 represent the NPN and PNP respectively, so that negligible input current is required.

c. Threshold Circuit. The operation of the circuit is straightforward: The amplifier bias is set to Δv volts below the zener voltage, where Δv is the required clip voltage above the baseline. In practice, one must select a unit which has a low temperature coefficient of the zener voltage, and which provides a reasonably sharp zener characteristic. The first point is important to long-term stability of the system, and the second, to linearity at low levels.

The best compromise was found to be a 6.8-volt zener. In this unit, the zener voltage knee is remarkably sharp, as can be seen in Fig. 12b. A 5.1-volt unit (optimum temperature coefficient) and an 8.2-volt unit are shown for comparison.

The temperature coefficient of the 6.8-volt unit is 0.040%/^{o}C; this causes a change in the clip level as a function of temperature of about $\pm$ 1% of full scale, for a temperature change of $\pm$ 25^{o}C.

The maximum output signal through the zener is 5 volts. At a level of 1 volt (-50 dB), the current through the zener is only slightly more than 2mA. It can be seen from Fig. 12b that below this current level considerable nonlinearity would result if either the 5.1- or 8.2-volt unit were used.

The clipped output signal is shown in Fig. 12c. The threshold is adjusted to make the increment from 40 to 50 dB equal to that from 50 dB to cutoff.

4. Intermediate Clamp and Buffer

a. Function. The purpose of this portion of the circuit is to recover $\ell n Q$, $\overline{x}$ and $\overline{y}$ signals in serial format, all referred to a common baseline. The circuit and its waveforms are shown in Fig. 13. The FET buffer and output clamp are very similar in operation to the integrator circuit already described, and will not be discussed further. The input coupling capacitor and clamp operate as follows: The input voltage v_i rises to a level proportional to $\ell n Q$ and remains there for 550 μsec. The output voltage v_o rises to the same level. Capacitor C retains its initial charge of zero volts. At this point, Q1 and Q2 are actuated for 300 μsec to clamp the outputs of C_1 and C_o to ground. This charges C_1 to $k\ell n$ Q volts; the output voltage v_o drops to zero. The remaining sequence is straightforward: $\overline{x}$ is allowed to pass, the clamps are reactuated; $\overline{y}$ passes, and again Q1 and Q2 are simultaneously actuated as the input signal drops to zero. Thus, the signal emerges as ℓn Q, $\overline{x}$ and $\overline{y}$ in serial form, and the initial conditions are restored.

b. Design Considerations. The main difficulty with the circuit shown involves the selection of C_1. This capacitor must be chosen small enough to restore quickly through the 470-ohm source resistance once the input drops to zero and back-biases the zener diode. It must not be chosen too small, or the leakage current of the FET will cause unwanted slopes atop the various pulses. This would be particularly serious because here the position signals have less than 100-mV maximum amplitude, and a change of 5 or 10 millivolts would be intolerable. With C_1 = 1000 pF, the maximum leakage current produces a change of 1-2 millivolts, which is quite acceptable.

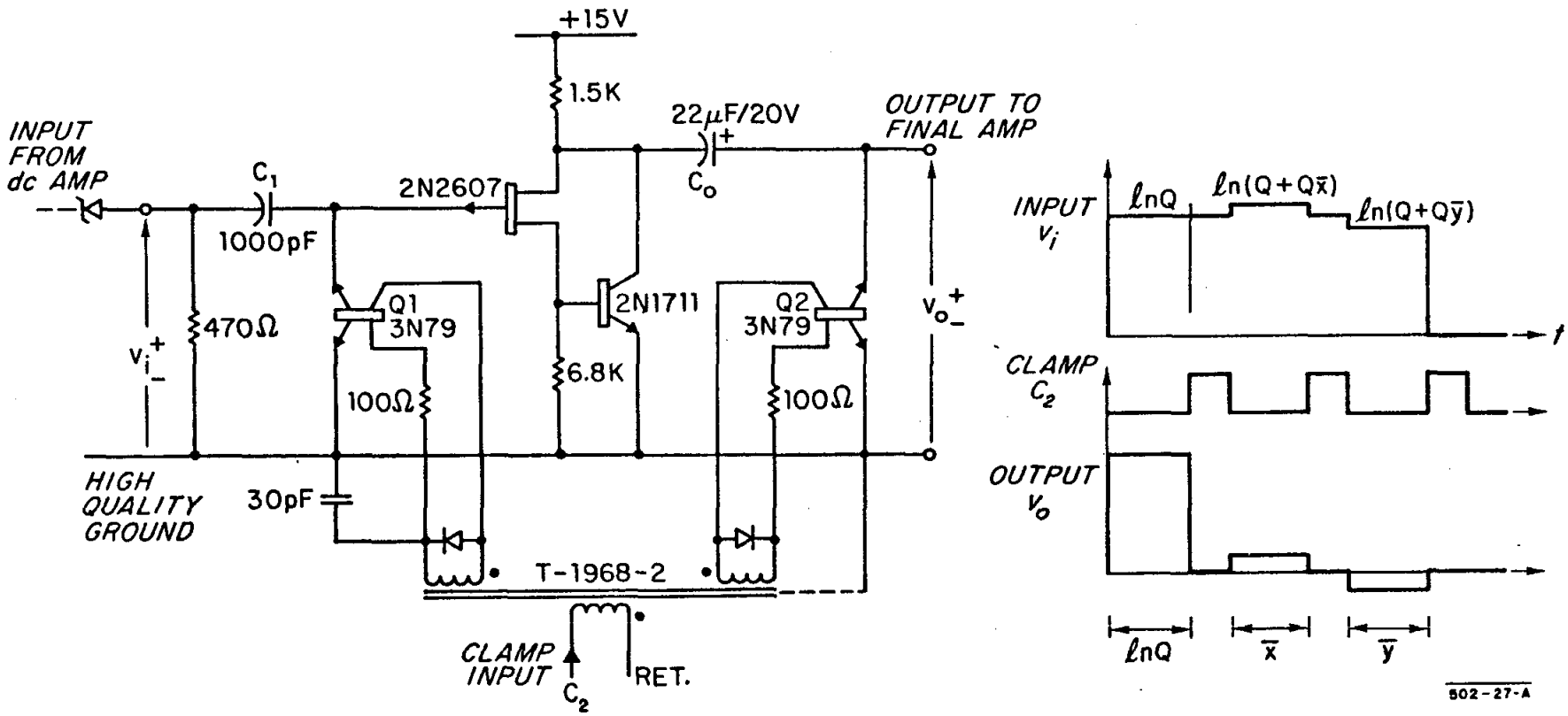


FIG. 13 - INTERMEDIATE CLAMP AND BUFFER

5. Range Switch, Amplifier and Baseband Transmitter

The complete circuit to be discussed is shown in Fig. 14. The overall operation is straightforward and will be described only briefly.

a. Range Switch. The purpose of the range switch is to attenuate the $\ell n\ Q$ signal to the same level as the $\overline{x}$ and $\overline{y}$ signals, so that all three signals can be amplified to the same nominal value. Transistor Q5 is back-biased while $\ell n\ Q$ is present, resulting in approximately 25 times attenuation of $\ell n\ Q$ at the input to the dc amplifier. When $\overline{x}$, and later $\overline{y}$, appear, Q5 is closed to pass these signals without attenuation.

b. DC Amplifier. The amplifier employs straightforward voltage feedback to obtain an overall gain of about 40. The gain is adjustable to provide for differences in the λ factor in the diode equation, i.e., to provide for different slopes of the diode voltage $-\ell n$ (current) characteristic from unit to unit.

c. Baseband Transmitter.[8] The function of the baseband transmitter is to isolate and buffer the dc amplifier output, and to provide a balanced output to drive a 600-ohm characteristic impedance transmission line. The transformer is a high quality audio unit. It must have a large enough inductance to prevent excessive droop on the signal pulses, and sufficient high-frequency response to preserve a reasonable rise time. Details of the circuit performance are given in Ref. 8.

6. Baseband Receiver[8]

Although the receiver will not be described in detail, it is worthy of brief mention. The circuit, exclusive of timing circuits, is shown in Fig. 15. Its function is to restore the signal amplitude to a zero baseline by means of a clamp. The clamp is driven by timing circuitry which is essentially identical

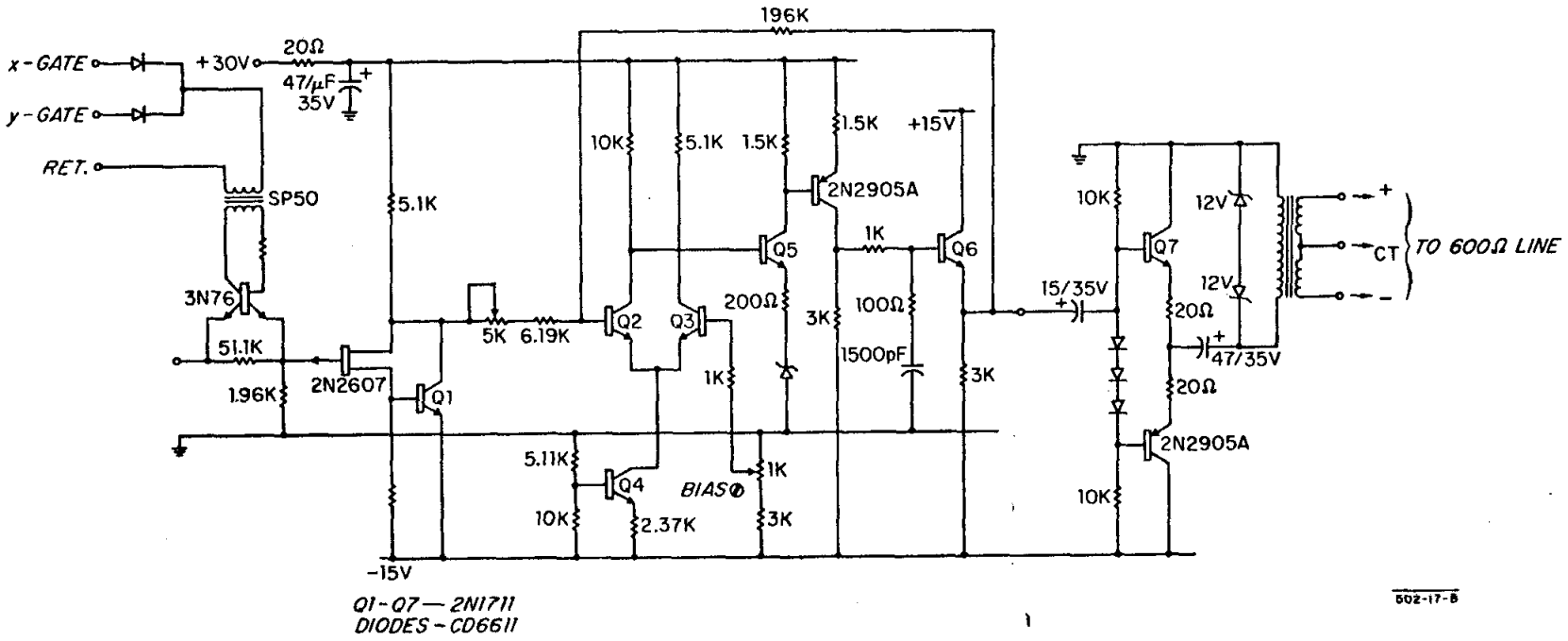


FIG. 14 — RANGE SWITCH, AMPLIFIER AND BASEBAND[8] TRANSMITTER.

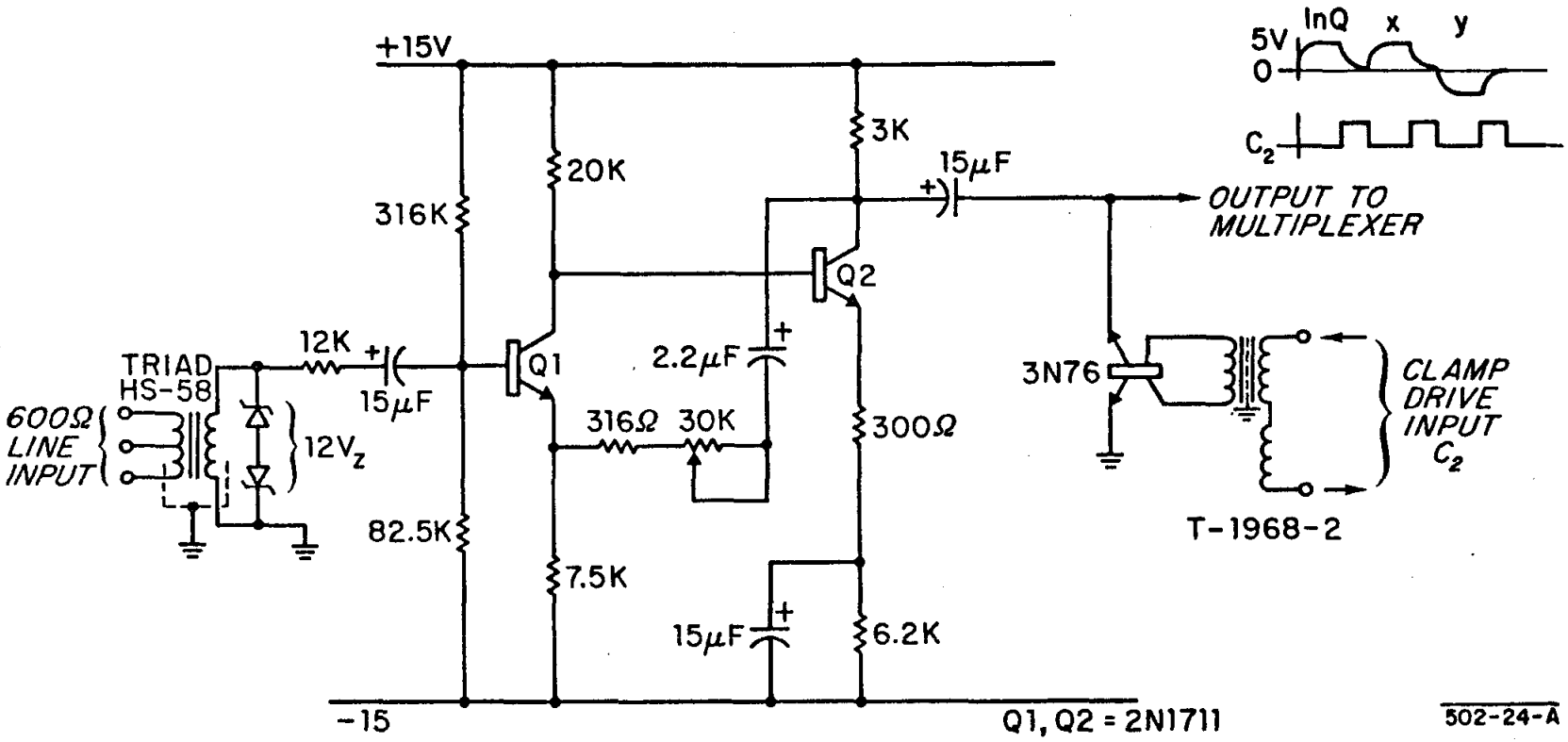


FIG. 15—BASEBAND RECEIVER CHANNEL[8]

to that contained in the main chassis. An additional function is to provide gain to compensate for differences in transmission losses. Details of the overall baseband response are given in Ref. 8.

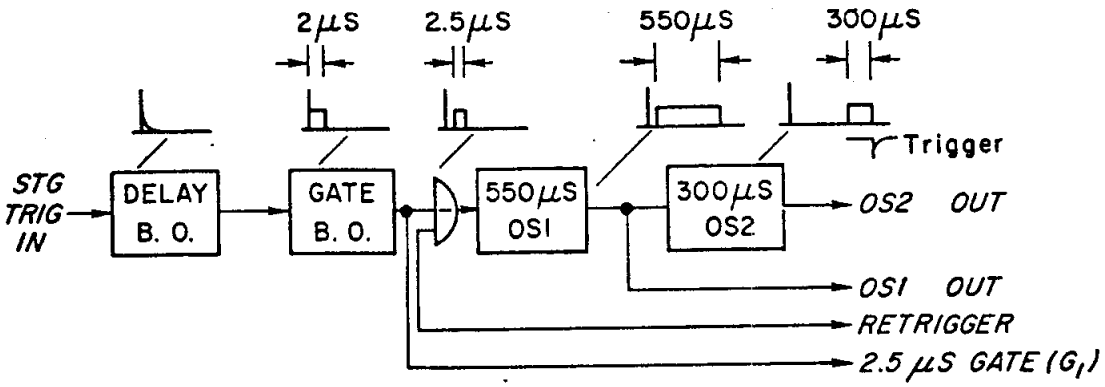
7. Timing Circuits

The block shown in Fig. 5 as "ℓn Q, X and Y Timing" will be described only functionally, since the circuits are quite straightforward. The only extraordinary feature of note is that the one-shots require very stable timing components; i.e., metal film fixed resistors, silver mica capacitors, and cermet trimpots, in order to achieve good temperature stability. In addition, a saturated design is used to achieve timing stability in the presence of supply voltage variations.

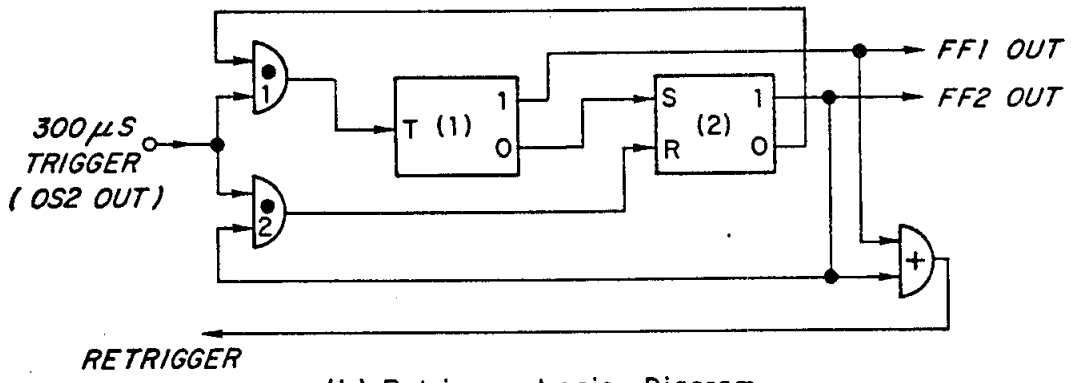
a. Functional Description. The circuit block diagram is shown in Figs. 16a, b, and c. Figure 17 illustrates the waveforms.

The main requirement of the circuit is to produce gate pulses for serializing ℓn Q, $\overline{x}$ and $\overline{y}$, and restoring pulses for clamping the integrating and coupling capacitors. The most straightforward approach to the problem would be to have a circuit of six consecutive one-shots, and provide either one circuit located at each sector, or one master circuit driving all sectors via transmission lines. The approach actually taken minimizes the number of one-shots, thus optimizing the timing stability to the point where independent circuits can be installed at each sector.

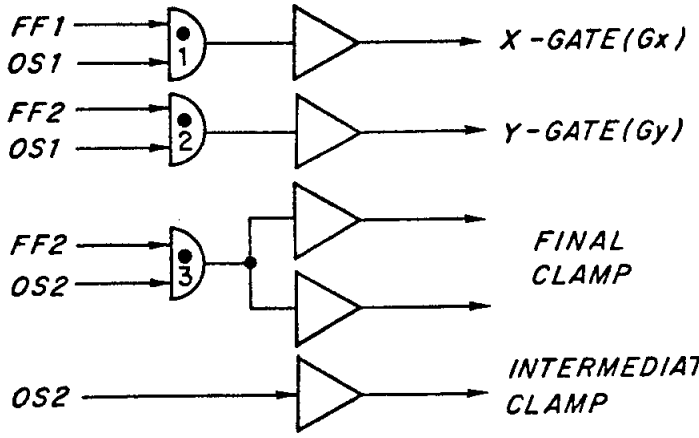
The number of one-shots is minimized at two when a recirculating trigger scheme is used (Fig. 16b). With this arrangement, the 360-pps STG pulse triggers the cascaded 550-μsec and 300-μsec one-shots once; and the retrigger logic enables the 300-μsec one-shot turnoff to retrigger the cascaded pair two more times. At this point, further triggering is blocked and the circuit has



(a) Blocking Oscillator and One-shot Gate Generators



(b) Retrigger Logic Diagram



(c) Output Gates and Drivers 502-8-A

FIG. 16 - TIMING CIRCUIT BLOCK DIAGRAM

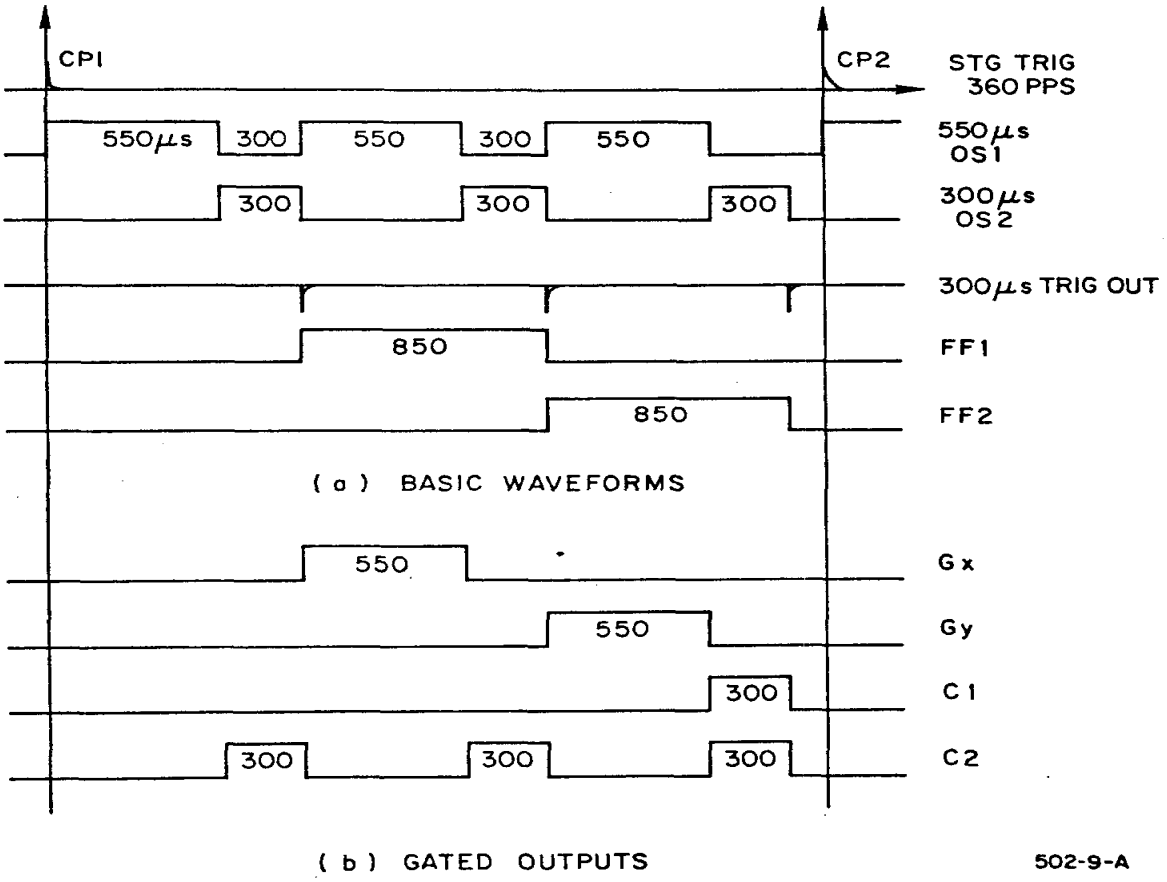


FIGURE 17 — TIMING WAVEFORMS

returned to its initial state to await the next STG pulse.

The operation of Fig. 16b is as follows (refer to the waveforms of Fig. 17a):

(1) FF1 and FF2 are initially in the zero state. The first OS2 trailing edge trigger enables AND gate 1, which in turn sets FF1 to the 1 state. AND gate 2 is inhibited, so that FF2 does not trigger.

(2) The output of FF1 passes through the OR gate to retrigger the OS1 - OS2 cascade.

(3) The second OS1 trailing-edge trigger resets FF1 to the zero state, which in turn sets FF2 to the 1 state. The output of FF2 passes through the OR gate to supply the second retrigger pulse; in addition, the change of state of FF2 inhibits AND gate 1 and enables AND gate 2 in preparation for the next pulse. At this point, FF1 is in its original zero state, and FF2 is in the 1 state.

(4) The third OS1 trigger enables gate 2 to reset FF2 to its original zero state, and is prevented from retriggering FF1 by the inhibited AND gate 1. Further operation therefore ceases until the arrival of the next 360-pps trigger pulse.

Figures 16c and 17b show the circuit and waveforms for the X and Y gates and the two different clamp pulses. Buffers are used after each AND gate, because the clamp transistors in some cases require drive currents as high as 30 mA.

8. Calibration Procedure

The calibration will be described very briefly before discussing the performance of the system. The procedure is as follows:

(1) The delay and gate widths are set to 2.0 and 2.5 μsec, respectively. The final setting of delay is done in the Klystron Gallery, since its value depends on the trigger-to-beam pulse delay in the injector, which is not yet firmly specified.

(2) The 550-μsec and 300-μsec one-shot delays are set to a nominal 2% accuracy using a properly calibrated oscilloscope.

(3) The output of the logarithmic amplifier is observed with the input signals at zero and with the offset jumper not connected. The jumper is connected in the direction required to make the baseline slightly negative. Only a small portion of the potentiometer should be required.

(4) A full scale simulated beam pulse is injected into Q, x and y inputs. The 10-volt, 2-μsec Q signal is centered within the gate pulse. Position outputs of $\pm$ 1 volt, and a Q output of -5 volts, should be obtained.

(5) The output of the final dc amplifier is observed and the Q input signal is changed in 10-dB steps from 0 to 60 dB. The threshold is adjusted to clip near 60 dB, so that the interval from 40 to 50 dB is the same as from 50 to 60 dB (cutoff).

(6) Observing the same point and with the input at -50 dB, trim capacitors are selected to reduce the $\bar{x}$ and $\bar{y}$ offsets to close to zero. (The same values are used in all circuit boards.) Then the jumper in each clamp is connected and the potentiometer adjusted to reduce the offset to zero.

(7) The dc amplifier gain is set to bring the maximum ℓn Q signal to 5.00 volts as measured with a suppressed-zero dc preamplifier (Tektronix Type Z). The dc amplifier bias is adjusted for a nominal zero-volt output.

8. The amplitude of positive and negative position signals is observed as the input level is changed over the full range. The maximum deviation from linearity over the range should be no worse than 10-15%. The signals are also observed as the input pulse width is changed from 2 to 0.2 μsec. A small nonlinearity in the ℓn Q signal will be seen, but the position signals should be essentially constant with changes in width.

The calibration is to be checked at 90-day intervals on a few selected units in order to study long-term drifts, such as may occur due to aging of the diodes in the logarithmic amplifier circuit, or due to changes in clamp transistor offsets.

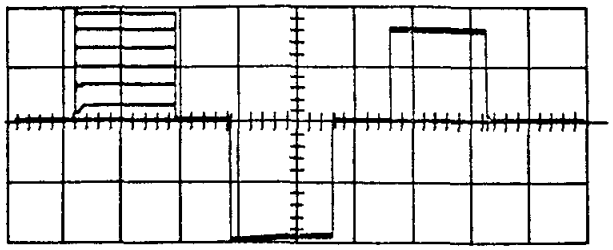
C. Performance Summary

1. ℓn Q Accuracy

The accuracy of the ℓn Q presentation is primarily a function of (1) logarithmic amplifier diode linearity and stability, (2) threshold setting accuracy and stability, and (3) variations in the beam pulse width.

The linearity of the CD 6611 diodes has been observed over many different units and, over the three-decade range, appears to be better than $\pm$ 2.5%. The main nonlinearity occurs near the bottom of the range, where clamp offsets and threshold nonlinearities become apparent. Needless to say, proper setting of the threshold is vital to good overall linearity. The output of a properly adjusted unit is shown in Fig. 18a.

The diode temperature stability is assured with the 70°C component oven. The effects of long-term aging at this juncture have not been observed. The diodes have been aged by the manufacturer at 300°C for 200 hours, so that any additional aging effects should take place slowly.



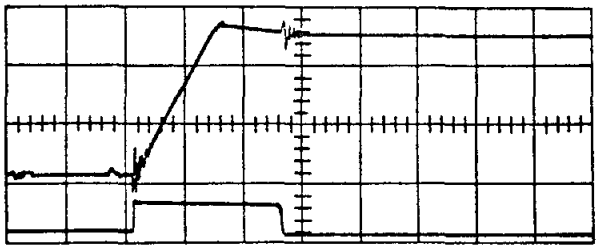
(a) ℓnQ, $\bar{x}$ and $\bar{y}$ Output

10 db steps of ℓnQ

0 to 60 db

ℓnQ = 5 volts peak

Note: $\bar{x}$ and $\bar{y}$ variations with ℓnQ amplitude

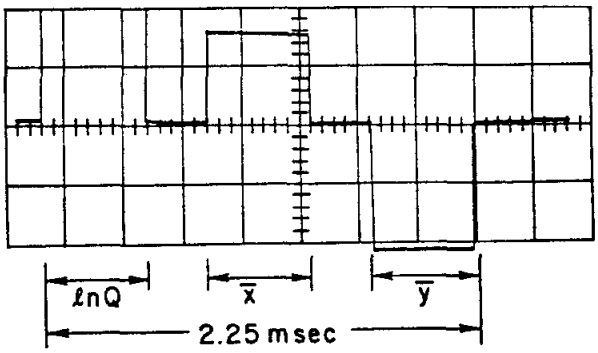


(b) Gated Integrator Input

Top - Integrated Signal

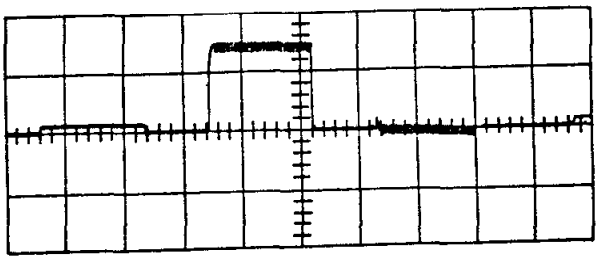
Bottom - Gate Signal

Horizontal = 1 μs / cm



(c) Position Signal Asymmetry

Output of Clamp Circuit



(d) Position Signal Offset and Noise @ ℓnQ = -50 db

Vertical = 2.5 V/cm

502-25-A

FIG. 18 - CIRCUIT WAVEFORMS

The threshold setting accuracy depends mainly on the stability of the dc amplifier, the temperature coefficient of the 6.8-volt zener diode, and the temperature coefficient of the uncompensated emitter-base junction of Q5, Fig. 12a. The dc amplifier output drifts about $\pm$ 3 to $\pm$ 5 millivolts from 0 to 60°C, which is negligible. The junction voltage has a negative temperature coefficient of about 2 mV/°C, which would cause a change of 120 mV over 60°C. Since the ℓn Q signal at this point is somewhat greater than 5 volts, the maximum error is +2.4%. (The error is positive because the junction voltage drop decreases with temperature.) If we consider that the calibration is made at 25°C ambient, the error from 0 to 60°C will range from – 1% to +1.4%, which is quite negligible in view of the logarithmic diode nonlinearity previously discussed.

Variations in the beam pulse width cause a different sort of error. Consider the gated integrator waveform shown in Fig. 18b. The integrator output ceases to rise at the end of the beam pulse, and some charge leaks off with the same time-constant before the gate closes. The decay slope is about 10 times lower because the initial voltages differ by about 10 times in the two cases. If the pulse width decreases, it is apparent that the same collected charge has longer to decay before the gate closes, which results in an error in ℓn Q. There is a slight compensating effect in that the integration is more linear for the narrower pulse, so that the initial value is higher. However, the net result is that for a pulse width of 0.2 μsec, the ℓn Q output will be about 4.5% lower than for a 2-μsec pulse containing the same charge.

2. Position Signal Accuracy

The errors in the position signal representation may be classified as either proportional or systematic. A proportional error is defined as an

uncertainty in the exact value of the beam position for a given measurement. A systematic error is defined as one which gives an erroneous indication of the sign of the displacement; this type of error is obviously the much more serious of the two.

Proportional errors arise from two causes: (1) the inherent nonlinearity of the logarithmic approximation, depending on the sign of the position signal; and (2) random nonlinearities in the logarithmic amplifier diode characteristics. The first results in a predictable error which is -13.1% for the positive maximum (same direction as Q) and +20.3% for the negative maximum (see Fig. 18c). This percentage error is a maximum for maximum position offsets and decreases as the beam approaches the central axis. The second factor results in random errors about a nominal value as the beam current changes; the effect is shown in Fig. 18a. From 0 to 40 dB, the total change is about 10%, and at -50 dB, about +25%. Since the maximum position signal represents 2.48 dB of the diode dynamic range, the above errors represent about 0.25- and 0.6-dB nonlinearities respectively. Because the diode characteristic is smooth, these errors should also decrease for smaller beam displacements.

Since the main purpose of the system is to determine when the beam center of charge is on the accelerator central axis, it is felt that the errors described above are perfectly tolerable. A significant systematic error, on the other hand, is completely intolerable. The major causes of systematic errors in the present system are the offset voltages in the transistor clamps, and leakages in the FET transistors. The offsets are quite stable with temperature, so that fixed offset bias adjustments can be relied upon at low levels. The FET leakage currents are practically negligible. Neither effect

is at all observable above $\ell n\ Q = -40$ dB.

The zero level for a properly adjusted unit at $\ell n\ Q = -50$ dB is illustrated in Fig. 18d. It is apparent that below this level, system noise will very soon pose a further limitation to the resolution of position.

A form of error not yet mentioned is that due to droop on the position signals. Because the position signals are so much smaller than $\ell n\ Q$ at the output of the logarithmic amplifier, the droop on $\overline{x}$ and $\overline{y}$ due to the $\ell n\ Q$ signal is magnified (Fig. 18c). Due to the fact that each sector signal is viewed at a different time through the multiplexing, another minor proportional error results.

It is worth noting that excessive droop on $\overline{x}$ and $\overline{y}$, and not on $\ell n\ Q$, is indicative of FET gate leakage in the Q integrator, whereas excessive droop on all three signals indicates a faulty FET in the coupling circuit which serializes $\ell n\ Q$, $\overline{x}$ and $\overline{y}$.

3. Sector-to-Sector Comparative Accuracy

The various kinds of errors and their relative importance have all been mentioned. They are summarized as follows:

(1) Nonlinearity in $\ell n\ Q$ due to diode characteristics.

(2) Temperature drift of threshold level.

(3) Temperature drift of zener voltage.

(4) Inherent asymmetry in position signals from the logarithmic approximation.

(5) Random errors in position signals due to diode nonlinearities.

(6) Offsets due to restoring clamps.

(7) Error in $\ell n\ Q$ due to pulse width variations.

(8) Error in multiplexed position signals due to droop.

(9) Noise.

It is noteworthy that so far as the comparative accuracy of the overall system is concerned, the only errors of significance are due to (1), (5) and (6). That is, any effect which is predictable, to the extent that it will be the same in all units along the accelerator, does not degrade the comparative accuracy of the system. The change of ℓn Q with pulse width, for example, is predictable and should affect all outputs by the same amount; hence the comparison of ℓn Q from sector-to-sector is still valid.

In all of the foregoing, of course, we have assumed perfect balance and linearity of the microwave system. In actual fact, this system has errors of its own which superimpose on the errors above to further degrade the overall performance. The most serious error in the microwave mixer is due to long-term drifts in the thermionic detector diodes.

This drift produces a systematic error in position – i.e., a fixed offset when the beam is, in fact, centered. This problem has been somewhat alleviated by incorporating remote-controlled switches which disconnect the microwave position signal, in order to observe the offset due to diode imbalance with just the reference signal applied.

It should be reiterated that the logarithmic presentation of ℓn Q is not, and is not intended to be, a highly accurate measurement of charge. Its principal utility lies in being able to display a wide dynamic range of charge, such as will be encountered with multiple beams, on a single 0- to 5-volt format. A maximum current pulse, followed immediately by a minimum current pulse, (-50 dB) can be displayed with equal facility, requiring no manual change of gain in the display system.

III. CHARGE MONITORING CIRCUITS

A. Functional Description

The charge monitoring portion of the system measures electron charge over a 60-dB range to a nominal accuracy of 1%. In the lower part of the range, the accuracy is limited by noise and 60-cycle pickup. A reversing switch at the input allows positron beams to be monitored also. Since the positron beam is in general $\approx$ 100 times weaker than the electron beam which produces it, only a limited dynamic range is required at the high-gain end.

The system (see Fig. 19) consists of a pre-integrator and preamplifier, which includes a droop compensation, followed by a gated, double RC integrator. After integration, the signal is amplified to a level between 2.5 and 5 volts, which is the optimum range for the FM telemetry system; it is then sampled and held for 2.25 msec. The gain of the system is controllable from the CCR in 6-dB steps, from 0 to 54 dB. In the case off interlaced beams of different amplitudes, one can increase the gain of the system in order to view the smallest beam, in which case larger beams will saturate the amplifiers. Of course, in order to view one particular beam, multiplexing must be provided between the FM receiver and the display.

The FM system is a hardwire link which has short-term drifts of less than 1%. Providing the overall calibration can be accomplished to sufficiently high accuracy, the system should be capable of comparing sector-to-sector charge to at least 1% over the top 18-24 dB of the range.

The main philosophy of design is first to amplify the signal as a pulse in a low-noise preamplifier, and then to gate the pulse into a double-RC integrator. The gate eliminates all noise from the system except that which occurs in a

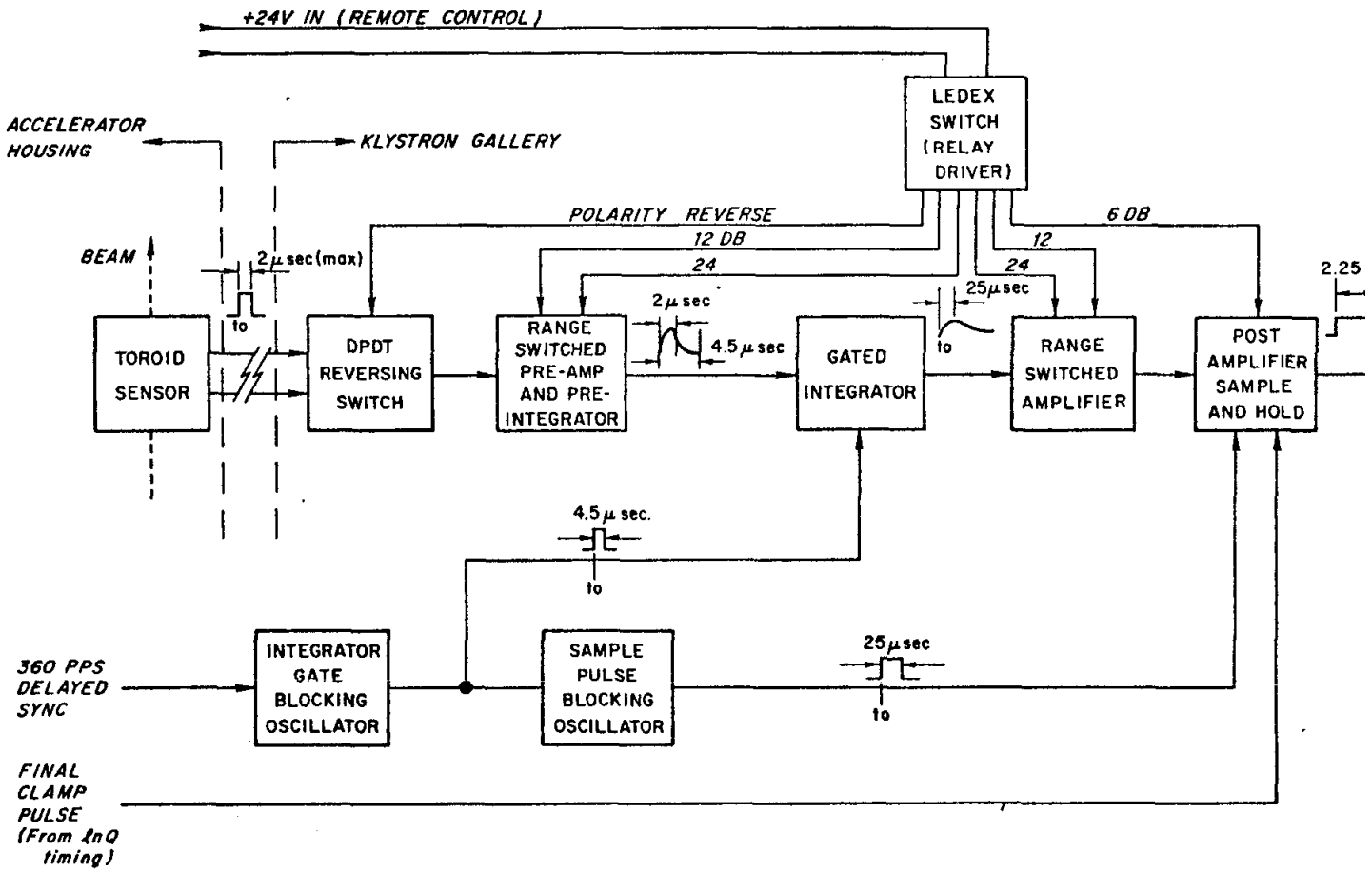


FIG. 19 - CHARGE MONITORING SYSTEM

4.5-μsec interval about the pulse. This is particularly important for eliminating 60-cps pickup, which would otherwise saturate the system at the maximum gain settings. The gate also eliminates the long trailing edge of the pulse, which could cause large errors in the integration.

The integrator itself produces a delayed peak, about 25 μsec after the beam pulse, the amplitude of which represents the pulse integral. The peak is allowed to decay, rather than being clamped as in the position monitor integrators. This is because the signal levels here are considerably lower than in the latter case, due to the higher accuracy of integration, and hence clamp offsets are much more objectionable. The sample-and-hold operation, therefore, is not performed until the integrator output has been amplified to its highest level, at which point clamp offsets are completely negligible.

Another major consideration is that in view of the remote location of the system, pulses must be processed without prior knowledge of the amplitude and width. Hence, as previously mentioned, the system must recover quickly from large overloads. Only if the integrated signal is kept in pulse form throughout the amplifiers is this problem relatively easily solved.

One additional requirement is that the system must operate in ambient temperatures between 0 and 60°C. Therefore, particular attention must be paid to the stability of amplifier gain, buffer output impedance, and any series resistances in the signal path.

B. Range Switching System

Changing the gain of the system in 6-dB steps from 0 to 54 dB is accomplished by switching gain in all three amplifier stages. Preamplifier noise and pickup limits the sensitivity at maximum gain settings.

The switching is accomplished using miniature dry reed relays to change an input resistor value; the relays are actuated through a Ledex stepping switch which is driven in turn via the CCR remote control system. The switching sequence of the various stages is as follows:

Step	Preamp	Stage 1	Stage 2	Gain (dB)	
1	0	0	0	0	
2	0	0	6	6	
3	0	12	0	12	
4	0	12	6	18	
5	0	24	0	24	
6	12	12	6	30	
7	12	24	0	36	
8	24	12	6	42	
9	24	24	0	48	e^-
10	24	24	6	54	
11	24	24	6	54	Polarity Reverse
12	24	24	0	48	e^+
13	24	12	6	42	
14	12	24	0	36	

The symbols e^- and e^+ indicate the ranges for electron and positron currents, respectively. Steps 11 through 14, which are duplicates of steps 10 through 7, allow measurement of positron beams to levels somewhat greater than 100 times the maximum electron beam.

A problem is encountered in range-switching the video amplifier: If the final output decreases enough to require an increase in the gain, it is in general not

known whether the decrease was due to a drop in beam intensity, or beam width, or both. Hence, if the effect were due to width, alone or in part, increasing the preamplifier gain could cause saturation. The problem is overcome with a pre-integrator, consisting of a small capacitance in parallel with the feedback path, which attenuates the narrower pulses to low amplitudes. This means that if the charge decreases due to a decrease in width, the pre-integrator assures that the amplitude is lowered in proportion. For the switching arrangement used, a time-constant of 0.6 μsec was found to be optimum. Two side benefits of the narrowing of overall bandwidth are that the preamplifier noise is reduced, and that precision wirewound resistors can be used without fear of degrading the bandwidth.

C. Circuit Design Details

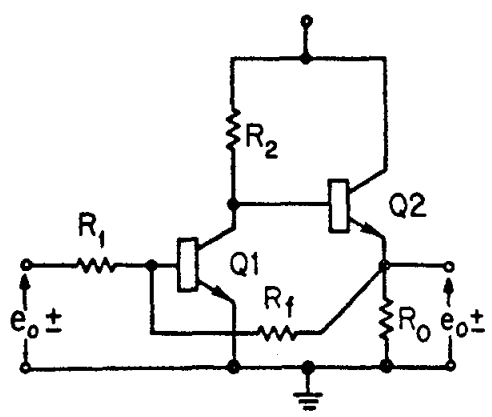
1. Preamplifier Design

The main requirements of the preamplifier are (a) low noise, (b) a high degree of gain stability, and (c) a provision for droop compensation. Figure 20 a shows the first preamplifier stage basic circuit; this stage has a gain of 10. Figure 20 b shows the gain-switched second stage; this same design is used in the remaining gain-switched stages. To increase the gain, the equivalent R_1 is changed by adding additional resistors in parallel. The addition of droop compensation to this basic circuit will be discussed later.

Both Figs. 20 a and 20b can be analyzed using the equivalent circuit of Fig 20 c. For Fig. 20 a the gain is calculated to be

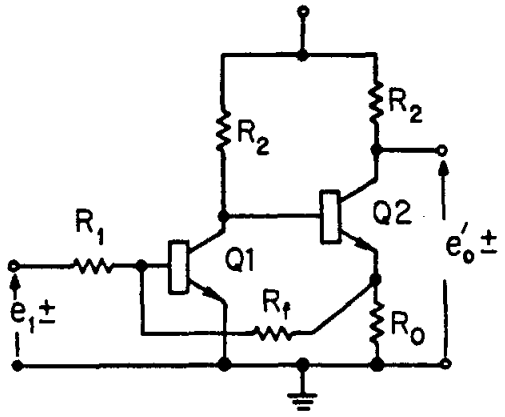
$$e_o = -\frac{R_f}{R_1} \frac{1}{1 + \dfrac{1 + R_f/R_1 + R_f/R_{e1}}{A_o}}$$

$$\approx -\frac{R_f}{R_1} (1 - \epsilon)$$



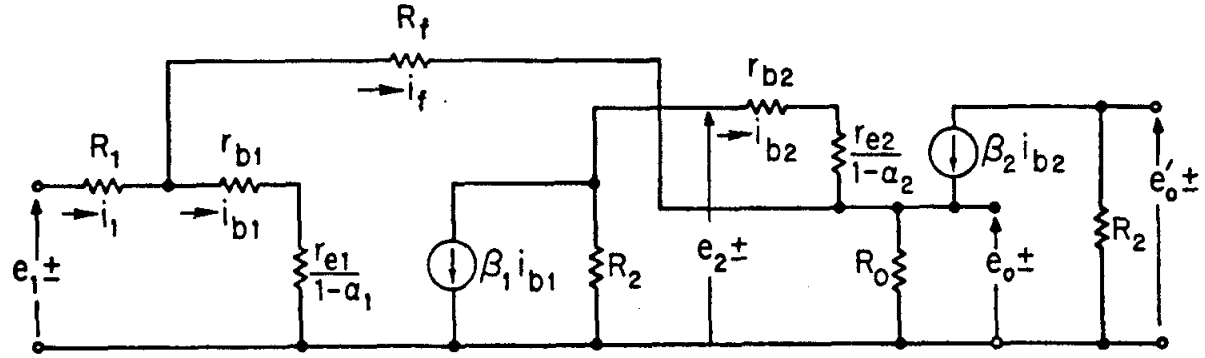
(a)

Single - stage
Inverting



(b)

Two - stage
Non - inverting



(c)

Equivalent Circuit

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FIG. 20 – AMPLIFIER CIRCUITS

where

e_o = output voltage

e_1 = input voltage

R_f = feedback resistance

R_1 = input resistance

$$R_{e_1} = r_{b1} + \frac{R_{e1}}{1 - \alpha_1}$$

$A_o = R_L/r_{e_1}$ = open loop gain of stage 1

$$\epsilon = \frac{1 + R_f/R_1 + R_f/R_{e1}}{A_o}$$

In the derivation, the following assumptions were made in calculating the term containing $1/A_o$:

$$R_{e2} = r_{b2} + \frac{r_{e2}}{1 - \alpha_2} \approx \beta_2 r_{e2}; \ \beta_2 >> 1$$

$$\left(\frac{1}{R_2} + \frac{1}{R_{e2}}\right)\frac{r_{e2}}{R_f} \ll \left(\frac{1}{r_{e1}}\right) .$$

Since the approximations enter only the error term, they affect second-order errors only.

The ϵ term is a small correction which must be added to the ideal gain, $A_c \approx R_f/R_1$. If high-stability external resistors are used for R_f and R_1, then the gain stability can be determined by a consideration of the variation of parameters in the expression for ϵ.

Extending the analysis further, the gain of Fig. 20b can be shown to be:

$$\frac{e_o'}{e_1} = \frac{R_f}{R_1}(1-\epsilon)\frac{R_2}{R_o}\frac{\beta_2}{1+\beta_2}\left(1+\frac{R_o}{R_f}-\frac{R_o}{A_o R_f}\right)$$

$$\approx \frac{R_f R_2}{R_1 R_o}(1-\epsilon)\frac{\beta_2}{1+\beta_2}\left(1+\frac{R_o}{R_f}\right)$$

$$\approx \frac{R_f R_2}{R_1 R_o}\left(1+\frac{R_o}{R_f}\right)\gamma(1-\epsilon)$$

$$= A_c \cdot \gamma \cdot (1-\epsilon) ,$$

where

$$A_c = \text{closed loop gain}$$

$$\gamma = \frac{\beta_2}{1+\beta_2}$$

$$\epsilon = 1+\frac{A_c + R_f/R_{e1}}{A_o}$$

Following the previous argument, the gain stability can be evaluated by a consideration of the term $\gamma(1-\epsilon)$.

a. Gain Stability. The maximum gain used in either stage is 10. Typical values for the first stage are as follows:

$$R_f = 10k\Omega, \quad R_1 = 1k\Omega, \quad \beta_1 = 320, \quad A_o = 1000$$

$$I_{c1} = 1/3 \text{ mA}, \quad r_e = \frac{25}{1/3} = 75 \text{ ohms}$$

$$\therefore \quad \frac{R_f}{\beta_1 r_e} = \frac{10,000}{320(75)} = 0.4$$

$$\therefore \quad \epsilon = 1 + 10 + 0.4 = 0.0114 \equiv 1.14\% .$$

Hence, the gain calculated by $e_o/e_1 = R_f/R_1$ will be 1.14% high.

The parameters of ϵ which change with temperature are r_{e1} and β_1. Over a 60°C range, $r_{e1} = kT/qI_e$ will increase by a factor of $360/300 = 1.2$; β_1 will increase approximately linearly by a similar amount. The new ϵ is then

$$\epsilon = \frac{1 + 10 + 0.4/(1.2)^2}{(1000)/(1.2)} = \frac{11.28}{833} = 0.035 \equiv 1.35\% .$$

Therefore, the incremental change is 0.21%, and the gain temperature coefficient is

$$\frac{\Delta A_o}{\Delta T} = \frac{0.21}{60} \ \%/^oC = 0.0035 \ \%/^oC$$

The stability of the second stage differs only by the factor $\gamma = \frac{\beta_2}{+ \beta_2}$. A 20% change in $\beta_2 = 320$ has a negligible effect compared with the variations already described. Note that the most significant effect is due to the variations in A_o caused by temperature changes in r_{e1}.

b. Noise. Since noise is a function of the source resistance (thermal noise), the amount of collector current (shot noise), and the β of the transistor (recombination noise), the main requirement of the transistor is that it exhibit a high β at a few tenths of a milliampere collector current. Also, for wideband operation, f_T shall be large. The transistor used, a 2N2484, has a β (min) of 320 below $I_c = 100 \ \mu A$. With source resistances of a few kilohms, a noise figure of better than 2 dB is achieved. The operating current of the first stage is typically 200 μA.

c. Droop Compensation. Figure 21 shows the droop compensation schematic and its equivalent circuit. The transfer function is

$$Y(s) = \frac{e_o(s)}{e_1(s)} = \frac{\beta R_L}{Z_{in}} ; \quad Z_{in} = R_s + \frac{\beta R_e + \beta sL}{\beta R_e + \beta sL} = \frac{R_s R_e + s(R_s + \beta R_e)L}{R_e + sL}$$

$$Y(s) = \frac{\beta R_L (R_e + sL)}{R_s R_e + s(\beta R_e + R_s)L} .$$

Assuming a low source resistance and $R_e >> r_e$, then $\beta R_e >> R_s$ and hence,

$$Y(s) = \frac{\beta R_L (R_e + sL)}{R_s R_e + s\beta R_e L} = \frac{\beta R_L}{R_s} \frac{(1 + s\tau_2)}{(1 + s\tau_1)}$$

where

$$\tau_2 = L/R_e$$

$$\tau_1 = \beta L/R_s .$$

Since $R_s = R_g + r_b + \frac{r_e}{1 - \alpha} \approx \frac{r_e}{1 - \alpha} \approx \beta r_e$, then $\tau_1 \approx L/r_e$; hence $\tau_1 >> \tau_2$ and in the region of interest,

$$Y(s) \approx \frac{\beta R_L}{R_s} \frac{1 + s\tau_2}{s\tau_2} = \frac{\beta R_L}{R_s} \left\{ \frac{\tau_2}{\tau_1} + \frac{1}{s\tau_1} \right\} .$$

The input pulse with droop is of the form

$$e_i(t) = e^{-\gamma\tau} ; \quad \gamma = \frac{L_T}{R_o} = \frac{\text{toroid inductance}}{\text{shunt resistance}}$$

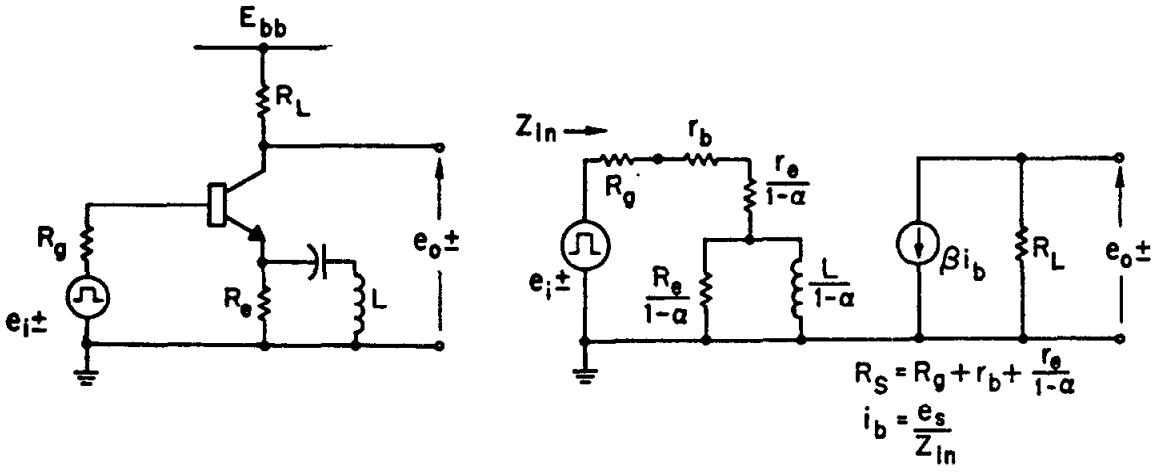
$$e_i(s) = \frac{1}{s + \gamma} .$$

Therefore

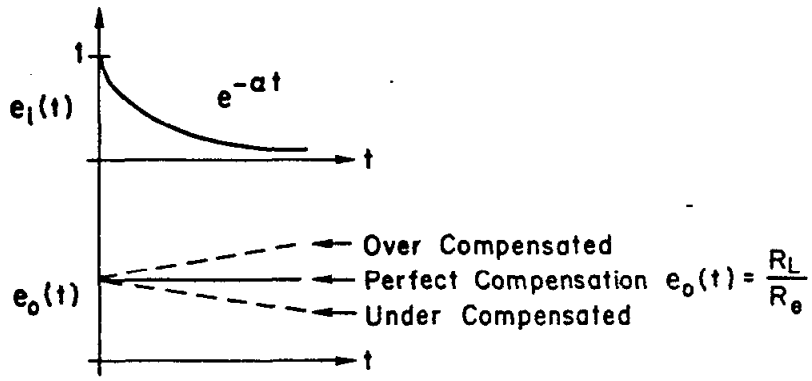
$$e_o(s) = \frac{\beta R_L}{R_s} \left\{ \frac{\tau_2}{\tau_1} \frac{1}{s + \gamma} + \frac{1}{\tau_1 s(s + \gamma)} \right\} .$$

Hence,

$$e_o(t) = \frac{\beta R_L}{R_s \tau_1} \left\{ \frac{1}{\gamma} + \tau_2 e^{-\gamma\tau} - \frac{1}{\gamma} e^{-\gamma\tau} \right\} .$$



(a) Schematic and Equivalent Circuit



(b) Waveforms

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FIG. 21 - DROOP COMPENSATION CIRCUIT

For perfect compensation, we must choose

$$\tau_2 = \frac{1}{\gamma}$$

$$\frac{L}{R_e} = \frac{L_T}{R_o}$$

where

L_T = toroid inductance = 1 - 2 mH

R_o = shunt resistance = 95 Ω .

In this case the output will be, for unity input,

$$e_o(t) = \frac{\beta R_L}{R_s \tau_1}\left(\frac{1}{\gamma}\right) = \frac{\beta R_L}{R_s}\frac{\tau_2}{\tau_1} = \frac{R_L}{R_e}$$

= low frequency gain of the stage.

The limitation to the width of pulse which can be compensated is related to the validity of the assumption that $\tau_1 >> \tau_2$. In our case, with $\tau_1 \approx$ 400 μsec, it can be shown that a 2-μsec maximum width pulse can be compensated to the order of 0.1% of its initial amplitude.

The droop compensation feature is easily added to the two-stage emitter-feedback amplifier described in the previous sections. The circuit is adjusted by injecting a square current pulse through the toroid calibrate winding, and changing the value of L while viewing the final output on an oscilloscope. Because of the slow rise time through the pre-integrator, a pulse width of 5 or 6 μsec must be used to properly observe the flat top.

2. Gated Integrator and Amplifier

The complete gated integrator, buffer, and range-switched amplifier circuits are shown in Fig. 22. The amplifier is identical to the basic two-stage circuit already described; it is included only to illustrate the general biasing and range-switching schemes, and will not be discussed further.

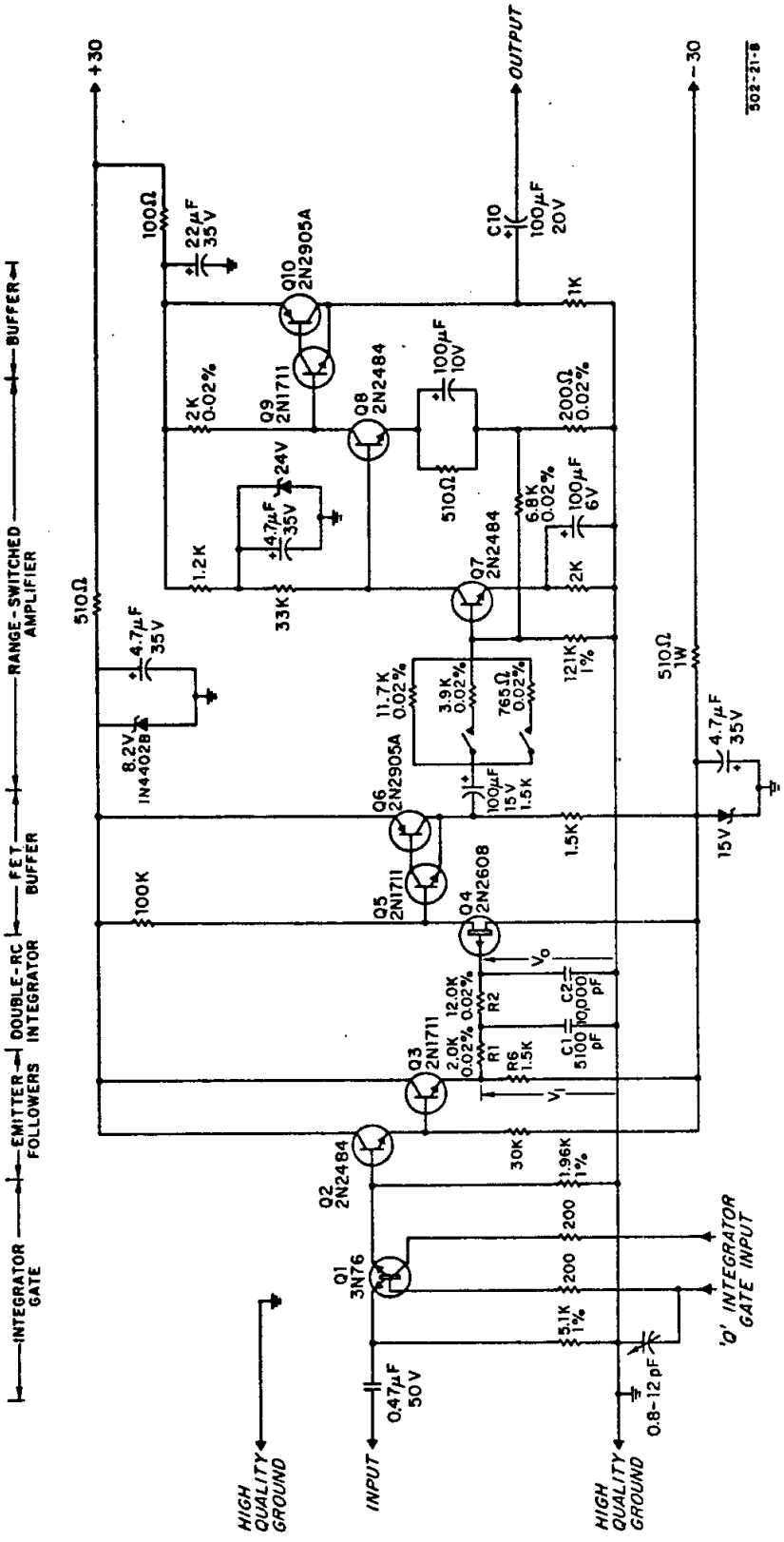


FIG. 22 — GATED INTEGRATOR AND AMPLIFIER

When turned on, the gate transistor Q1 forms a voltage divider with the 1.96-kΩ base resistor of Q2. This base resistor must be kept small to minimize the dc offset due to the flow of base current in Q2, and, at the same time, should be kept large to minimize the attenuation through Q1. With the values shown, the offset voltage due to base current is < 2 mV, which is 1.2% of the minimum pulse; at the same time, the drop through Q1 is < 0.1%.

The two-stage emitter-follower buffer provides an input resistance of > 1 mΩ, and an output resistance of < 3 ohms. Hence the R_{out} is about 1/1000 of the integrator input resistance, so that changes due to temperature should be considerably less than 0.1%.

The double-RC integrator is used first, to avoid the use of a restoring clamp, and second, to produce a relatively broad output pulse which can be sampled more easily than the output of a single RC integrator. Since the integrator reduces the peak input amplitude by about 50 times, the smallest integrated signal would be about 2 mV peak. Clamp offsets, on the other hand, are typically of the order of 1 mV and somewhat temperature sensitive, and hence would severely limit the linearity at low levels. Avoiding the use of a clamp, and allowing the integrator to discharge back through the emitter-follower, results in a nominal 1% accuracy down to levels where noise becomes the chief limitation.

For a rectangular input pulse, the integrator output is a critically damped waveform as shown. The first time-constant, R_1C_1, essentially controls the time to the peak, and the sensitivity of this time to pulse width variations. The

and

$$t_o = \ell n \left(\frac{1 - \exp s_2 T}{1 - \exp s_1 T} \right)^{1/(s_2 - s_1)}$$

where

$$s_1 = 1/s_2 \tau_1 \tau_2$$

$$s_2 = \tau_3 \frac{\left(1 \pm \sqrt{1 - 4\,\tau_1 \tau_2 / \tau_3^2}\right)}{2\tau_1 \tau_2}$$

$$\tau_1 = R_1 C_1 \,, \quad \tau_2 = R_2 C_2 \,, \quad \tau_3 = R_1 C_1 + C_2 (R_1 + R_2)$$

E_i = input amplitude

T = input pulse width

In the circuit shown, the nominal values are $\tau_1 = 10\,\mu$sec, $\tau_2 = 120\,\mu$sec, $t_o = 25\,\mu$sec, T = 2 μsec (max). The peak output e_o(max) is about 80% of that of a single stage integrator with $\tau = 120\,\mu$sec. For $\tau_1 \ll \tau_2$, the peak is $R_2/(R_2 + R_1)$ times the single-stage output.

The nominal accuracy of integration is 1% for the widest pulse, and better than 1% for narrower pulses. The peak shifts slightly for different pulse widths, but for our purposes, the error so produced is of secondary importance, since the same effect should occur in all units.

The errors due to tolerances of the RC time constants are difficult to assess. In general, an emphasis has been placed on the stability, rather than the accuracy, of components; the reason for this is that an adjustment in overall gain can compensate for differences in tolerances, providing that the system is stable. The precision wire-bound resistors, used in the amplifiers as well as the integrator, and the silver mica capacitors, have temperature coefficients of approximately $\pm$ 5 ppm/^{o}C in the range of interest. Hence, in principle,

one should be able to match two adjacent integrators as well as the second-order errors will permit.

3. Amplifier Range Switching

As has already been mentioned, the gain is increased by adding resistors in parallel with the amplifier input resistor. This is the most convenient component to change because it carries no bias currents. The resistors are calculated to change the gain by factors of 2, 4 or 16, corresponding to 6, 12 or 24 dB in voltage. The actual gains of the three main amplifiers at the 0-dB setting are: preamplifier, $\times 28.1$; Stage 1, 5.81; Stage 2, 6.95 (nominal). The last stage is adjustable in order to compensate for toroid, integrator, and amplifier gain tolerances from unit to unit.

The relays used to switch in the parallel resistors are actuated through a reversible, motor driven rotary selector. One deck of the selector switch is attached to a resistance divider which is biased with a fixed voltage; the output of the divider, a function of the switch position, is displayed on a meter in the CCR console.

Each of the remaining decks drives one of the relays in the amplifier chain. The decks are wired internal to the switch housing to minimize the number of output connections; the switching logic has already been described in Section III. B.

4. Sample-And-Hold Circuit

The complete sample-and-hold circuit, together with the final amplifier and buffer, is shown in Fig. 23. The circuit differs from the previous gated integrators only in that it has a short time-constant, 0.68 μsec, and that it is direct-coupled from the final buffer. The short time-constant is desirable in order to realize the full output of the buffer, with a minimum of timing uncertainty. The small capacitor is possible because the signal is always between 2.5 and 5 volts

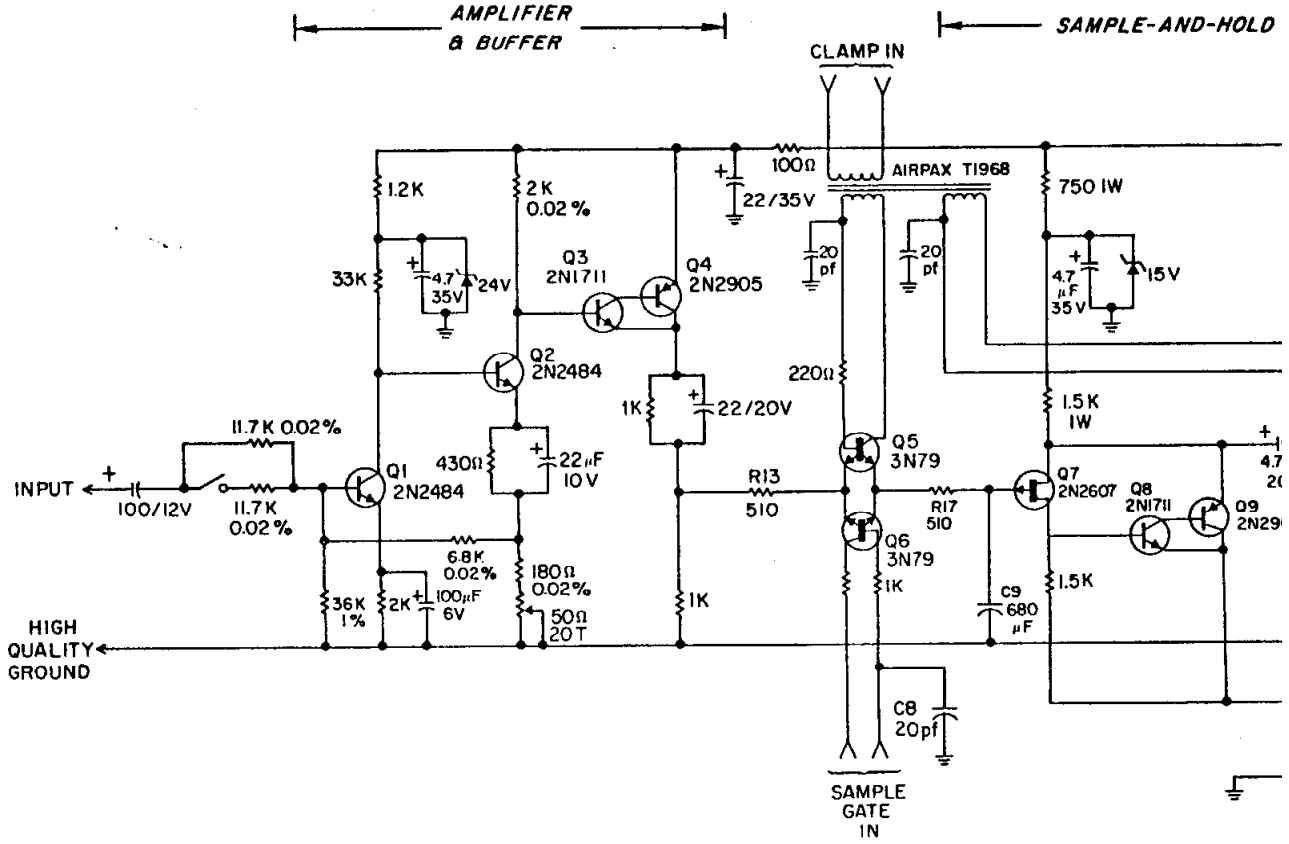


FIG. 23 - SAMPLE-AND-HOLD CIRCUIT

at this point, so that the FET leakage current can cause no more than a 0.1% droop on the pulse.

The output coupling time-constant to the FM transmitter causes a nominal 0.5 % droop on the signal. Part of the reason for having a gain control is to be able to equalize the CCR multiplexer outputs in the presence of this droop. The value of the droop itself is not as important as its stability; here, we are forced to accept the errors produced by changes in the capacitance with temperature. For example, a 20% change in capacitance would cause a 0.2% error if the pulse were being sampled near the end of the hold period.

5. Timing Circuits

The timing circuit for the linear Q system consists of two cascaded blocking oscillators which generate the integrator and sampling gates (Fig. 24). The cascade is triggered from the delayed gate of the position monitor timing board. The first of the two blocking oscillators is identical to those used in the position timing circuits.

The basic operation of the blocking oscillator is well known, although the detailed analysis is quite complicated due to the non-linear operation of the magnetic circuit. It will only be pointed out that in the case at hand, the L/R time-constant associated with the load circuit is so long that the time duration of the output pulse is essentially controlled by the L/R of the emitter circuit. In the first unit, which uses a 4:1 stepdown ratio from collector to emitter, the inductance of the emitter winding is

$$\frac{L(\text{primary})}{(N_2/N_1)^2} = \frac{200(10^{-6})}{16} = 12.5(10^{-6})\ \text{H}$$

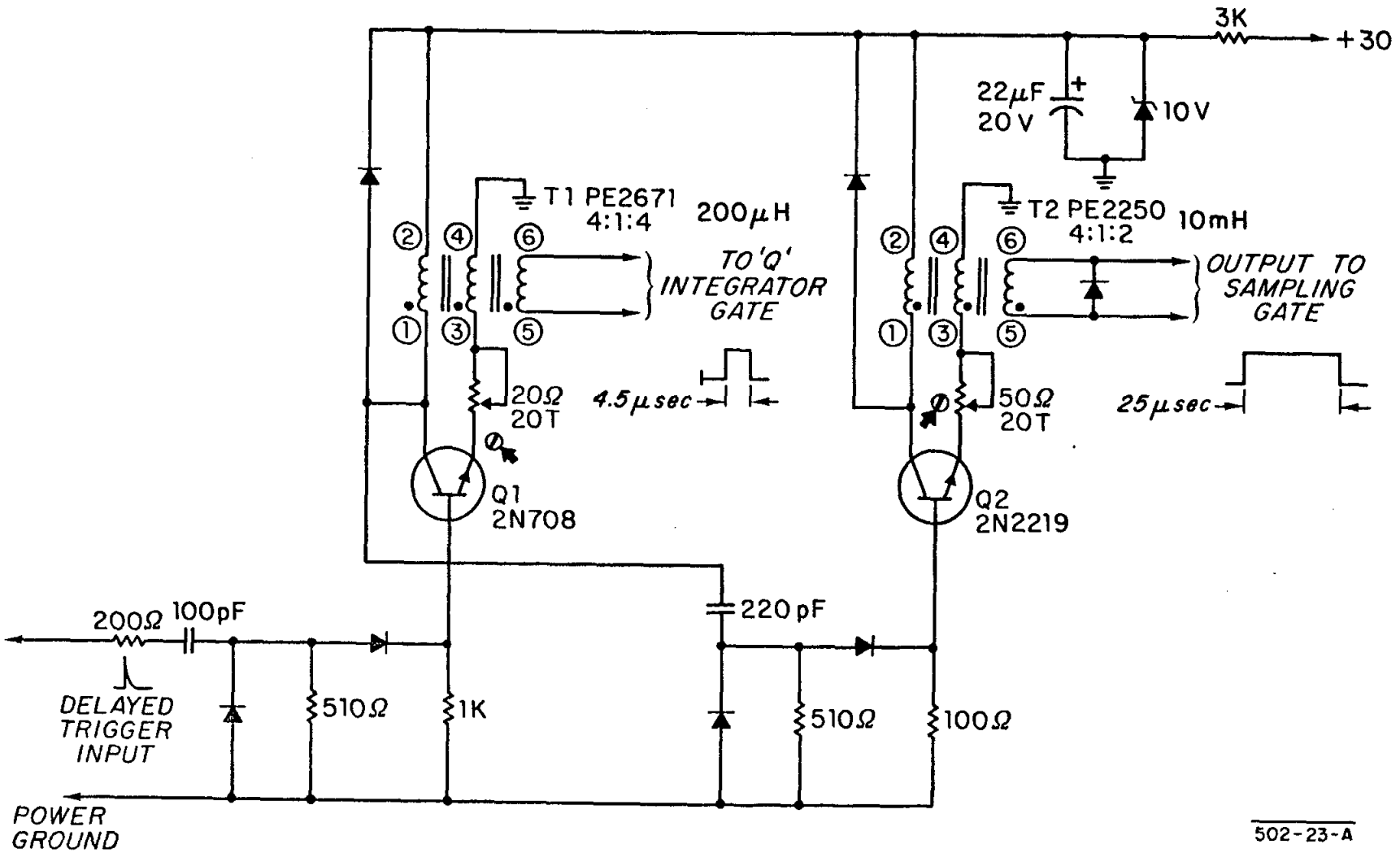


FIG. 24—TIMING CIRCUIT

The shortest pulse is determined by the maximum resistance in the emitter circuit, which is approximately 20 ohms; hence

$$\tau_{min} = \frac{L}{R} = \frac{12.5(10^{-6})}{2} = 6.25\ \mu sec$$

A similar calculation for the 25-μsec sampling gate oscillator yields

$$\tau_{min} = 12.5\ \mu sec$$

$$\tau_{max} = 312\ \mu sec$$

In the latter case, the time constant is so long that, in practice, saturation of the transformer core prevents the pulse from extending much beyond 50 μsec.

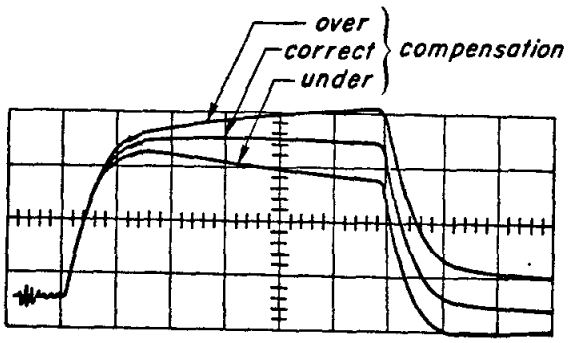
6. Calibration Procedure

The calibration procedure will be outlined very briefly before describing system performance. The steps are as follows:

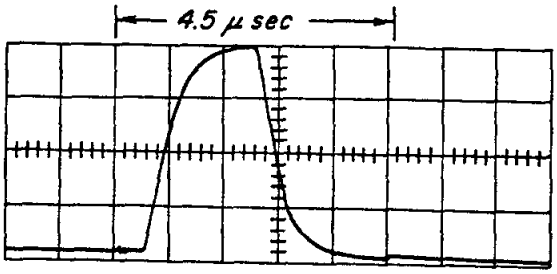
(a) A current pulse of known amplitude and duration is injected into the calibrate winding of the toroid. The amplitude and width are measured on an oscilloscope using a calibrated suppressed zero dc preamplifier. The time-base of the oscilloscope should be calibrated to better than 1% using a time-interval counter. The absolute value of the charge pulse need not be known to better than 1%, but repeatability should be 1%.

(b) With the pulse widened to 5 or 6 μsec, and the gain of the system at 0 dB, the compensating inductance is selected to produce a preamplifier output as shown in Fig. 25 a.

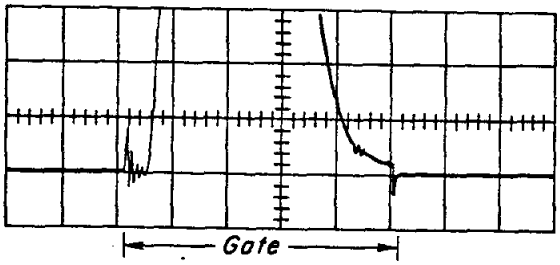
(c) The pulse is narrowed to 2.0 μsec, accurately measured, and its amplitude set to correspond to a beam current of 100 mA (380 mV out of the toroid). The pulse is adjusted within the integrator gate as shown in Fig. 25 b and 25 c. The corresponding integrator output is shown in Fig. 25 d.



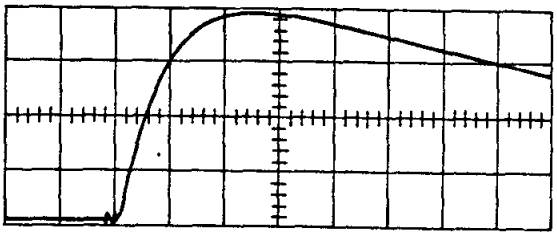
(a) Preamp Output
V=10V Peak (compensated)
H=1 μsec/cm



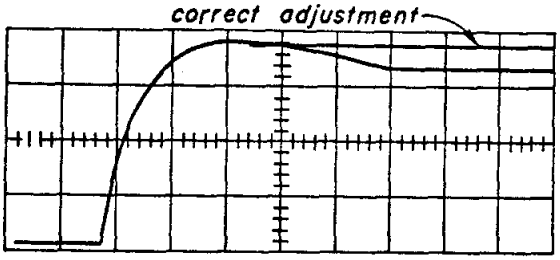
(b) 2 μsec Wide Gated Pulse
V=10V Peak
H=1 μsec/cm



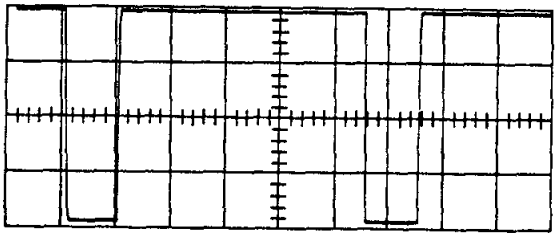
(c) 2 μsec Gated Pulse Baseline
V=0.2V/cm ≡ 2%/cm Vmax
H=1 μsec/cm (Vmax=10V)



(d) Integrator Output
V=0.11V (V_{in} = 10 Vmax
H=10 μsec/cm



(e) Sample-and-hold Output
V=5V maximum
H=10 μsec/cm



(f) Final Output to FM
V=5V maximum
H=0.5 msec/cm

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FIG. 25 - CIRCUIT WAVEFORMS

(d) With the signal temporarily removed, and the gain of the system at maximum, the output noise and offset levels are observed. The noise should be about ± 100 mV peak-to-peak; the offset is adjusted for a minimum with the integrator gate trimmed capacitor.

(e) With the signal as in (c) reapplied, and the gain at 0 dB, the sampling gate is adjusted to maximize the final output as shown in Fig. 25e. The gain of the final amplifier is then adjusted to give a final output of 5.00 volts at the 0-dB setting (Fig. 25f).

(f) Finally, the gain is checked over the entire range by introducing 6-dB steps of attenuation in the signal path, each time increasing the gain by 6 dB and comparing the final output with 5.00 volts.

D. Performance Summary

In order to observe the system stability, a prototype unit was cycled over a 0-60°C range in a temperature chamber. From the results, the comparative accuracy of the complete system is inferred.

During the tests, the input pulse amplitude was monitored using a zero-suppressed dc preamplifier (Tektronix Type Z); the pulse width was monitored using a time-interval counter with a resolution of ±1 nsec (El Dorado Model 793). The accuracy of measurement with the Z-unit varies between ±0.5% and ±0.1%, depending on the range being used. The test results are summarized below:

(1) The overall gain change from 0-60°C was +1.2%. This change is attributed to an increase in transistor β with temperature. The effect is predictable and should occur in the same direction in all units.

(2) The nonlinearity of gain over the normal 2.5- to 5-volt output range was about +0.5%. This is attributed to the fact that the emitter-follower output impedances decrease slightly with large positive signal

levels, resulting in less attenuation from base-to-emitter. The net change can be accounted for by the presence of several emitter-followers in the circuit. Again, the result is predictable and, to first-order, should be the same in all units.

(3) The change in output of the integrators as a function of pulse width was measured for widths of 2 μsec and 0.2 μsec. As expected, the output was approximately 1% higher for the narrower width.

(4) The accuracy of the gain steps was monitored by introducing 6-dB steps of attenuation in the signal path, then increasing the gain by a similar amount to obtain the same 5-volt output as before. The attenuator which was used is specified at $\pm 0.5\%$ absolute accuracy; the accuracy per step is inferred to be $\pm 0.2\%$ as measured on the 10-volt range of the Z-unit.

Typical accuracy of the gain steps appeared to be $\pm 0.5\%$ maximum. Often it was difficult to resolve the differences due to drifts in the pulse amplitude and width, and slow zero drifts of the Z-unit. Usually several readings had to be made at each setting in order to assure that the system was stable during the measurement.

The same prototype unit was later installed in the Klystron Gallery. The noise level observed was $\pm 2\%$ of full scale on the most sensitive range. The dc offset at the final output was less than 10 mV on a 5-volt scale, or 0.2%. This offset can be calibrated out in the CCR display system, and hence is not a source of error.

The comparative accuracy of large numbers of units has not yet been observed. Due to the dispersal of the system, each unit is being calibrated in situ, which involves being matched to a particular toroid. It is expected that

a measure of the system stability and calibration accuracy will be obtained when the electron beam is sent through a number of units at once. Because it is hoped to maintain the loss in charge along the machine to the order of 1%, random inaccuracies between adjacent units, of this same order of magnitude, should be readily apparent at the CCR display. At the present time, it is felt that the chief uncertainty in calibration is in the accuracy of the amount of charge being injected into the calibrate winding.

IV. CONCLUSIONS

The position monitoring system described appears to meet its major design objective of reliable, pulse-to-pulse operation over a 60-dB range of charge.

The ℓn Q information, which is primarily useful for monitoring interlaced beams of widely different charge, is nominally ±5% accurate.

The position signals have maximum proportional errors of +13.1% and -20.3% for the largest signals; these errors decrease as the beam approaches the wave-guide central axis. The zero discrimination error of the position signals is a nominal ±0.2 mm over the top 40 dB of range, exclusive of the microwave diode imbalance. The useful range of position measurement extends to -60 dB.

The main limitations in the circuitry are the offset voltages of the dual emitter transistor clamps, the low-level bandwidth and noise of the logarimithic amplifier, and the linearity of the logarithmic diodes. Since limits are approached in several of these directions simultaneously, extending the dynamic range appears difficult without relaxing the speed of operation. Alternatively, to increase the speed, as would be required for a higher machine repetition rate, the dynamic range would have to be relaxed because of the increased difficulty of clamping the large buffer coupling capacitors.

Generally speaking, it is felt that the technique of using gated integrators with clamped ac outputs, and serial normalization in a logarithmic amplifier, has been exploited to near the optimum within the required speed of operation.

The linear charge monitoring system has been shown to operate reliably over a wide temperature range to the required 1% accuracy. Within the resolution of the measuring instruments, it appears that the system is capable of sector-to-sector comparison of charge to better than 1%, at least over the top

24 dB of range. Noise and pickup represent errors of ±2% on the highest gain setting. Difficulties in calibration, and the ±1/4% accuracy of the combined FM telemetry and multiplexer systems, pose the main limitations to sector-to-sector comparative accuracy.

In view of its relatively low-noise and wide-dynamic range, the system is also capable of low-level current detection. For example, an 80-dB range of charge can be detected with a minimum signal-to-noise of 2.5/1; the lower level is equivalent to a peak charge of 20 picocoulombs. Thus, the system may be useful as an aid to steering very weak beams, such as ordinarily fall below the cutoff threshold of the position monitoring system.

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