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Electronics for the BaBar Central Drift Chamber*

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Abstract

The central drift chamber for the BaBar detector at the SLAC B-factory is based on a hexagonal cell design with 7104 cells arranged in 40 layers and drift gas Helium:isobutane (80%:20%). Performance optimization and integration requirements led to an electronics design that mounts the amplifier-discriminator and digitizing circuitry directly on the endplate. High channel density is achieved using a 4-channel custom amplifier-discriminator IC and an 8-channel custom CMOS TDC/FADC IC on a single circuit board. Data read from the front ends are multiplexed on 4 fiber optic links, and prompt trigger data are sent out continuously on 24 links. Analysis of cosmic ray data demonstrates that the electronics design meets the performance goals for the BaBar drift chamber. The final electronics were installed on the drift chamber in July, 1998. Installation of BaBar on beamline is scheduled for March, 1999.

I. Introduction

The PEP-II B-Factory is completing construction and commissioning at Stanford Linear Accelerator Center. It is designed to deliver high luminosity colliding e^+e^- beams at energies of 3.1 and 9 GeV to study the violation of CP symmetry in B^0 mesons. The BaBar detector[1] has been designed to fully exploit the physics potential of PEP-II. The detector design is shown in Figure 1. From the beampipe outward, the detector includes a silicon strip vertex detector, drift chamber central tracker, ring-imaging Cerenkov detector, CsI crystal calorimeter, 1.5 T superconducting coil and a flux return instrumented with resistive plate chambers. The central drift chamber[2] provides charged-track reconstruction, particle identification using dE/dx and prompt hit information for a charged-track trigger. This note describes the drift chamber electronics designed to provide this functionallity.

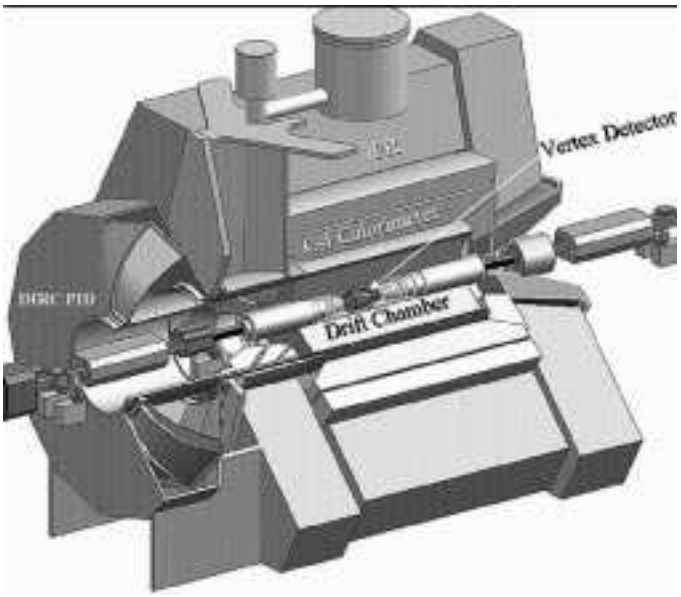

Figure 1: The BaBar detector at PEP-II.

The drift chamber is cylindrical with a 24 cm inner radius, 81 cm outer radius and total length 276 cm. The rear endplate is a flat aluminum plate 2.4 cm thick. The forward endplate is the same except thinned to 1.2 cm from a radius of 47 cm to the outer radius. Due to the forward boost from the asymmetric beam energies, the chamber is positioned so the beam interaction point is displaced from the chamber center by 36.7 cm towards the rear endplate. The inner cylinder is 1 mm Be within the fiducial region of the detector, the outer cylinder is two carbon fiber layers sandwiched around a Nomex core. A hexagonal small-cell design is used, arranged in ten superlayers of 4 layers each. Superlayers 1, 4, 7 and 10 are axial, and the others are alternating by roughly $\pm 4^\circ$ stereo. There are a total of 7104 cells.

Signals are read from the rear end of the drift chamber only. Accelerator beamline design and requirements on containment of the solenoidal field made it difficult to design a system with a large number of cables coming from the rear endplate. As a result, a design was pursued that has all the amplifying, digitizing and readout electronics located directly on the rear endplate. The electronics remains outside the fiducial region of calorimeter (due to the forward boost, the BaBar design has only barrel and forward calorimeters, no calorimeter in the backward direction).

II. Design Requirements

The gas mixture selected for use in the BaBar drift chamber (Helium 80% Isobutane 20%) represents an optimization of position and charge measurement resolution while maintaining low mass to minimize the multiple scattering contribution to momentum resolution. The electron drift velocity in this mixture is unsaturated and varies with electric field. At nominal operating anode voltage (1960 V), the drift velocity in the middle of the cell is roughly 25 μm/nsec. The lorentz angle in the 1.5 T magnetic field is predicted to be around 16° and the total drift time is about 600 nsec.

Resolution over much of the cell is dominated by ionization statistics (ionization studies predict roughly 21 clusters/cm). Optimal spatial resolution near the sense wire is obtained by minimizing the threshold on the timing measurement of the leading edge of ionization arriving at the wire. Monte Carlo studies suggest a threshold of <3 electrons result in a mean cell resolution that meets BaBar resolution goals of 140 μm average over the cell.

The predicted resolution for dE/dx is around 7% for a minimum-ionizing track traversing the chamber at a right angle to the wires. Monte Carlo studies have shown that slow shaping of the charge signal followed by digitization with a bi-linear 15 MHz FADC (described below) satisfies the resolution requirements and has adequate dynamic range.

The charged trigger design operates on a clock that is 1/16 of the BaBar system clock (59.5 MHz). The drift chamber is required to send a snapshot of the chamber hit occupancy once every tick of the trigger system clock (269 nsec).

Finally, the drift chamber electronics must communicate to the BaBar data acquisition system[3] using a standard interface. This structure requires pipelining the digitized data for the level 1 trigger latency time and readout through multiple event buffers and fiber-optic links to the standard BaBar readout module (ROM). Four event buffers insure deadtime of $<1\%$ at the design trigger rate of 2 kHz at 10 times the expected machine-induced background occupancy.

III. Electronics Design

Mounting the digitizing electronics directly on the rear endplate reduced the number and size of cables coming from the endplate but put significant demands on 1) the electronics channel density and 2) the mechanical integration of the electronics and associated cooling onto the rear endplate. The high channel density was addressed largely by the use of two custom integrated circuits described below. The mechanical integration made use of a 16-fold azimuthal symmetry imposed on the cell arrangement that allowed instrumentation of each 1/16 wedge with only 3 flavors of electronics enclosures (front end assemblies, FEA), mounted on radial bars that carry the water cooling.

Figure 2 shows a schematic of the electronics of a 1/16 wedge of the chamber endplate. The HV boards provide the anode and field high voltage and are the signal interface between the wire feedthroughs on the endplate and the front end assemblies. Front end assemblies contain amplifier-digitizer boards with the custom amplifier and digitizer ICs and a readout interface board. Event data readout and FEA configuration are done through four data I/O modules (DIOM), which communicate to the ROMs via 4 fiber-optic control and data link pairs. Trigger data are collected and sent to the trigger system in 8 trigger I/O modules (TIOM) using 24 fiber-optic links. The sections below describe the various parts in more detail.

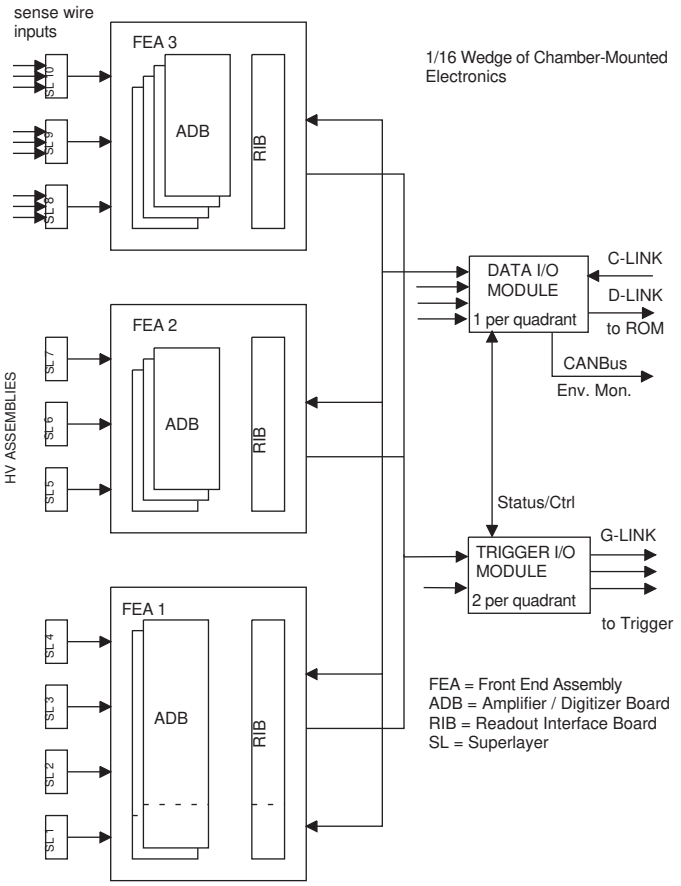

Figure 2: Block diagram of drift chamber electronics for a single 1/16 wedge on the rear endplate.

A. HV Assemblies

The high voltage assembly is a two-tiered board that provides anode and field shaping voltages to the feedthroughs on the chamber endplate and routes the sense wire signals to a front end assembly connector. Each HV assembly covers

12-18 cells in a 4-layer superlayer. Low-insertion-force jacks plug on the feedthrough crimp pins that hold the wires in place. The lower board distributes the anode voltage to each sense wire (1960 V) and guard voltage (340 V) to field wires at the superlayer boundaries. In addition, layers 1 and 40 have field wires at 880 volts to isolate them from the inner and outer wall. Other field wires are grounded to the endplate through conducting feedthroughs. The anode current is limited with 5 MΩ resistors (1 MΩ on superlayer 1) and a 220 pF capacitor is used for HV isolation. There is filtering on each HV board.

High voltage is supplied using a CAEN SY527 HV mainframe[4]. The A934 plug-in module provides 40 μA current per channel. HV boards are daisy-chained together segmenting superlayer 1 in 8 azimuthal sections and the other superlayers in 4 sections.

B. Front End Assembly

An inner radius front end assembly is shown in Figure 3. It is a wedge-shaped aluminum enclosure that contains 2, 3 or 4 amplifier-digitizer boards and a readout interface board that controls the readout. The amplifier-digitizer board is built around two custom ICs described below.

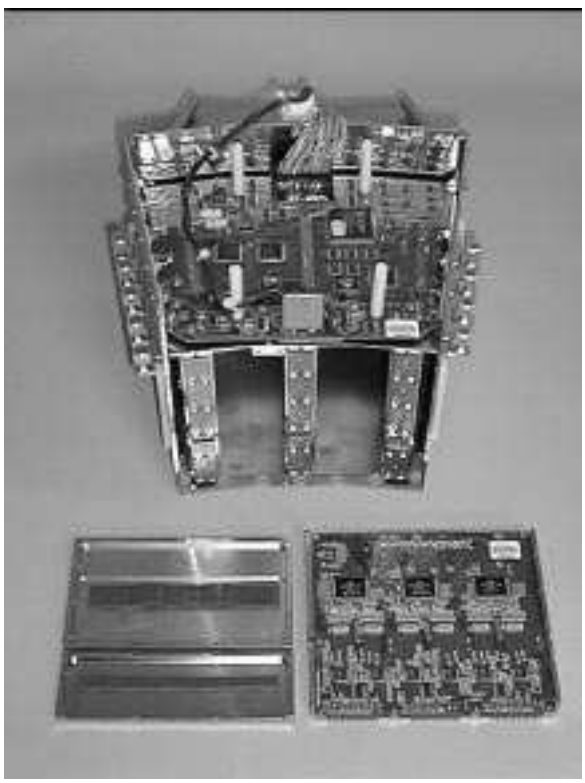

Figure 3: Front End Assembly (FEA) with top and side removed to show three amplifier-digitizer boards (inside their shields) and the readout interface board. In the foreground is an amplifier-digitizer board with the shields removed. This FEA is a type that fits in the middle slot of a wedge.

1) Amplifier IC

The drift chamber amplifier chip[5] is a semi-custom bipolar integrated circuit containing 4 channels per 48 pin package. Each channel has a front-end transimpedance amplifier stage with feedback resistor and open-loop gain chosen to provide 420Ω termination impedance for the sense wire. This stage feeds two separate legs: 1) a high-bandwidth discriminator with adjustable threshold for leading edge timing and 2) a slow-shaped output for charge digitization. The bandwidth at the discriminator input is roughly 50 MHz at the high end and a high-pass filter limits the low end to 5 MHz. The discriminator produces a differential output corresponding to time over threshold plus 40 nsec. The slow-shaped differential analog output has a nominal bandwidth of 1.5 MHz. The chip also contains an internal calibration circuit. Charge can be injected on a 3 pF capacitor on the input of each channel controlled by a voltage input, a strobe and independent selection of each channel.

2) Digitizer IC

Leading edge timing and charge digitization are done in a custom 8-channel CMOS integrated circuit called the ELEFANT chip[6]. A schematic of one channel is shown if Figure 4. The slow-shaped signal from the amplifier IC is digitized using a 15 MHz 6-bit FADC. Access to the top, middle and bottom of the FADC resistor ladder allow operation with two ranges. This feature is used to extend the dynamic range to 7 bits. The arrival time of the amplifier chip discriminator output is recorded with a TDC that uses a 6-bit vernier to measure the time within each FADC clock cycle. If a discriminator hit occurs, the 6-bit vernier time overwrites the 6-bit charge information and the 7th bit is set to flag this sample as a TDC hit. To prevent overwriting the leading charge information, the FADC charge samples are delayed by one sample. Additional late-arriving ionization will produce TDC hits that leave gaps in waveform which must be interpolated in the integration to determine the charge. Figure 5 shows several sample waveforms from cosmic rays in the drift chamber.

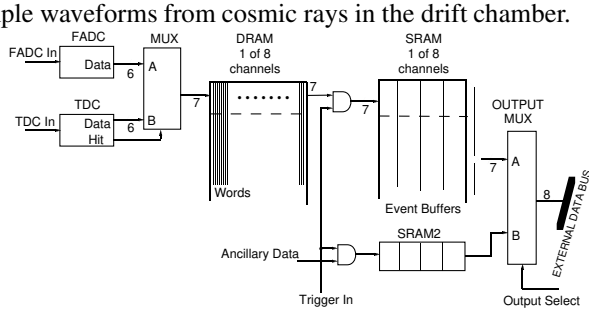

Figure 4: Block diagram of single channel of ELEFANT chip.

Following digitization, the data are stored in a digital pipeline for the Level 1 trigger latency period (∼12 μsec). After a level 1 trigger, the 32 samples at the end of the pipeline are transferred to one of four possible event buffers. Also stored with the data are a trigger time, a trigger tag and a hit flag byte that indicates which, if any, channels had hits. The hit flag allows sparse readout of only the hit channels. In addition, the ELEFANT provides hit information each sample on 8 output lines for use in defining a prompt track trigger. The definition of a hit in the hit flag and in the trigger output is selectable as either the presence of a TDC hit within

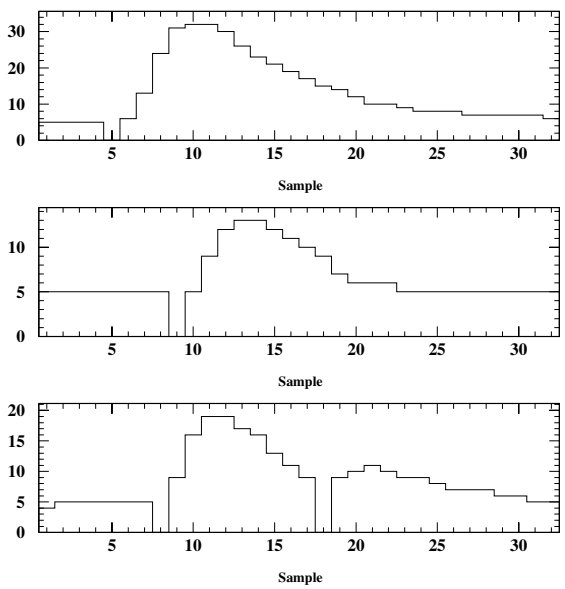

Figure 5: Sample FADC waveforms from cosmic ray data.

that sample period or an increase in the FADC value above a programmed threshold relative to the value two sample periods earlier.

3) Circuit Boards

Pairs of 4-channel amplifier chips feed signals to the 8-channel ELEFANTs on the amplifier- digitizer board (Figure 3). The inner radius Front End Assembly covers superlayers 1-4 and has two amplifier-digitizer boards, each with a total of 64 channels. Three 48-channel boards are used in the middle FEA to read out superlayers 5-7 and four 48-channel boards in the outer FEA read out superlayers 8-10.

Eighty-pin and 100-pin connectors on the amplifier-digitizer board interface it to the readout interface board (RIB) described below. The RIB provides configuration data, DAC voltages and readout control sequences and receives event and trigger data. FPGAs on the amplifier-digitizer boards down-sample the ELEFANT trigger data from 15 MHz to the 3.7 MHz trigger clock rate then send the data to the RIB.

Separate aluminum shields fit over the amplifier section and digital sections of the boards. These shields serve to isolate the sensitive amplifiers from the digital noise generated by the ELEFANT and associated readout signal traffic. In addition, heat conducting foam on the inside of the shields presses down on the chips and takes heat out into the shield and through the FEA enclosure to the radial cooling bars.

The readout interface board is a wedge-shaped board that receives commands de-multiplexed from the fiber-optic link by the data I/O module described below and performs the requested operation, either writing/reading configuration registers or initiating the readout of event data from the ELEFANTs. In an event read request, FPGAs read out each board in parallel into local FIFOs, then, following a grant signal from the DIOM, begins sending data up to the DIOM for multiplexing on the fiber-optic link to the ROM. In addition, the RIB responds to a number of other commands: 1) Clear Readout - reset the event buffer read and write pointers, 2) Sync - re-syncronize system clocks, 3) L1 Accept - forward level 1 trigger signal and trigger tag to ELEFANTs, and 4) Cal Stobe - strobe calibration circuitry. Configuration registers include DACs for setting the discriminator threshold, the calibration charge, and the top, middle and bottom taps of the FADC resistor ladder.

The RIB also does further multiplexing of the trigger data, sending the data up to the trigger I/O module serialized on 8-12 lines running at 59.5 MHz clock rate.

C. Data Acquisition and Trigger Interfaces

The Data I/O Module (DIOM) sends and receives data from the BaBar Readout Module (ROM) via a pair of fiber-optic links. The transmitter/receiver pair is a Finasar FTR8510[7], interfaced using HP Gigalink (HDMP-1022, 1024)[8] serializer chips. The function of this module is to 1) receive command and control signals over the command fiber, de-multiplex, decode specific commands and distribute to the FEAs, 2) receive data from the FEAs, multiplex it and send it to the ROM on the data link fiber, 3) distribute control and clock signals to adjacent trigger I/O modules, and 4) monitor drift chamber environmental sensors. One DIOM is required to control and readout each quadrant of the drift chamber. Commands decoded by the DIOM include: 1) Sync - generates a re-syncronization command for the TIOMs, 2) Event Read - after some delay sends a grant signal to the FEAs to begin sending data, and 3) Reset - reset signals sent to selected FEAs or TIOMs.

The Trigger I/O Module (TIOM) receives trigger data from the FEAs and multiplexes it on fiber-optic links to the drift chamber track-trigger system[9]. A single TIOM receives the data from two wedges of FEAs and sends the data out on 3 fiber-optic links. A total of 24 links are required for the entire chamber. The fiber transmitter is a Finisar FTM8510[7], driven by an HP Gigalink (HDMP-1022)[8] chip. The two TIOMs in a quadrant receive reset, clock and re-sync control lines from the DIOM controlling that quadrant. It sends temperature, voltage and fiber-link status information to the DIOM for monitoring purposes.

Both data and trigger I/O modules are mounted at the outer radius of the cylinder extension on the rear endplate. Fibers are connected through penetrations in the rear bulkhead.

D. Environmental Monitoring

Environmental sensors for the drift chamber include temperature and voltage in all the FEAs, DIOMs and TIOMs, fiber-optic link status, temperature on the endplates and inner and outer cylinders, humidity in the endplate regions and radiation monitors on both endplates. To minimize cabling on the rear endplate, environmental monitoring is placed in each DIOM. The circuitry includes a micro-controller (68HC705

MCU), an ADC, analog MUXs and a CANBus interface. CANBus is a standard interface adopted by BaBar for slow controls and monitoring. Opto-isolators are used to isolate front end electronics from off-detector readout electronics.

Four radiation monitors on the rear and two on the front endplate employ RADFET devices[10] that record accumulated doses. Two ranges are used, some to record doses in the 1 rad range and others set to respond at the 100 rad level.

E. Mechanical Design and Cooling

Limited access when the chamber is installed in BaBar required strict alignment to insure ease in replacing and servicing the electronics. Connector alignment is assured first in the assembly of the HV boards on jigs that precisely reproduced the feedthrough pattern on the chamber endplate. Alignment of the FEA boxes to the HV board connectors is acheived as the box slides into place using first card guides along the bars and FEA sides, then alignment pins screwed into the chamber endplate that pick up precision holes in the bottom of the FEA.

Power dissapated in the FEAs is 21 W (inner), 24 W (middle) and 30 W (outer). The DIOM take 18 W and the TIOMs 12 W. The total power in the rear endplate electronics is about 1.5 kW. The FEAs are screwed firmly down to radial bars that carry water cooling. DIOM and TIOM enclosures are mounted to cooling plates welded to water pipes along the outer radius of the electronics enclosure.

IV. PERFORMANCE

The electronics was installed on the drift chamber in July, 1998 and a number of tests done to evaluate the electronics performance. BaBar readout modules were used to configure, trigger and readout the electronics. Software was written that enabled measurement and monitoring of a number of variables for each channel, including FADC pedestal, analog gain, timing offsets, and discriminator noise floor. In addition, a 3 meter long scintillator was placed down the central tube to provide a trigger for cosmic rays. Roughly 1 million triggers were recorded and used to study performance for position resolution and dE/dx.

Progress was made on eliminating noise sources both within the FEA boxes and external sources to the point that the current measured noise is consistent with the expected intrinsic noise from the front-end amplifier and the drift chamber sense wires. Calibration quantities have been monitored for stability between calibration runs over the month of cosmic ray data taking. Figure 5 is the distribution of analog gain determined from calibration after the electronics was installed. The analog gain calibration was found to have a thermal dependence slightly larger than expected (.5%/°C), which has required more attention to allowing the electronics to warm up before taking data. The electronics cooling system has been shown to maintain a stable temperature at the level of ± 1°C.

Cosmic ray data were analyzed to determine the optimal time-to-distance functions and measure resolution versus drift distance from the sense wire for a variety of settings

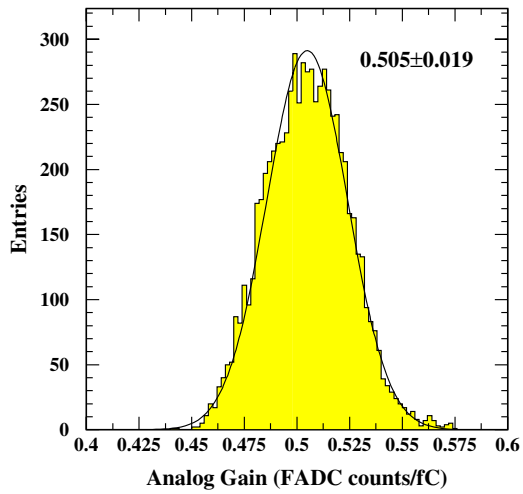

Figure 6: Distribution of analog gain determined from calibration for the 7104 channels of drift chamber electronics.

of high voltage and discriminator threshold. Figure 4 shows the measured resolution versus drift distance for the nominal high voltage (1960 V) and a threshold setting of 190 mV (corresponding to roughly 3 electron threshold). Doubling the chamber gain results in a 10 μm gain in resolution in the middle of the cell, suggesting that we are very near the intrinsic limit.

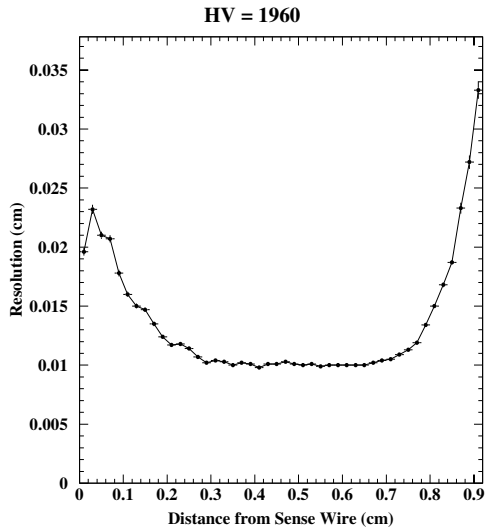

Figure 7: Resolution versus distance from the sense wire for cosmic ray data taken at HV=1960 V.

The dE/dx resolution was also studied. These data were taken with no magnetic field so the momentum of the cosmic ray is unknown. Nevertheless, resolution can be studied by looking at the difference in mean dE/dx between the upper and lower half of the track. Based on the width of this distribution, the predicted value for a single track is 6.5 %, in good agreement with expectation.

V. CONCLUSIONS

The drift chamber with the electronics is currently installed in the BaBar detector, which is preparing to be rolled on the PEP-II beamline in March 1999. First beam with BaBar is expected in late April 1999.

A drift chamber electronics system with over 7000 channels has been built that meets BaBar requirements for leading edge timing resolution, charge measurement for dE/dx and prompt hit information for a charged-track trigger. Two custom integrated circuits were employed to acheive high channel density, which, together with careful mechanical integration, enabled the electronics to be mounted on the chamber endplate. Recent tests with cosmic rays on the full drift chamber confirm expected performance, stability and reliability.

VI. ACKNOWLEDGMENTS

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