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ASIC IMPLEMENTATION OF A DATA–PUSH ARCHITECTURE FOR SILICON PIXEL READOUT

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ABSTRACT

A digital circuit for reading out a silicon pixel array consisting of 64 × 256 elements has been designed. The readout architecture has a data-push sequencing with a throughput of about 200ns/hit. The critical elements of this design have been fabricated through MOSIS using the HP 1.2μm double-metal-single-polysilicon process. Design details of the ASIC and test results are presented. Measurements of interface effects (metastability) between the analog and digital circuit are also presented.

1. Introduction

The advantages of silicon pixel detectors, namely, their higher spatial resolution and significantly improved pattern recognition (due to a 3-dimensional space point measurement on a charged track), have been well recognized. Additionally, their ability to withstand higher doses of damaging radiation make them a highly attractive detector for inner tracking layers at hadron colliders. Hybrid pixel detectors with high spatial resolution ($\leq 5\mu m$ in each dimension), albeit, with slow sequential readout of the pixels have been commercially available for about a decade. Hence, the thrust of the R&D in this area has been on readout chips for use in high energy physics.

The Data-Push Architecture (DPA) is designed for use at radii of about 10 cm in intermediate luminosity ($L \leq 10^{33} cm^{-2} s^{-1}$) environments or at about 3 cm radii in low luminosity ($L \leq 10^{32} cm^{-2} s^{-1}$) applications. The crucial feature of this readout architecture is that it has data-driven sequencing; a read cycle is initiated by any pixel with a signal above threshold and data are shipped out sequentially. This architecture ensures that the data are available with minimal delay after an event and can enter in decision making at the lowest level of the trigger logic.

Figure 1 shows a simplified block diagram for a pixel array consisting of 64 × 256 elements. The unit cell consists of a charge preamplifier, a discriminator and a storage capacitor. Charged particles producing signals above threshold generate *hit* signals on common bus lines along each column. The column logic registers these signals and

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initiates a readout cycle which presents the analog information for each row in the *hit* column to the row logic. These signals are discriminated and the row with the valid *hit* is identified. Next, the data consisting of a row address, a column address, pulse heights (including column neighbours) and a time-stamp are sent out on an external bus. The details of the analog circuitry, shown in the dashed box, can be found elsewhere.[1] The digital circuit can be broadly classified into *Column Logic, Row Logic, Time-Stamp Logic* and *Control Logic*. Below, we describe these in greater detail.

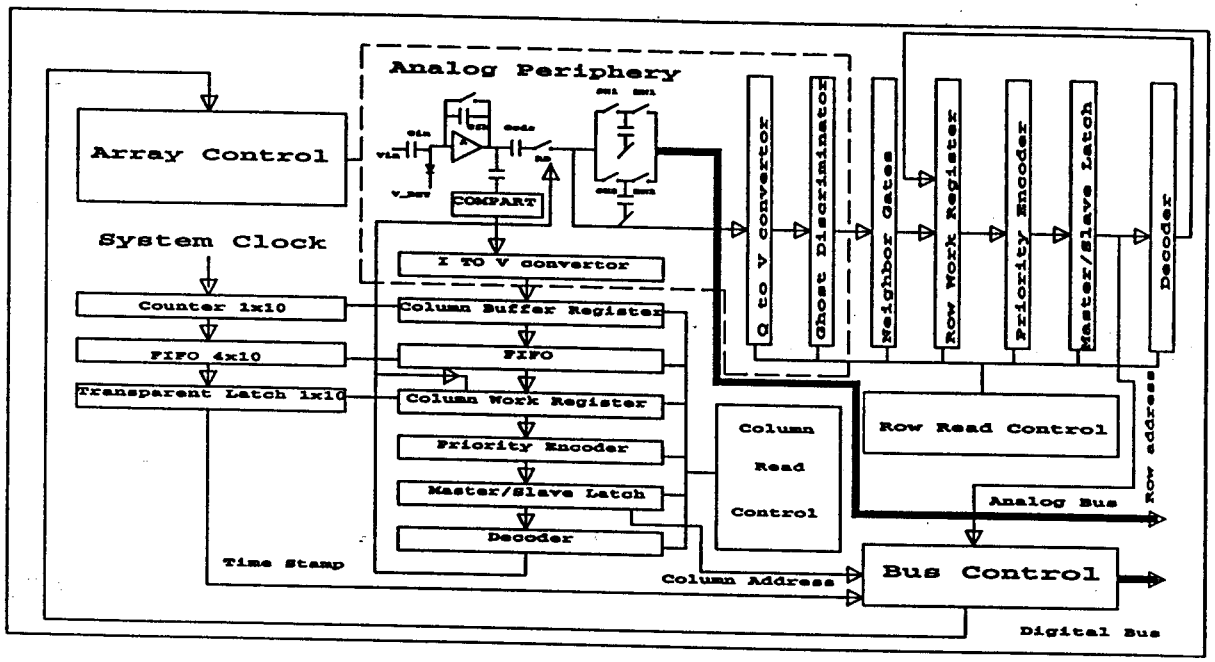

Fig. 1. Block diagram of the DPA pixel array readout system.

2. Digital Logic

The task of the digital circuit is to latch signals along column busses asynchronously and record their time of arrival (time-stamp). Also, it should be able to handle multiple hits in the same time window. Furthermore, adequate buffering has to be provided to minimize any loss of data.

2.1. Column Logic and Time-Stamp Logic

The Column Logic is composed of *data buffers*, FIFO, *work registers*, a *priority encoder*, *master/slave latches* and a *decoder*. The most crucial element of the design is the digital front-end consisting of 64 channels of buffer registers and reset logic. Figure 2 shows the gate level diagram for a single channel. The data (DC0) are latched in a flip-flop and a signal (DF0) is sent to the FIFO. The signal (CRST0) is used to promptly reset the analog circuits in each pixel along the column, thereby minimizing

the dead-time for that column. The signal *RST_N* resets the buffer register later on in the read cycle. We will return to this front-end later when we discuss metastability issues.

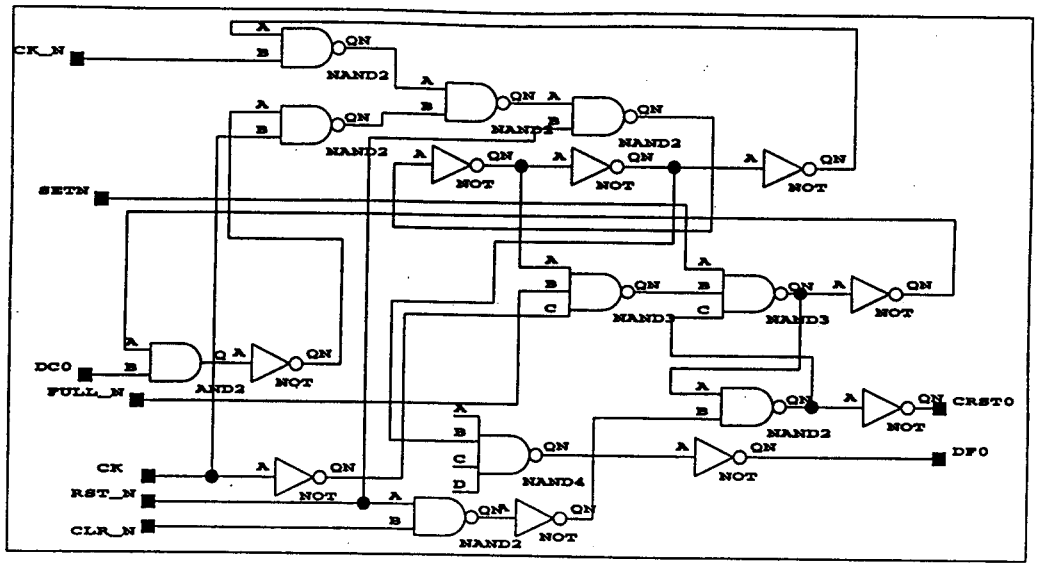

Fig. 2. Design of a single channel of the front-end of the column circuit.

Figure 3 shows the circuit of a single bit of the 4-deep FIFO which stores the data temporarily. The write line (WR) allows the data (DI1) into the storage cell and the read line (*OE_N*) allows data from the storage cell into a tri-state data bus. The data bus routes information into the work register. The Control Logic prevents new data from being loaded when the 4 levels of the FIFO are full.

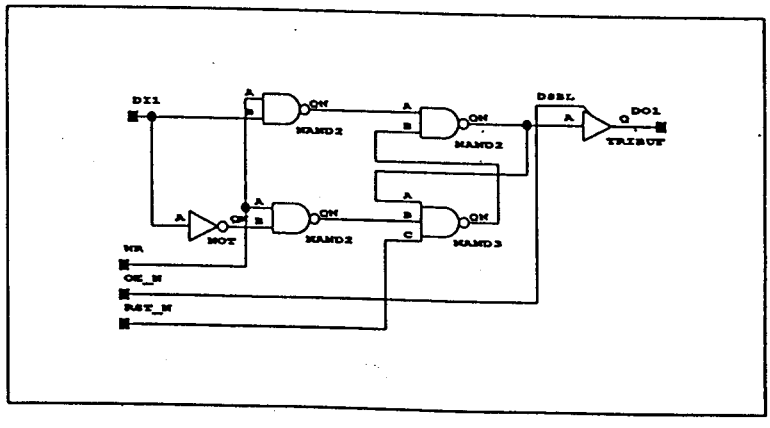

Fig. 3. Gate level design of a single cell in the FIFO.

The data out of the FIFO go into a register followed by the priority encoder. This is a 64-bit input and 6-bit output encoder (a similar 256/8 bits encoder is used in the Row Logic), details of which are not shown here. It promptly picks up the highest bit with a valid *hit*, encodes the column address for that bit and sends it to the Bus Control

for temporary storage. Simultaneously, this bit is decoded, a read signal is issued to the pixel cells in that column and the decoded bit is fed back to the *work register* as a reset signal. The next data bit is selected by the encoder under Control Logic when the row periphery has finished storing the previous hit.

The Time-Stamp Logic works in parallel with the Column Logic. It consists of a 10-bit counter and a 4-deep FIFO which corresponds to the column FIFO. The time-stamp accuracy is 20 ns for a system clock of 50MHz. The FIFO is controlled by the same write and read lines as that of column FIFO.

2.2. Row Logic and Control Logic

As described above, the column logic locates the first column with a valid *hit* and allows all analog signals on the rows in that column to be presented to common busses along the rows. These analog pulses are stored in 2-deep analog multiplexors (Ping-Pong) and go into the charge-to-voltage convertors under Control Logic. Next, these signals are discriminated and digital signals enter the Row Logic. The whole read out system including both analog and digital circuits is queued by the Control Logic, details of which are beyond the scope of this article.[3]

The Row Logic has features similar to the Column Logic. It encodes the addresses of rows with valid data and presents them to the Control Logic for transmission to the external bus. In addition, it records the addresses of nearest neighbours, taking edge effects and overlapping addresses into account. There is no need for buffering the digital data at this point because all operations are synchronous.

3. ASIC Implementation

Two ASIC's containing a 16 channel version of the column architecture were fabricated through MOSIS using the HP 1.2μm double-metal-single-polysilicon process. The ASIC's performed well compared to expected behaviour obtained from HSPICE simulations. A detailed description of these ASIC's can be found elsewhere.[2]

3.1. Metastability

Whenever a digital circuit is presented with asynchronous data, metastable behaviour can be expected under certain conditions.[4] This is described schematically in figure 4a. When the input pulses arrive within a clock pulse, the falling edge of the clock latches the data and a normal output pulse is generated (Line A). When the input pulses arrive after the falling edge of the clock the output pulse is generated by the next clock pulse (Line B). In our case, this results in normal operation but the time-stamp is shifted by one clock period. If the input data transition occurs close to the falling edge of a clock the output can be in an unpredictable state (Line C). As shown in the figure, this may result in improper pulse shapes which are either too low in voltage and width ("runts") or experience additional delay. In the former case, this metastable behavior results in loss of data and in the latter case there can be failures in the later stages of the circuit that expect synchronous pulses.

The prototype ASIC's displayed metastable behaviour of both types. The frequency of occurance of "runts" was measured for input rise-times in the range of 4 ns to 25 ns which is expected from pixel detectors. For all rise-times, the width of the metastability was determined to be less than 1 ns, ie, "runts" occurred only if the phase

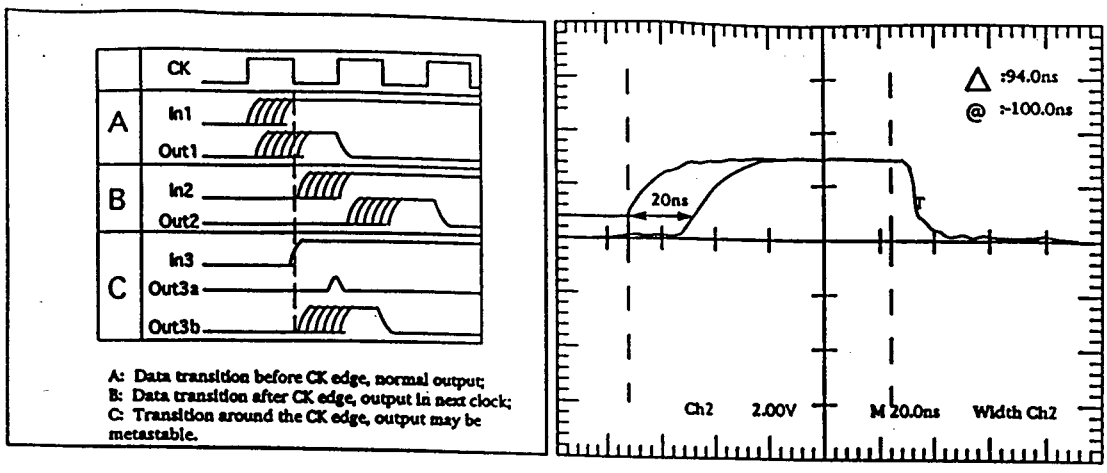

Fig. 4. a: Metastable behaviour in a Flip-Flop; b: Typical metastability time-window.

difference between the input and the clock falling edge was less than 0.5 ns. For a 20 ns clock period (50 MHz clock) this would effect less than 5 % of the asynchronous inputs. Furthermore, out of the inputs that did fall in this 1 ns time window, less than 0.1 % produced "runts". Hence, the loss of data due to metastability in this circuit can be considered negligible for particle physics applications.

The second form of metastability was also observed but it has not yet been fully quantified. In figure 4b we show output pulses generated by input pulses with 4 ns rise-times. The two pulses shown are delayed by approximately 20 ns with respect to each other. This time difference represents the extreme cases that were observed when the input pulse arrived within the metastability window. The frequency of occurrance of these delayed pulses has not yet been measured but is expected to be low. The failure that can be caused by these late pulses requires detailed study that has not yet been performed. Once characterized, corrective measures can be taken to minimize such effects.

4. Summary

A data-push readout circuit for silicon pixel detectors has been designed and the critical elements have been fabricated using the HP 1.2*um* process. The logical functions have been tested and are consistent with HSPICE simulations. Preliminary measurements of metastability in the front-end of the digital circuit indicate that low failure rates can be achieved.

References

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2. S. Mani, *et. al.*, "An Asynchronous Data Acquisition ASIC with a Data-Push Architecture", to be published in Nuclear Instruments and Methods.
3. For a detailed description, see S. Rojas, Masters' thesis, in preperation.
4. T. J. Gabara *et. al.*, "Metastability of CMOS Master/Slave Flip-Flops", IEEE Transactions on Circuits and Systems, *Vol.39, No.10, October 1992*