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An Analog Memory Integrated Circuit for Waveform Acquisition up to 900 MHz*

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Abstract

The design and implementation of a switched-capacitor memory suitable for capturing high-speed analog waveforms is described. Highlights of the presented circuit are a 900 MHz sampling frequency (generated on chip), input signal independent cell pedestals and sampling instances, and cell gains that are insensitive to component sizes. A two-channel version of the memory with 32 cells for each channel has been integrated in a 2-µm complementary metal oxide semiconductor (CMOS) process with poly-to-poly capacitors. The measured rms cell pedestal variation in a channel after baseline subtraction is less than 0.3 mV across the full input signal range. The cell-to-cell gain matching is better than 0.01% rms, and the nonlinearity is less than 0.03% for a 2.5-V input range. The dynamic range of the memory exceeds 13 bits, and the peak signal-to-(noise+distortion) ratio for a 21.4 MHz sine wave sampled at 900 MHz is 59 dB.

I. INTRODUCTION

The potential of switched-capacitor technology for acquiring analog signals in high-energy physics (HEP) applications has been demonstrated in a number of analog memory designs [1–8]. When compared with flash analog-to-digital converters and charge-coupled devices, these circuits can show superior performance with respect to cost, density, dynamic range, and power dissipation. Analog memory circuits essentially exploit the fact that in HEP applications commonly only parts of the analog input waveforms need to be encoded digitally; a continuous digitization is thus not required. Applications for such circuits include, for example, pulse echo phenomena (ultrasonic material and medical testing), pulse shape recording (HEP detectors, accelerator diagnostics), and laboratory instrumentation (oscilloscopes). In high-energy physics experiments, analog memory devices are presently employed to record signals at sampling rates up to 100 MHz and with a dynamic range up to 12 b [9–12].

This work investigates the feasibility of using switched capacitor technology for the acquisition of high dynamic range signals at sampling rates exceeding 100 MHz. Traditionally, flash analog-to-digital converters are employed in high-speed sampling systems. Commercial monolithic flash converters are, however, presently limited to an 8-b dynamic range for sampling rates exceeding 100 MHz. In addition, such converters are expensive and dissipate considerable power.

This paper presents a switched-capacitor analog memory with a dynamic range that exceeds 12 b at sampling rates up to 900 MHz. The device can be used in a system to measure positions of a high energy accelerator electron beam. In this application, waveforms from hundreds of beam position sensors must be sampled at rates of several hundred MHz. The input waveforms are sampled at a high rate, stored in the memory devices, and subsequently read out and digitized at a lower rate before new waveforms are acquired.

II. CIRCUIT DESCRIPTION

A simplified schematic of one memory channel is shown in Fig. 1 [13, 14]. Each memory cell consists of a large write transistor M_{wi}, a minimum-size read transistor M_{ri}, and a storage capacitor C_i. The dc reference voltages are V_{com} and V_{bias}. During data acquisition, transistor M_{in} is turned on, connecting the signal V_{in} to the input bus, while transistor M_{out} and the read switches M_{ri} are all off. An analog signal applied at the circuit's input is sampled onto the cell capacitors C_i by sequentially turning transistors M_{w1} through M_{w32} on and off. During readout, transfer gate M_{in} is turned off while M_{out} and M_{rst} are turned on, forcing the input bus to V_{bias}. The transistor M_{rst} is then turned off, and the voltage stored in the first cell is read out by turning transistor M_{r1} on. After the output has settled, the signal may be digitized with an external low-speed analog-to-digital converter. After digitization, M_{r1} is turned off, and

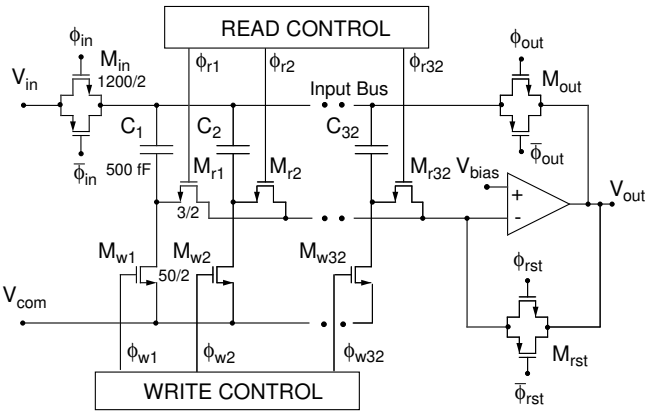

Fig. 1. Simplified schematic of one 32-cell analog memory channel.

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M_{rst} is again turned on, which forces the input bus back to V_{bias}. The cycle is repeated for all cells.

The principal performance issues for the intended application are low cell-to-cell sample period, offset, and gain variations across a channel, all of which are governed by the circuit architecture and its sensitivity to the matching properties of its constituent transistors and capacitors. In the presented circuit, the cell-to-cell response variation is dominated by charge injection during turn-off of the large NMOS write transistors, and the resulting pedestal mismatch increases with the size of the transistors for a given sampling capacitance C_i [14]. The on-resistance of the write transistor must be low enough to satisfy the input bandwidth requirements. The size of the write transistor is thus a trade-off between the input bandwidth and the pedestal mismatch for a given sampling capacitor value, which in turn is chosen on the basis of thermal noise considerations and the need to make relevant parasitics negligible. Note that complementary write switches would reduce the overall pedestal sizes, but would worsen the cell pedestal uniformity across a channel. Furthermore, the generation of precise complementary write control signals is hard to implement for high speed designs.

An important characteristic of the proposed memory circuit is that the cell pedestals do not depend on the input signal level and can be accurately determined and then cancelled by means of either analog or digital subtraction. Moreover, the turn-off time of the write switches is independent of the input signal level, eliminating the timing errors that would require extensive ac data correction at high sampling rates.

The gain variation (dA_i/A) across a channel as a function of the capacitor mismatch (dC_i/C_i) can be approximated by [13]

$$\frac{dA_i}{A} = \frac{C_p}{C_i}\left(\frac{dC_i}{C_i}\right), \tag{1}$$

where C_p is the parasitic capacitance between the input and output of the operational amplifier. Capacitance C_p is generally small compared to C_i, and the gain from cell to cell is thus insensitive to capacitor size mismatch [15, 16].

A common input switch, M_{in}, could be used in the circuit of Fig. 1 because of the relatively small number of memory cells required in each channel for the intended application. This input switch must be large enough to achieve the desired bandwidth in the presence of the parasitic capacitance of the input bus and the combined capacitance of the addressed memory cells.

During the write phase, the cells of a memory channel are addressed sequentially via a starved inverter delay chain, as illustrated in Fig. 2. Such inverter chains have been employed previously in digital HEP applications [17]. A write pulse applied at A_{in} propagates through the delay elements, thereby locally producing the write address signals ϕ_{w1} through ϕ_{w32}. No high speed external clock that could perturb the analog signal during or after the sampling process is needed to achieve high sampling rates. The sampling frequency is governed by the inverter delay, and in order to ensure a delay that is independent of process variations, a servo feedback circuit that regulates voltage V_{ctr} is used [14]. The circuit dynamically adjusts V_{ctr} so that the total chain delay is determined by the delay of the two input control signals, A_{in} and A_{ref}. This feedback circuit also eliminates sensitivity of the inverter chain delay to variations in temperature and supply voltage.

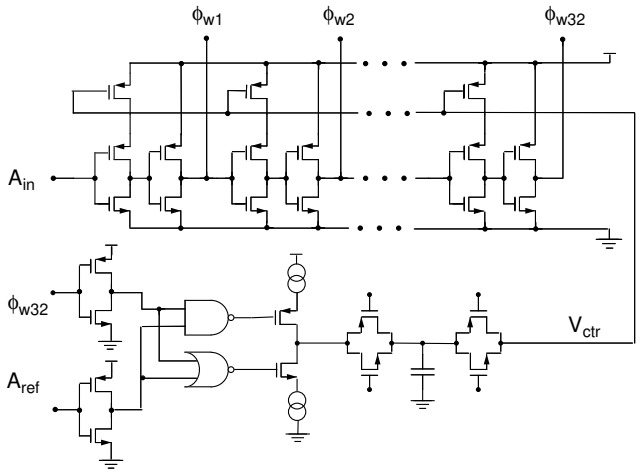

Fig. 2. Starved inverter delay elements with feedback compensation.

The readout of the analog memory is implemented with an on-chip two-phase read shift-register together with logic that generates the control signals for M_{r1} through M_{r32} (Fig. 1).

III. EXPERIMENTAL RESULTS

A. Implementation

A two-channel analog memory with 32 cells in each channel has been integrated in a 2-μm CMOS technology with poly-poly capacitors. The write and read control circuitry is common to both memory channels. The memory has been tailored for use in a beam position measurement system for an accelerator. In order to investigate the influence of the high-speed inverter delay chain circuit on the memory's performance (e.g. the matching of cell responses), a lower speed version of the chip was fabricated with the inverter delay chain replaced by a traditional two-phase write shift register. The two clock phases are generated on chip from a single input clock. The dimensions of both chips are 2.22 mm x 2.25 mm.

B. Test Setup

Figure 3 shows a block diagram of the measurement setup. The analog memory is placed on a custom printed-circuit board consisting of two signal layers, a ground plane, and a power plane. The analog input ac test signals for the memory are generated by a pulse generator and a sine wave signal source. The output of the sine wave generator is filtered by a passive bandpass and ac coupled to the analog memory input. The dc baseline input voltage V_{bl} and the reference input voltages V_{com} and V_{bias} (Fig. 1) are provided by three on-board digital-to-analog converters (DACs). The waveforms acquired in the analog

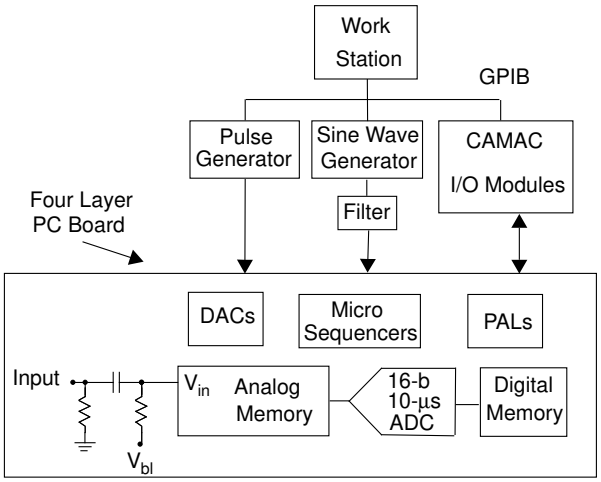

Fig. 3. Simplified test setup.

memory are read out, digitized with a 10-µs, 16-b commercial analog-to-digital converter, and stored in local static memory. The stored data is then transferred to a UNIX workstation for processing via optically isolated input/output CAMAC modules. The local control signals are generated by means of a programmable micro-sequencer.

C. DC Results

Performance parameters such as offset, gain, linearity, and noise were determined by recording the analog memory response to a set of dc voltages V_{bl} with the reference voltage V_{com} set to 2.5 V. Measurement results obtained from the analog memory with the shift-register write control (low-speed sampling chip) and from the analog memory with the delay chain write control (high-speed sampling chip) are virtually identical for dc input voltages. The results described in this section, which were obtained from the high-speed sampling chip, are thus representative of both analog memories. The delay between the two write control signals, A_{in} and A_{ref}, was set so as to establish a sampling frequency of 900 MHz.

An rms noise voltage of 0.3 mV was obtained from sets of 100 repeated measurements. For an input voltage range of 2.5 V, the dynamic range for dc input signals is thus better than 8,000/1. The theoretical noise voltage of the analog memory can be expressed as

$$\bar{v}^2 = \frac{kT}{C_i} + \left(\frac{C_i + C_{op}}{C_i}\right)^2 \bar{v}_{eq}^2, \qquad (2)$$

where k is the Boltzman constant, T is the temperature in Kelvin, C_{op} is the capacitance at the inverting input node of the amplifier during readout, and $\bar{v}_{eq}$ is the input-referred noise voltage of the amplifier. At a temperature of 300 K, the *kT/C* noise that is sampled on the 500 fF cell capacitor during the write phase is approximately 0.1 mV. The noise contribution of the on-chip amplifier v_{eq} in the test setup is calculated to be 0.1 mV. With a value for the capacitance C_{op} that is estimated to be twice the sampling capacitance, the total circuit noise in the system is theoretically 0.22 mV. This value is slightly lower than the measured noise voltage of 0.3 mV.

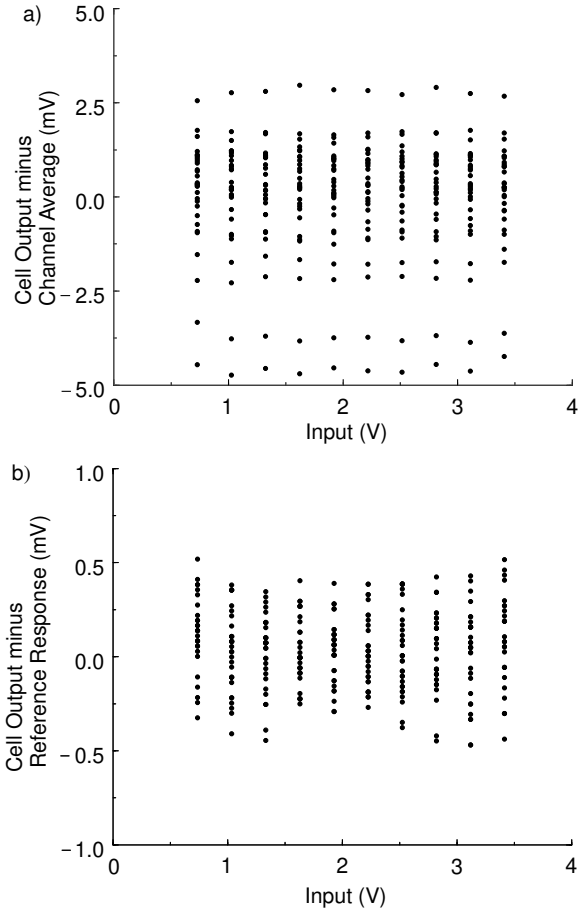

Fig. 4. Pedestal variations (a) before and (b) after subtraction of response to one dc reference input level. (900 MHz sampling frequency).

The raw cell-to-cell pedestal variation across a channel was measured to be 2 mV rms. Figure 4a shows the pedestal voltages of the 32 cells in one channel as a function of the input voltage level. The average output voltage of the memory channel is subtracted, so that the measurement data can be plotted on the same scale. In Fig. 4b the data is plotted with the cell responses to a single dc input voltage (V_{bl} = 2 V) subtracted. The rms cell response variation across the full input voltage range is only 0.3 mV (noise floor), demonstrating that the pedestal variations are independent of the dc input level and can be cancelled by a simple subtraction procedure.

The measured cell-to-cell gain matching is better than 0.01% rms with a mean gain of 0.9967, and the integral nonlinearity is less than 0.03% for a 2.5 V input range. The power dissipation for one channel operated from a single +5 V supply is 2 mW.

D. AC Results from the Low-Speed Sampling Chip

The ac performance of the circuits has been evaluated by applying a free running sine wave at the analog input. The ped-

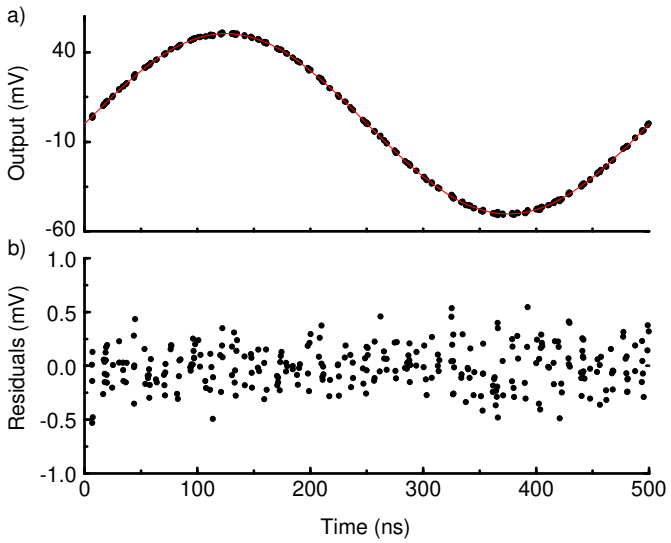

Fig. 5. a) Results of 20 measurement sets fitted to a 100-mV_{pp}, 2-MHz sine wave sampled at 13 MHz and plotted on a time scale modulo the period of the sine wave. b) Residuals from the fit.

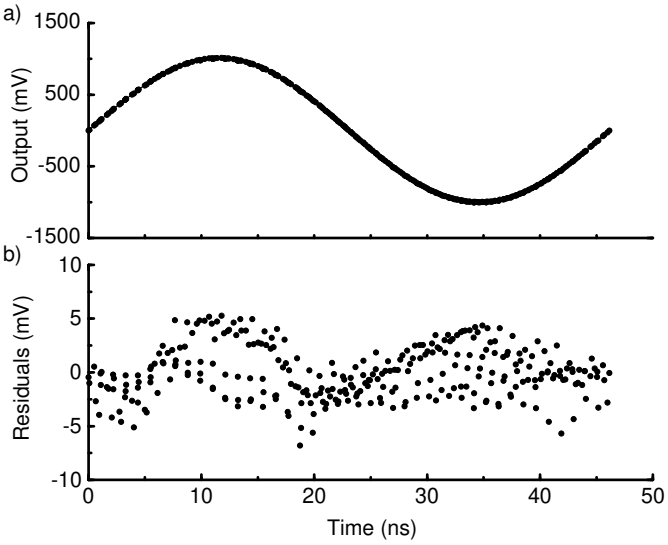

Fig. 7. a) Results of 20 measurement sets fitted to a 2-V_{pp}, 21.4-MHz sine wave sampled at 900 MHz and plotted on a time scale modulo the period of the sine wave. b) Residuals from the fit.

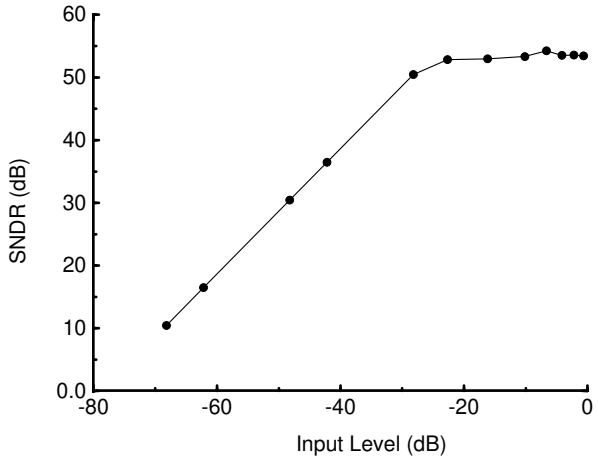

Fig. 6. Signal-to-(noise+distortion) ratio as a function of amplitude for a 2 MHz sine wave sampled at 13 MHz.

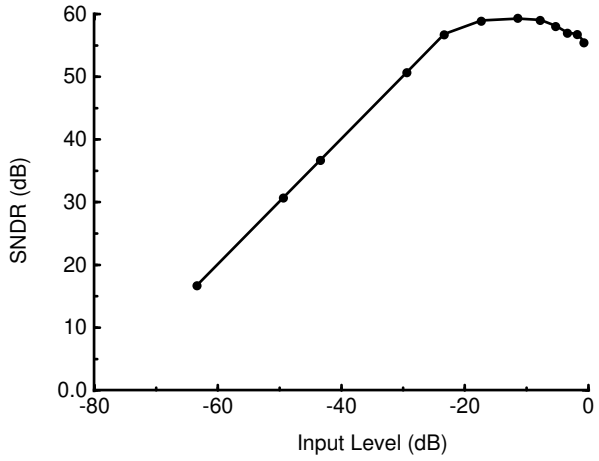

Fig. 8. Signal-to-(noise+distortion) ratio as a function of amplitude for a 21.4 MHz sine wave sampled at 900 MHz.

estal subtracted responses of 20 separate sets of measurements are then fitted to a common frequency, offset, and amplitude and a free phase for each set of measurements [18–20]. Figure 5a shows a plot of a 100-mV_{pp} amplitude, 2-MHz sine wave fitted to the measurement data. The clock frequency of the write shift register was set to 13 MHz. In Fig. 5b the deviations of the measured data from the ideal sine wave are plotted and an rms error of 0.3 mV is calculated. Since the phase of the input signal was not synchronized to the sampling process, this result is also a measure of the ac uniformity of the cells across a channel (e.g. linearity, gain). Figure 6 shows a plot of the signal-to-(noise+distortion) ratio (SNDR) as a function of the input amplitude, as measured for a 2-MHz input frequency and a 13-MHz sampling rate. An input level of 0 dB represents a sine wave whose peak-to-peak amplitude equals the 2.5 V input range of the analog memory. The SNDR figure is a good measure on how accurately an ac input signal can be reconstructed. As shown in Fig. 6, the analog memory achieves a 78-dB dynamic range for ac signals and a peak SNDR of 53 dB.

E. AC Results from the High-Speed Sampling Chip

The delay of the inverter-chain write control circuit on the high-speed sampling chip can be adjusted to obtain a sampling rate between 200 and 900 MHz. In this section, measurement results are presented that were obtained at a sampling rate of 900 MHz. The memory cell input time constant is designed to be 0.5 ns at V_{com} = 2.5 V and is independent of the input signal amplitude. Figures 7a and b show the response of the memory to a 2-V_{pp}, 21.4-MHz input sine wave and the residuals from the fit to an ideal curve, respectively. The fit yields rms devia-

tions of 3.4 mV. In Fig. 8 the SNDR is plotted as a function of the input sine wave amplitude. The dynamic range is 78 dB, and the peak SNDR is 59 dB. The performance of the memory degrades at large signal amplitudes principally due to harmonic distortion and timing errors. The cell-to-cell sample timing variation was measured to be less than 20 ps [14].

IV. CONCLUSION

This work presents a switched-capacitor analog sampling circuit in which cell pedestals are independent of the signal level, cell gains are insensitive to capacitor sizes, and the time at which the signal is sampled is independent of the input voltage. This enables a straightforward improvement of the circuit's performance by means of a simple offset subtraction procedure.

Two analog memory chips were designed, fabricated, and tested. The high-speed sampling chip comprises an inverter delay chain for write control that generates the sample clocks on chip from a single start pulse. The second chip employs a traditional two-phase shift register to generate the sample clocks for the analog memory. The dimensions of the memory cell components are a trade-off between the input bandwidth and the cell-to-cell response variations.

For dc input signals the performance of the two chips is identical. The raw cell-to-cell pedestal variation across a channel was measured to be 2 mV rms. After baseline substraction, the cell response variation across the full input voltage range is only 0.3 mV (noise floor). The measured nonlinearity is 0.03% for a 2.5 V input range and the cell-to-cell gain matching is 0.01% rms.

In order to measure the ac performance of an analog memory, test signals must be easy to define and generate. Sinusoidal signals fulfil these requirements and are widely used for the evaluation of electronic components. The signal-to-(noise +distortion) ratio gives a measure for the errors introduced by inaccurate sampling times, variations in the dc and ac response of different cells, nonlinearities, and circuit noise. For the high-speed sampling chip, a peak SNDR of 59 dB (or 10 effective bits) was achieved for a 21.4 MHz sine wave sampled at 900 MHz. Measurements on the low-speed chip yield a peak SNDR of 53 dB, as measured for a 2 MHz input sine wave sampled at 13 MHz.

V. ACKNOWLEDGMENTS

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