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MONOLITHIC TRANSCEIVER FOR FASTBUS CABLE SEGMENT—CSX*

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ABSTRACT

Specifications for a five-channel differential transceiver for the FASTBUS Cable Segment have been developed.[1,2] The transceiver, CSX, is being planned as a full-custom integrated circuit implementation. Specification and development plans are discussed. The project is being carried out in collaboration with the NIM/FASTBUS Committee.

INTRODUCTION

The FASTBUS Standard specifies a current-driven cable segment bus. Since no suitable driver circuits are commercially available for this purpose, present implementations utilize custom hybrid drivers and off-the-shelf ECL differential receivers. To overcome limitations of these cable segment interfaces and to reduce the required board space, specifications for the development of a monolithic five-channel differential transceiver have been developed. In collaboration with the NIM/FASTBUS Committee, we have received funding from the Department of Energy for a commercial contract to design and fabricate prototype units of the CSX integrated circuit. After a series of preliminary contacts with vendors of design and fabrication services for application specific integrated circuits (ASIC), we have solicited proposals for the CSX development. At present a contract for the design and production of prototypes is being finalized.

CSX DEVELOPMENT SPECIFICATIONS

The proposed logic diagram for the transceiver is shown in Fig. 1. A device pin-out and function table are given in Fig. 2. Following is a summary of significant aspects of the development specifications:[2]

Power supply voltages: an extended operating range of the interface supply voltages VCCI and VEEI from ±5 V to ±12 V will provide wider voltage ranges for driver current output compliance and receiver input common mode rejection.

Current driver voltage compliance: range limits specified at 0.5 V to 1.0 V typical from interface power supplies.

Receiver common mode voltage range: range limits specified at 1.0 V typical from interface power supplies.

Receiver differential input sensitivity: minimum input signal of ±25 mV typical to produce proper output logic state at specified propagation delay.

Driver current control: digital current select input (ISEL) to double output current from 4 mA to 8 mA.

Combination of the 8 mA output current option and the extended operating range for the interface power supply will permit special cable segment implementations for high-noise environments.

A gate programming feature allows the single-ended I/O to be configured as a bussed (BIO) or split (SIO) connection to four channels of the transceiver (one channel always has separate input and output connections). In the BIO configuration, four control terminals are available to simplify interface designs. Support for ECL and TTL compatibility on the same chip for single-ended I/O and control inputs will be investigated.

CSX transceivers will be packaged in standard PLCC28 plastic-leaded chip-carrier packages (JEDEC MO-047AB) suitable for surface mounting or usable with sockets. A printed circuit layout for a full cable segment interface of a Master module with 12 each CSX transceivers can readily be implemented in an area of approximately 3 × 16 cm (1 1/4 × 6 1/4 inches) along the module auxiliary connector, based on two signal layers. A layout study is shown in Fig. 3.

DEVELOPMENT PLAN

The CSX transceiver project will be implemented in two phases. A contract for the transceiver chip design and prototype fabrication is being finalized now. Design work is expected to start in December 1988. Delivery of 50 each packaged and tested prototype integrated circuits for final evaluation and approval is planned six to eight months after project start. The second phase, a joint production order from laboratories, universities and industry involved in FASTBUS work, is expected during the second half of 1989. At a production volume of 10K units, the cost of CSX transceivers has been estimated at $23 each.

REFERENCES

[1] ANSI/IEEE Standard 960–1986, *"FASTBUS Modular High-Speed Data Acquisition and Control System."*

[2] H. V. Walz, B. Bertolucci, D. B. Gustavson, *"Technical Specification, Monolithic Transceiver for FASTBUS Cable Segment—CSX,"* SLAC-TN-86-7, December 1986.

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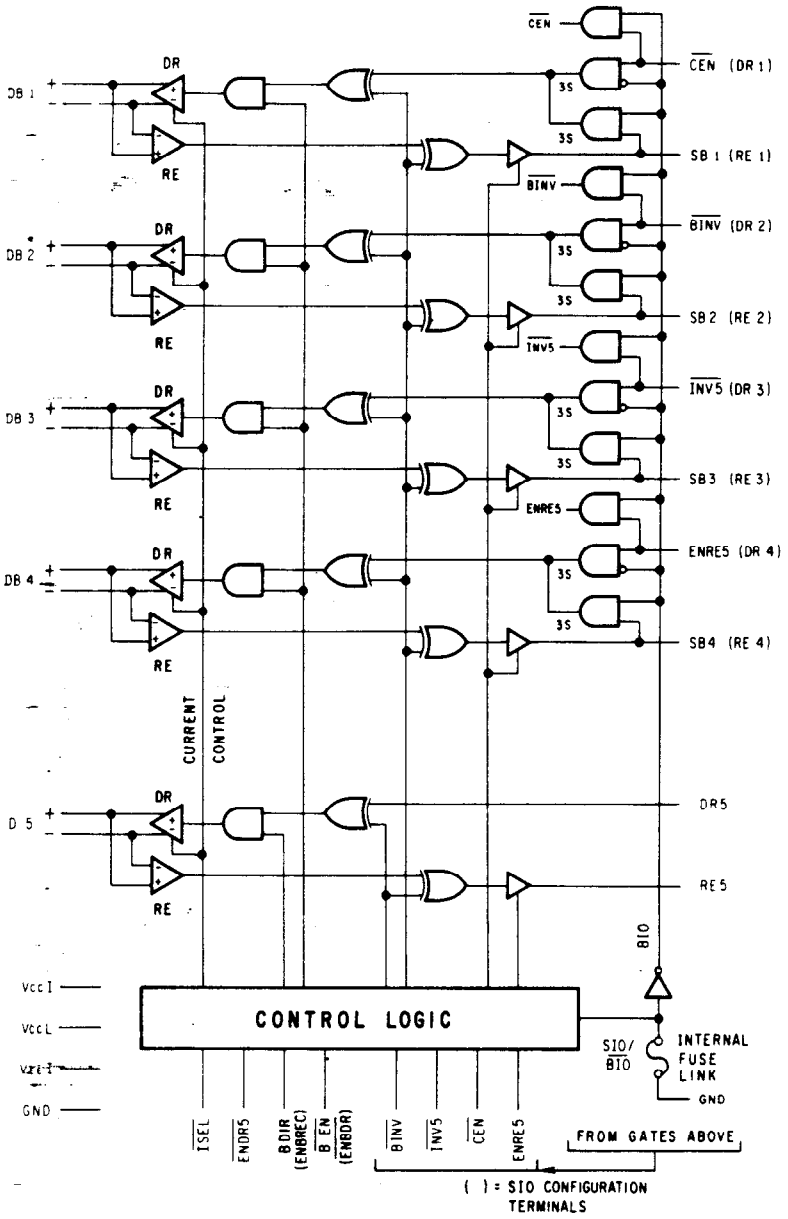
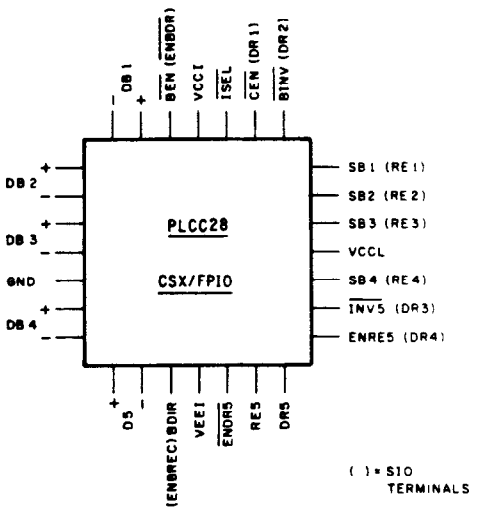


Fig. 1. CSX/FPIO gate programmable transceiver.



DBi - Differential Bus I/O Terminals
SBi - Single-End Bus I/O Terminals
DBi - Current Driver Inputs
REi - Receiver Outputs

CSX/BIO FUNCTION TABLE			
	L	H	DESCRIPTION
$\overline{ISEL}$	2IS	IS	DRIVER CURRENT CONTROL
$\overline{CEN}$	EN	DIS	ALL DR AND RE OUTPUTS
$\overline{BEN}$	EN	DIS	DR 1-4 AND RE 1-4 OUTPUTS
BDIR	SB→DB	DB→SB	BUS DIRECTION CONTROL
$\overline{BINV}$	SB→DB	SB→DB	BUS INVERT CONTROL
$\overline{INV5}$	RE4→DR5	RE5→DR5	DR5, RE5 INVERT CONTROL
$\overline{ENDR5}$	EN	DIS	DRIVER 5 OUTPUT
ENRE5	DIS	EN	RE 5 OUTPUT
All control inputs have on-chip pull-ups to Logic = H level			

CSX/SIO FUNCTION TABLE			
	L	H	DESCRIPTION
$\overline{ENBDR}$	EN	DIS	DR1-4 OUTPUTS
ENBREC	DIS	EN	RE1-4 OUTPUTS

Fig. 2. CSX/FPIO pin-out and function table.

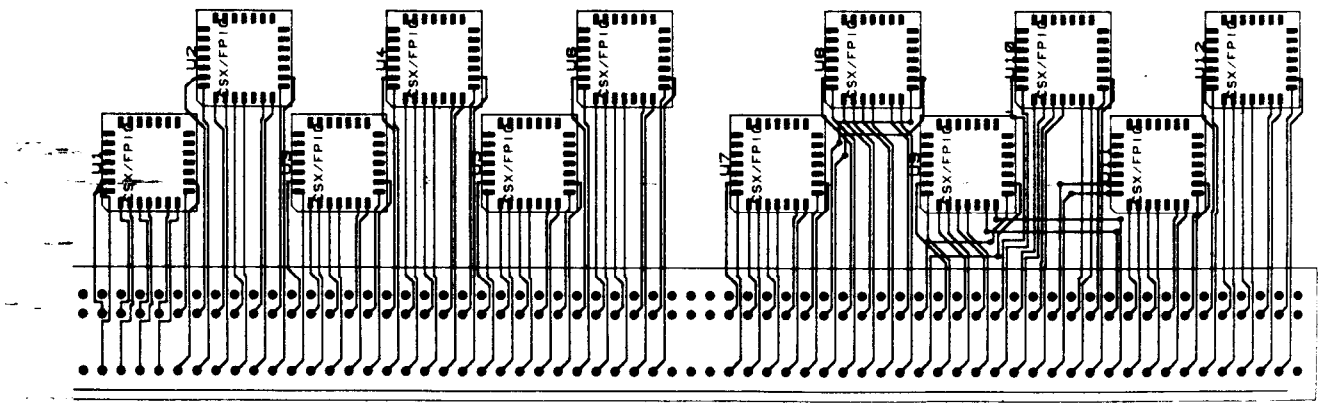


Fig. 3. Printed circuit layout study.