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A FASTBUS FLASH ADC SYSTEM FOR THE MARK II VERTEX CHAMBER*

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INTRODUCTION

This is a description of a flash ADC system built for the Mark II experiment at the Stanford Linear Accelerator Center (SLAC). This system was designed for use in the experiment's vertex chamber where signals could occur over a relatively long time, approximately 10 microseconds. This long time, coupled with fast cable amplifiers, necessitated an alternate design approach than was used with a dE/dX FASTBUS flash ADC design [1]. See Figure 1 for a block diagram of the system.

PHYSICAL CONFIGURATION

A representation of the physical configuration of the FASTBUS portion of the system is shown in Figure 3. The subsystem is contained in two FASTBUS crates. There are 26 FADC boards in the subsystem, 12 + 1 spare in each crate. The timing generator is on two boards, one named I/O Controller and the other named I/O Interface. All (26) High Speed Clocks are driven on individual shielded twisted pair cables from the I/O Controller board. This was done to minimize channel mismatch due to small differences in High Speed Clock waveshapes. Both the I/O Controller and the I/O Interface boards drive three signals on their crate backplanes:

ACQUISITION
START PROC.
PROCESSING CLK

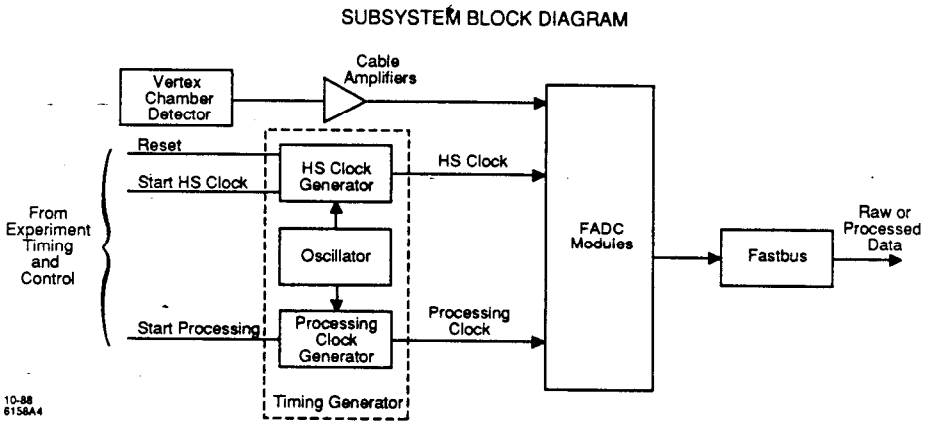

Figure 1.

GENERAL OPERATION

Approximately 380 analog signals from the Vertex Chamber Detector are sent to the Flash Analog-to-Digital (FADC) modules via the Cable Amplifiers. The FADC modules digitize the analog signals into 1022, 10 nanosecond samples for each input, with six bit amplitude resolution. The FADC modules also have the capability of detecting when the amplitude has exceeded a preset threshold value and also can detect when the amplitude drops below the threshold.

Figure 2 shows the overall timing involved in the system. The RESET pulse clears any current mode and gets the FADC module into the Acquisition mode. In this mode the system will digitize the analog inputs with the timing derived from the High Speed (HS) Clock. The next pulse to arrive is the START HS CLOCK. The timing of this pulse is very important since the HS Clock is coherent with this pulse and all the timing for digitization is derived from this clock. The number of pulses in the HS Clock burst is determined by the timing generator. If further processing is desired a START PROCESSING signal must occur before the next RESET pulse arrives. The START PROCESSING signal will get the FADC module into the Processing mode, and will allow the Processing Clocks to provide timing for the processing to take place. When the processing cycle is complete the FADC module will drop out of the processing mode and will be accessible for FASTBUS operations.

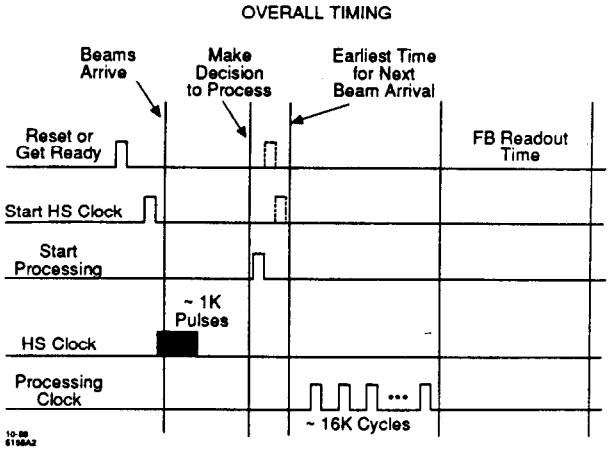

Figure 2.

*Work supported by the Department of Energy, contract DE-AC03-76SF00515.

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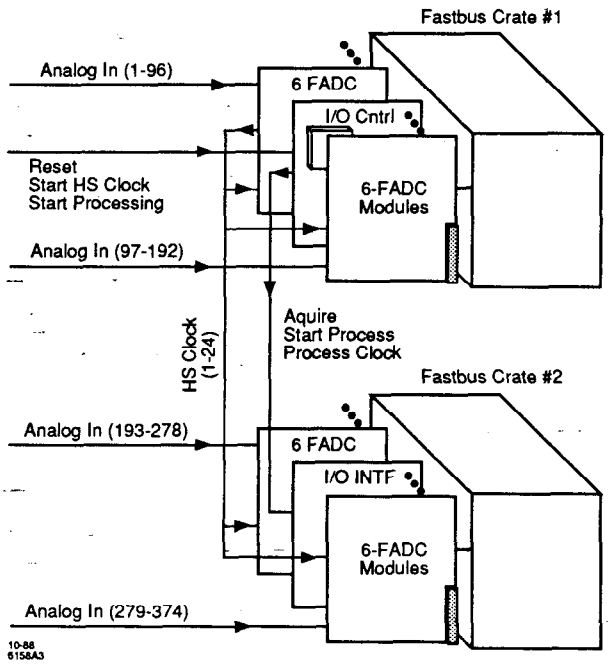

Figure 3.

The spares are installed in the crates so that they can be powered-up and calibrated ahead of time. The on-board oscillator is on the I/O Controller board. The crates are not full so there is room to add more modules necessary to access the FASTBUS crate segments.

OPERATING SPECIFICS

Timing Generator

The timing generator diagram is shown in Figure 4. The on-board oscillator is a commercial device built by Berkeley Nucleonics. Some pertinent specifications:

Model	C-1000
Frequency	100 Mhz
Frequency stability	$+/- 2 \times 10^{-7}$/week
Jitter (between ext trig & first coherent clock pulse)	+/- 100 ps peak
Input/output levels	ECL

The timing generator has the capability of generating two timing strings — High Speed Clocks and Processing Clocks. When the Reset pulse arrives the timing generator starts jam transferring the acquisition number into the length counter, and sends out an ACQUISITION pulse to the FADC modules. It also clears a Start Inhibit latch. When the START HS CLOCK pulse arrives, the oscillator syncs off the trail edge of this pulse and a coherent 100 Mhz pulse train known as the HS Clock is sent to all the FADC modules. After the oscillator syncs the Start Inhibit latch is set again to inhibit multiple starts. The length counter counts down at each HS Clock pulse. When the length counter reaches zero the HS Clocks are gated off.

When the START PROCESSING pulse arrives the timing generator starts jam transferring the processing number into the length counter and sends out a START PROC. signal to all the FADC modules. The timing generator then sends out a 20 Mhz signal known as the PROCESSING CLK to all the FADC modules. The length counter is decremented on each PROCESS CLOCK and when it reaches zero the PROCESS CLOCK is gated off.

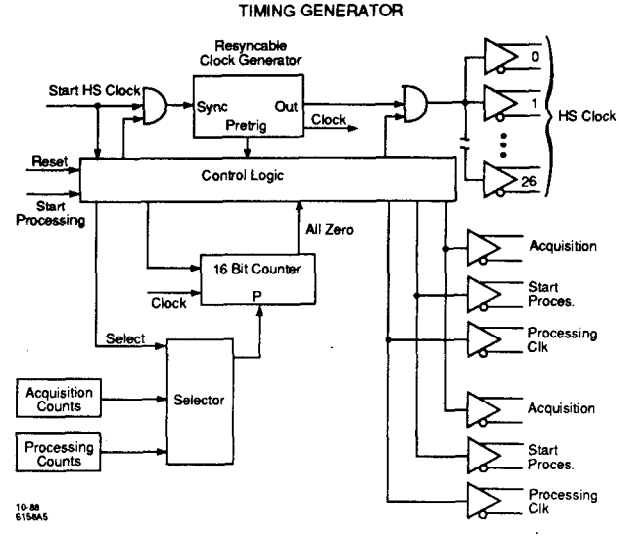

Figure 4.

FADC Module

The Flash ADC module has the following functional characteristics:

- 16 Analog to digital channels — each channel has:
  - An isolated differential amplifier
  - Two emitter-follower amplifier stages
  - Manual d.c. offset adjustment
  - A 6-bit, 100 Msps, flash analog-to-digital converter
  - Data memory for 1024 (1K), 6 bit, words
- Processing logic
  - Threshold memory — 16 each, 4 bit words
  - 6 bit comparator
  - Address memory — 32 each, 10 bit words
    - Holds address of first data over the threshold value
    - Holds address of last data over the threshold value
- FASTBUS logic
  - Supports data space and csr space partitioning

- Has a 16 bit NTA register — doubles as an address generator during Acquisition mode and Data Processing mode
- Supports random data (mode 0) Reads and Writes
- Supports block transfer (mode 1) Reads and Writes
- Supports NTA transfer (mode 2) Reads and Writes
- Internal memory access

Data Memory	Read Only
Threshold Memory	Read/Write
Address Memory	Read Only

- Returns SS codes on all transfers (Busy code returned if FASTBUS transfer attempted during Acquisition mode or Data Processing mode

FADC Module Operation

The FADC module block diagram is shown in Figure 5.

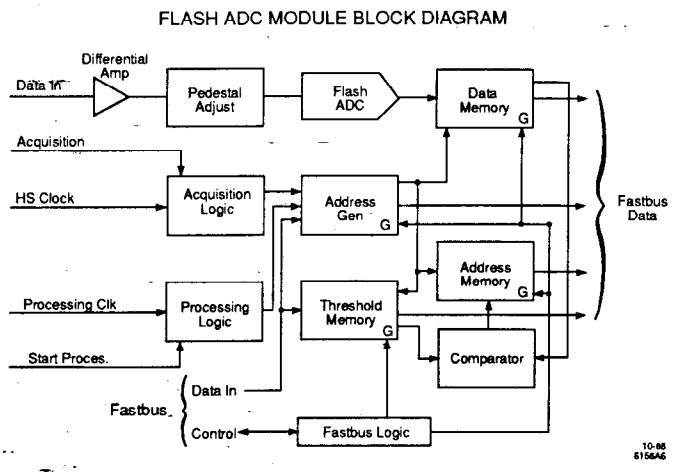

Figure 5.

First a threshold must be established for each channel. This can be any value between 0 and 15 (decimal). These values are loaded into the Threshhold Memory. The module goes into the Acquisition mode when the ACQUISITION pulse is received. The HS Clock signal provides timing pulses so that all the incoming analog signals are divided up into 1022, 10 nanosecond time slices. The amplitude of the time slices are stored in the Data Memory. Next, the module goes into the Data Processing mode when the START PROCESS. signal is encountered. In this mode each amplitude value is compared with its channel's threshold and the "first over" and "last over" address values are recorded (in the Address Memory). See Figure 6. The rate of operation is controlled by the Process Clock.

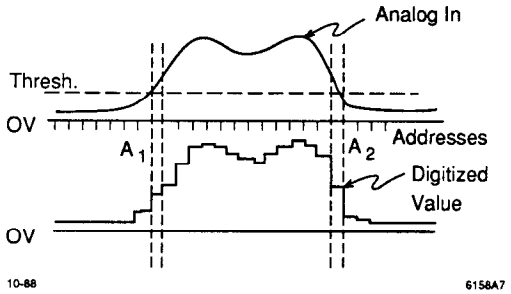

Figure 6.

FASTBUS Operations

Usually at this point the host will Read the Address Memory and decide which portions of the Data Memory are interesting and will read just these portions. The amplitude of the digitized waveform will be proportional to the velocity of the ionizing particle and the timing of the waveform will be proportional to the proximity of the particle to the sensing wires in the chamber.

SYSTEM TEST RESULTS

The system tests to date have shown a timing resolution sigma of 200 picoseconds.

REFERENCE

[1] See IEEE Transactions on Nuclear Science **33**, 1 (1986) pp. 86-89.