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A CDU–BASED DATA ACQUISITION SYSTEM FOR THE ENERGY SPECTROMETER AT THE STANFORD LINEAR COLLIDER*

D. D. BRIGGS AND J. E. TINSMAN
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94309

F. ROUSE†
Lawrence Berkeley Laboratory, Berkeley, California 94720

CHRISTOPH VON ZANTHIER
University of California at Santa Cruz, Santa Cruz, California 95064

Abstract

We describe a system using the Calorimetry Data Unit (a 32-channel multisample analog integrated circuit) to read out the charge ejected by secondary emission of a synchrotron beam from wires lying in its path. The wires comprise the Wire–Imaging Synchrotron Radiation Detector (WISRD) in the SLC Extraction–Line Spectrometer. The primary module in the system is a board containing 24 channels of charge sensitive amplification, shaping, sampling, multiplexing and digitization. This board also provides a fast analog measure of the charge distribution across the wires. We discuss the design and performance of this system.

Introduction

The Wire–Imaging Synchrotron Radiation Detector (WISRD) Readout system provides a novel measurement of the Stanford Linear Collider (SLC) at the Stanford Linear Accelerator Center beam energies on a pulse-by-pulse basis by measuring distributions of synchrotron radiation in the Extraction–Line Spectrometers (ELS).[1] The electron and positron beams leaving the Interaction Point (IP) are steered into ELS beam lines where each beam generates a pattern of synchrotron radiation. (See Figure 1.) Each pattern includes an initial and a final stripe. Each stripe falls on an array of 96 copper wires on 100 μm centers, each 75 μm diameter and 2 cm long. Two such arrays comprise one WISRD. The nominal distance between synchrotron stripes is 27 cm and is inversely proportional to the beam energy. The synchrotron radiation ejects charge from the wires. The total charge ejected from the wire array by each stripe is approximately 180 fC distributed over a few wires for 10^{10} electrons or positrons in an ideal primary beam of zero emittance, width and dispersion.[2] (See Figure 2.) Measurement of the mass of the Z^0 by the Mark II Detector[3] at SLC requires measurement of the beam energies. Compared to the energy measurement available from the Phosphor Screen Monitors in the ELS, this new technique offers improved resolution, due to its improved acceptance for high energy synchrotron light with lower production angle. The distributions are also of interest to accelerator diagnostics.

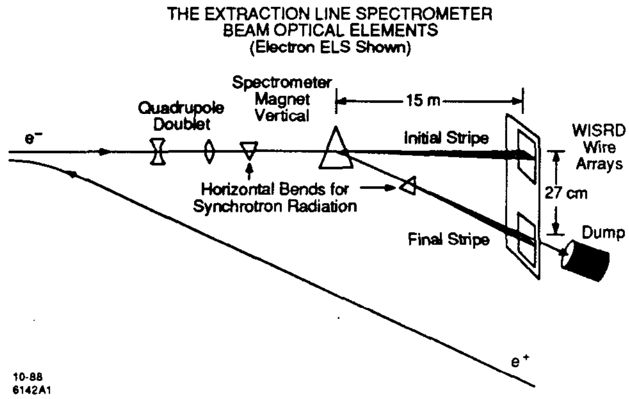

Fig. 1. Elements of the Extraction Line Spectrometer Beam Optics (electron beam into the south dump shown).

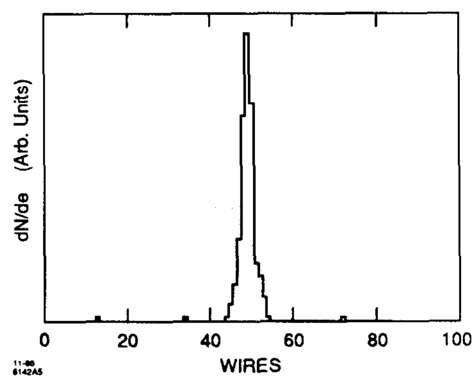

Fig. 2. Shown is a Monte Carlo histogram of the charge in arbitrary units as a function of wire number in an array. The above distribution corresponds to an ideal primary beam of zero emittance, width and dispersion. The total charge for a primary beam of 10^{10} electrons or positrons is predicted to be 180 fC. In operation the final stripe is expected to be four to six times wider than the initial stripe, due to dispersion, with the same total charge.

Environment

Each WISRD detector is about 600 feet downstream from the IP on opposite sides. They are within a few feet of their respective beam dumps and within inches of the beam pipes which deliver beams to the IP. Access is prohibited during operation and extremely limited by the accelerator schedule in any case. The radiation environment is harsh. Any cabling to the

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† Presidential Fellow, University of California at Berkeley.

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detector must run near the beamline. Therefore, preamplification, shaping and digitization are performed near the detector by several Data Acquisition (DAQ) modules. The major design considerations for these modules were resolution, reliability in a high radiation and electronic background environment, speed and space constraints, and ease of repair given its remote location. The resulting design achieves good modularity and packing density by putting 24 channels of readout and digitization per module. The digitized data are sent to CAMAC-based memory located near the counting house of the Mark II detector.

Front End Electronics

The WISRD readout system comprises an RF cabinet next to each WISRD detector connected by a 25-pair cable to a CAMAC-based control and readout crate in a CAMAC branch of the Mark II Detector readout system. Each RF cabinet is stainless steel with continuous Cu-Be leaf spring shielding gaskets in all openings (Equipto Electronics Corporation R3 type EMI/RFI cabinet) and contains a Eurocard crate, a power supply chassis, fans, EMI filters on the 115 VAC power, EMI filters on the DC voltages (+5V, ±15V, ±9V) and common-mode suppression on all signals between the RF cabinet, the CAMAC crate and the detector. The Eurocard crate contains modules described below. Connection to the detector is made by eight cables 20 feet long, each comprising 25 coaxial cables (RG-174), in an overall shield of Zippertubing.®

The Eurocard crate contains eight DAQ modules, one Analog module and one Calibration/Communication module. Each is of a 6 U double-width format, providing two backplane connectors of 32 pairs each. One backplane connector receives bussed power, calibration and control signals. The other is used for routing individual interconnections. (See Figure 3.) Each wire array is attached to four DAQ modules.

The DAQ module block diagram is shown in Figure 4. It contains:

* 24 channels of charge-sensitive preamplifiers (LeCroy HQV-820) and shaping amplifiers.
* summing circuitry to generate two linearly weighted sums using the outputs of the shaping amplifiers.
* an Analytek AN-201 Calorimetry Data Unit[3] (CDU): an analog memory which acts as a multi-channel sample-and-hold and multiplexer.
* a Burr-Brown ADC804 serial output 12-bit ADC.
* a Signetics 82S105 FPLS sequencer which coordinates the CDU and ADC and encodes the serial data for transmission.
* attenuation and distribution for each of four bussed calibration lines.

The shaping amplifier output peaks at 5 μs in response to a step-function input. The equivalent noise charge evaluated at the output of the shaping amplifiers is about 1 fC. These outputs couple to the CDU and the weighted sums.

On each beam pulse, the CDU takes two sequential samples per channel. Samples stored in the CDU are read out serially. The output of the CDU is a differential current which is coupled through a differential-current to voltage converter to the ADC. The nonlinearity of the CDU is five percent, as referenced to a line through endpoints of the transfer function over a dynamic range of 300 fC.

FRONT END ELECTRONICS

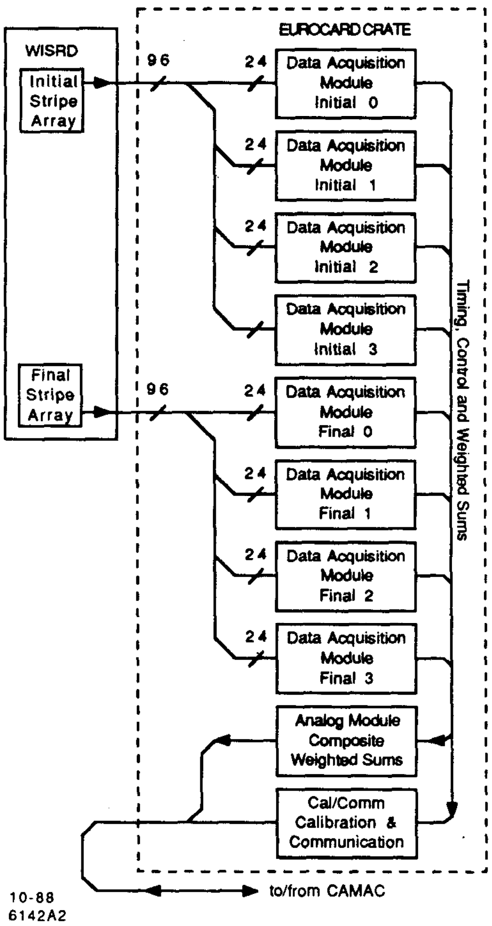

Fig. 3. The Front End Electronics is located in an RF enclosure near each of two detectors, and communicates with electronics in a single CAMAC crate located near the Mark II Detector, 600 feet away.

The serial data stream from the ADC is processed by the sequencer which forms a message consisting of a leading one bit, 12 data bits, and a trailing parity bit. These bits are then Manchester encoded for transmission. This sequencer also generates the control timing for the CDU readout and ADC conversion.

The summing circuitry generates its two weighted sums, a and b, as follows: Given a charge distribution across the subarray of wires associated with a DAQ module, $q_1, q_2, ... q_{24}$:

$$a \propto \sum_{k=1}^{24} k \cdot q_k \qquad b \propto \sum_{k=1}^{24} (25-k) \cdot q_k \quad .$$

The sums from individual DAQ boards are combined by the Analog module to form composite weighted sums, A_m and B_m (middle) over the central 48 wires, and A_t and B_t (total) over the entire 96 wires in an array. The ratio $A-B/A+B$, either over the middle or the entire array, provides a measure of the deviation from the nominal stripe position in each array. The composite sum waveforms are transmitted back to the control room for viewing on an oscilloscope for diagnostic purposes. These signals provide an estimate of the charge yield of the wires and can be used to make a relative measure of the beam energies in real time.

DATA ACQUISITION MODULE BLOCK DIAGRAM

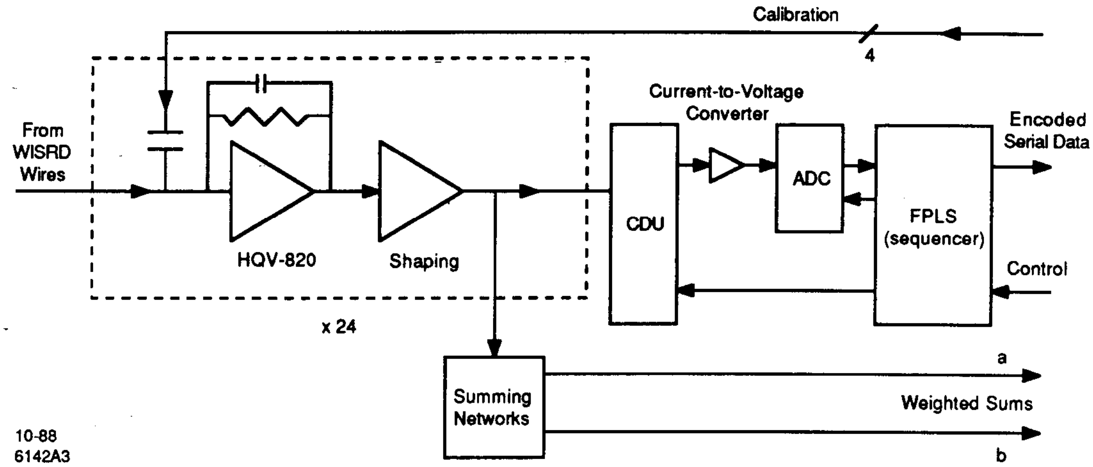

Fig. 4. The Data Acquisition Module receives signals from 24 wires in the WISRD array, amplifies and shapes the signals, and stores two samples of each shaped output in a parallel-in, serial-out analog memory (CDU) on every beam crossing. After data acquisition, the analog samples are digitized and Manchester-encoded for transmission. The Data Acquisition Module also forms two weighted sums of the charge distribution on its wires.

The Eurocard crate is connected to the CAMAC-based control and readout using the Calibration/Communication module (in the Eurocard crate). The Cal/Comm module receives calibration and control signals and buffers them onto the backplane of the Eurocard crate. It converts the TTL-level messages from the DAQs into low-impedance differential signals for transmission back to the CAMAC readout electronics and provides a local clock for the DAQ module sequencers.

CAMAC Readout Electronics

The CAMAC crate contains one Timing Generator module, two Cable I/O modules and eight Two-Channel FIFO modules. Each WISRD requires a Cable I/O module and four Two-Channel FIFOs. The Timing generator is common to both WISRDs. The Cable I/O modules are connected to their respective cables via a formatting chassis which provides common-mode suppression of all analog and digital signals. (See Figure 5.)

Each Cable I/O module interfaces its long cable to associated FIFO modules via front panel LEMO connections and to the Timing Generator via an Auxillary Timing Bus (ATB) on the CAMAC P2 connector. In response to timing signals, the Cable I/O module sends command and control signals to its Cal/Comm module. It also provides a calibration voltage. In addition, it can substitute test data blocks loaded from CAMAC for the data from the DAQ modules for diagnostic purposes.

The Two-Channel FIFO module decodes incoming messages and detects errors. In response to control signals on the ATB, the data of each decoded message are written into a FIFO memory 16 bits wide by 64 words deep. The data is stored in the lower 12 bits with any errors identified in the most significant four bits.

The Timing Generator module accepts a data record written from CAMAC describing a pulse train 16 bits wide and, in response to a beam-crossing signal, asserts the pulse train on the ATB. The data record consists of up to 1024 pairs of 16-bit words. Of the pair, one word contains the data to be asserted

CAMAC ELECTRONICS

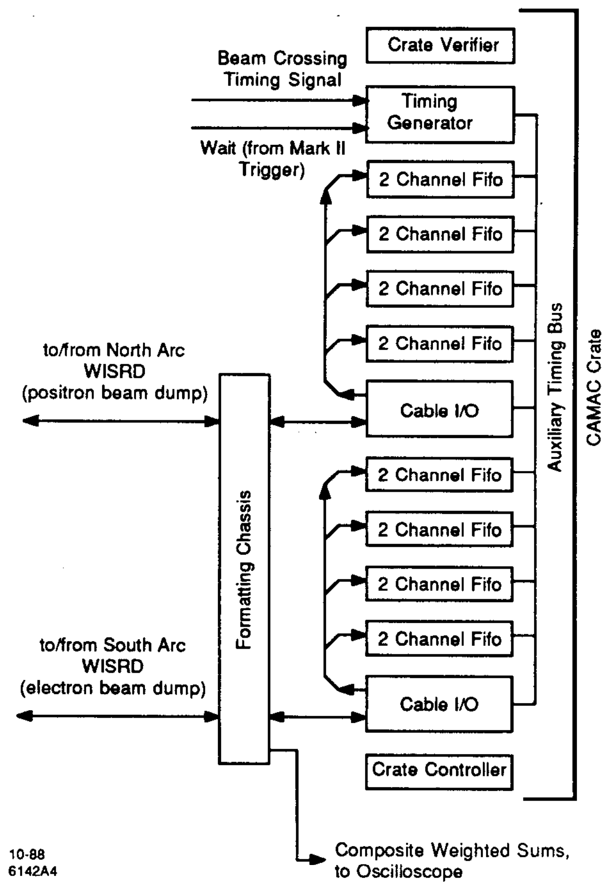

Fig. 5. A single crate of CAMAC modules services both WISRD detectors. The Timing Generator receives through CAMAC a list describing its output sequence. On every beam crossing, it asserts its output sequence on the Auxiliary Timing Bus. These signals comprise timing and control for the other CAMAC modules and, through the Cable I/O modules, to the Front End Electronics. Encoded data from the two detectors are decoded and stored for readout in the two-channel FIFO modules.

and the other word contains a counter value which triggers the output of the next pair. A local 8 MHz clock drives the counter.

Results

The time between the beam crossing and completion of data acquisition into CAMAC is 1.1 ms providing beam pulse energy measurements at the maximum accelerator repetition rate of 180 Hz for every event logged by the Mark II Detector. Digital message transmission has been exercised, with no message errors in more than 5×10^6 messages. We have used the composite sum signals to verify a Monte Carlo model of charge yield of one WISRD detector in the beamline. Beam pick-up and other external electronic backgrounds were undetectable.

Conclusion

The Wire–Imaging Synchrotron Radiation Detector Readout system provides a novel high-resolution, pulse-by-pulse measurement of the Stanford Linear Collider (SLC) beam energies by measuring distributions of synchrotron radiation in the Extraction–Line Spectrometers. Full digital implementation of the system is in progress and is expected for the resumption of SLC operation in February 1989.

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