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READOUT AND TRIGGER ELECTRONICS FOR THE TPC VERTEX CHAMBER†

M.T. Ronan, R.C. Jared and T.K. McGathen,

Lawrence Berkeley Laboratory
University of California, Berkeley, CA 94720

A.M. Eisner,

University of California Intercampus Institute
for Research at Particle Accelerators
Stanford, California 94305

W.J. Broeder and G.L. Godfrey,

Stanford Linear Accelerator Center
Stanford, California 94305

Introduction

The TPC/Two-Gamma facility has been upgraded[1] with a Straw Vertex Chamber for high-luminosity running of the PEP storage ring at SLAC. The high accuracy position resolution of the vertex chamber, measured to within about 4 cm of the beam vertex, will provide an impact parameter resolution of less than 90 microns for tracks with momenta greater than 1 GeV/c. When used in conjunction with the Time Projection Chamber, the vertex chamber will allow reconstruction of B meson decay vertices for B lifetime measurements, and tagging of $B - \overline{B}$ events for studying mixing and other properties of b quark systems. In addition, the reconstruction of K^0_S mesons will be improved.

The introduction of the vertex chamber required the addition of new front-end electronics and a new 1024-channel, high-accuracy TDC system. The preamplifier/discriminator should be capable of triggering on the first electrons and the time digitzer should preserve the measurement resolution. For the TDC's, in order to maintain compatibility with the existing TPC readout system, an upgrade of a previous inner drift chamber digitizer system has been chosen. Tests of the accuracy and stability of the original design indicated that the new design specifications would be met.

The TPC detector requires a fast pretrigger to turn on its gating grid within 500 ns of the e^+e^- beam crossing time, to minimize the loss of ionization information. A pretrigger based on the Straw Chamber signals, operating at a rate of about 2 K/sec, will be used for charged particle final states. In addition, in order to reject low mass Two-Photon events at the final trigger level, an accurate transverse momentum cutoff will be made by the Straw Chamber trigger logic.

In this paper, we describe the readout and trigger electronics systems which have been built to satisfy the above requirements.

Straw Vertex Chamber for the TPC Experiment

The Vertex Chamber, designed and built at SLAC, consists of 984 25μm-aluminum-100μm-mylar laminates wrapped as straws, each forming an 8 mm diameter cylindrical cathode with a 30 micron sense wire along the axis. The straw tubes are arranged in 14 layers, with staggered pairs of layers forming doublets and an outer quadruplet for triggering, as shown in the quarter section of Fig. 1. The aluminum chamber ends, held apart by a beryllium (.75 mm) cylinder, are tapered at a 45° angle so that the innermost straw is 39 cm long, while the outermost is 60 cm long. This cylinder slides onto the beryllium (1.0 mm) beam pipe. The beam pipe (4.0 cm radius), stainless steel end walls, and outer carbon-fiber (2.0 mm) cylinder (16 cm radius) form a pressure vessel. Beryllium and carbon-fiber were used to minimize multiple scattering. With Ar-CO_2 gas at 4 atmospheres, the chamber will have a drift velocity of about 60 μm/ns near the sense wire, falling off by more than an order of magnitude near the tube walls. Vertex chambers with a similar design[2] have achieved spatial resolutions of 35-50 microns.

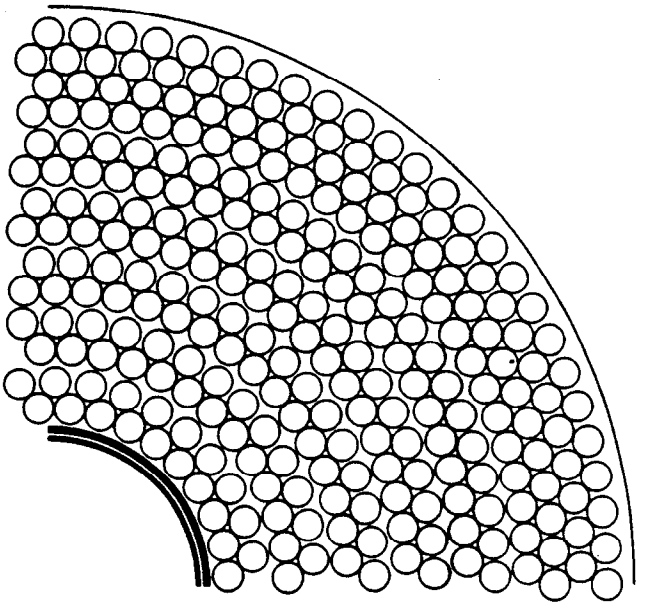

Fig. 1: Quarter section of the Straw Vertex Chamber for the TPC/Two-Gamma facility.

Preamplifier / Discriminator Electronics

Approximately 30 meters of RG174 cable connect the straw chamber to the preamplifiers, with the center conductors at +4.0 KV. The cables are soldered in groups of 8 to cards which handle the HV distribution and decoupling. These cards plug into the 8 channel preamplifier/discriminator cards.

The preamplifier, shown in Fig. 2, consists of a grounded base tran-

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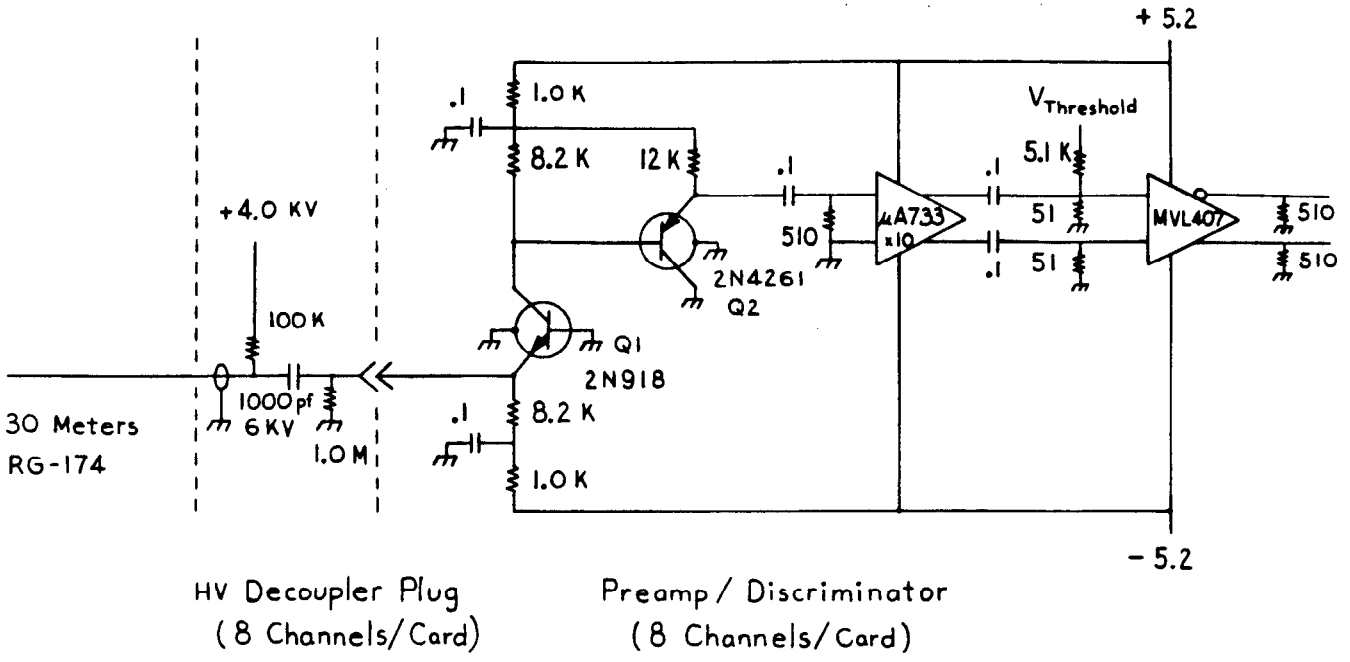

Fig. 2: Straw Chamber front-end electronics.

sistor, Q1, and an emitter follower, Q2, driving a 733 amplifier with x10 gain. The negative charge of the chamber signal is deposited on the collector capacitance of Q1 and base capacitance of Q2, which have been chosen to be small. This few picofarad capacitance discharges through the 8.2kΩ collector resistor and through the buffered 510Ω resistor at the 733 input, thus forming a 20 ns integration time. The 733 provides an additional x10 voltage gain and drives the LeCroy[3] MVL407 comparator whose differential ECL output is carried on twist-flat cable to the Time Digitizer Electronics.

The front-end electronics, which have achieved a threshold of a few femto-Coulombs for the several nanosecond rise-time pulse of the Straw Chamber, were designed and built at SLAC.

Time Digitizer Electronics

To eliminate any significant electronic contribution to the error in the measured position, a time measurement with better than 200 ps accuracy was specified. The need for frequent calibration runs during the experiment would be avoided if a long term stability of better than 200 ps were achieved. A 10-bit dynamic range was chosen to cover the maximum drift time of a Straw Chamber cell, about 360 ns.

Figure 3 shows the essential features of the Time Digitizer Electronics. In operation the reset signal charges the capacitor C8 to three volts before a beam crossing. If an event is present, the Flip Flop will

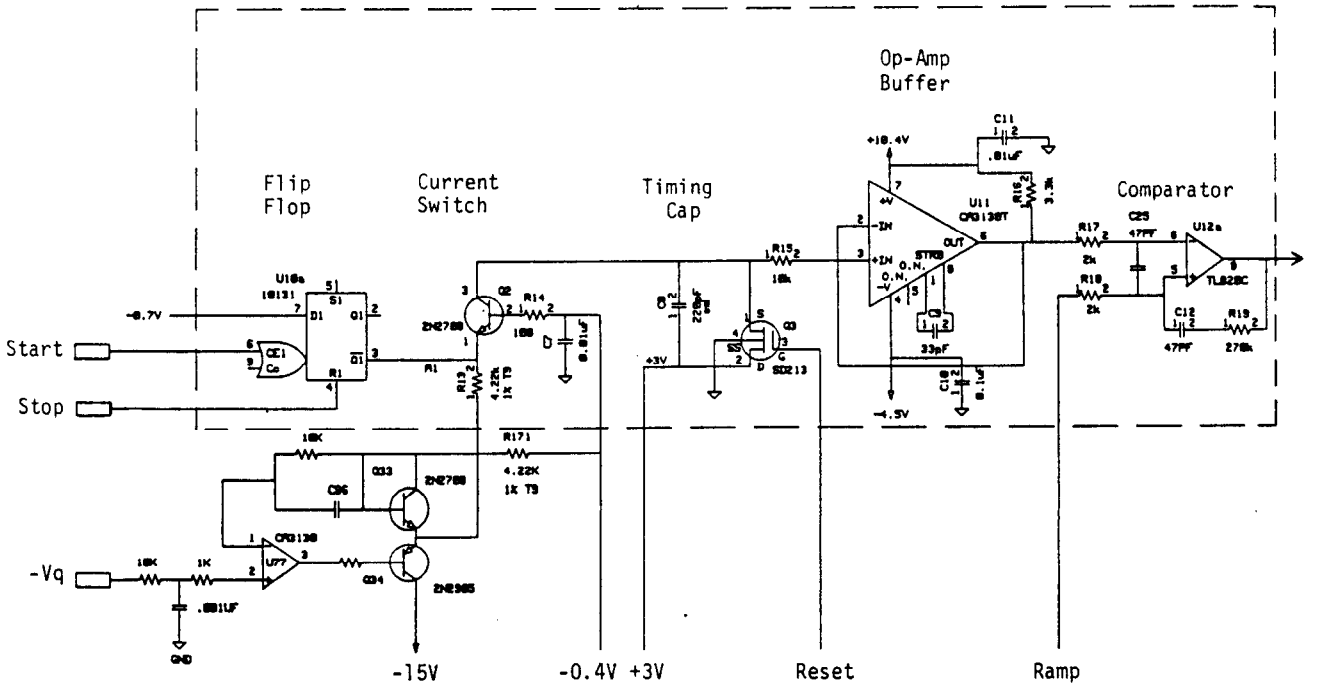

Fig. 3: A TDC electronics channel.

be set by the input signal and then reset by the common stop. Thus the time width of the Flip Flop output will be equal to the drift time. During the time that the Flip Flop is set, a constant current is gated through transistor Q2 to partially discharge C8. This results in a voltage proportional to the drift time plus a constant at one input to the comparator. The amplitude to digital conversion is performed using a standard ramp-counter technique; whereby, a ramp generated synchronously with the enabling of a clock (not shown) is used to latch the clock time when the stored amplitude is crossed, thus forming the output from the time digitizer.

This design is an improved version of an existing drift chamber circuit. The buffer U77 was added for the capacitor discharging voltage Vq. Previously this voltage was common to 16 boards, coming from the control board. The RC network on the input provides AC filtering and the transistor Q33 provides compensation for temperature induced changes to the V_{be} drop of the discharging transistors Q2 on each of the 16 channels.

The digital section (not shown) was changed from 8 bits to 10 bits using a 10 bit CMOS latch, AM29AC821. This chip is equivalent to the 74S374 but uses only 80 μamps. Normally the increase from 8 to 10 bits would increase digitizing time by a factor of four; however, we increased the speed of the digitizer clock from 12.5 MHz to 25 MHz so that the digitizing time was only doubled from 20 μs to 40 μs. This was accomplished mainly with the use of TTL FAST logic, and the short (4 ns) set-up time of the AM29AC821.

The time digitizers for the Straw Chamber have been built to fit within the existing TPC readout system which consists of 35 parallel R/O controllers. The Straw Chamber signals are digitized within 40 μs and are read out by one of the R/O controllers into the TPC data buffer.

The TDC drafting and layout were done on the LBL CAD system, while the 1024 channel system was produced by private industry. Test results showing that the specifications have been met are described below.

TPC Triggering

The TPC Trigger[4] operates with three levels of triggering: a pretrigger stage which selects events of interest within the PEP crossing time interval of 2.45 μs and turns on the TPC gating grid; a second level used for fast digital decisions; and a final trigger level which finds tracks[5] using the full 30 μs of drift information from the TPC. The Straw Chamber will be used at the first level in the required pretriggering, and will provide an accurate transverse momentum decision for additional event rejection.

During the pretrigger decision time, the TPC gating grid is off and ionization drifting into the endcap sectors is lost. In addition, for 1 μs after gating the electronic noise is above zero suppression levels so that readout is inhibited. The overall pretrigger decision is made within 500 ns to minimize the loss of TPC information before readout begins. The Straw Chamber trigger logic uses signals from 480 tubes in 96 channels of fast digital and analog circuitry, each representing an interval in azimuthal angle, to define single-track candidates. This logic is described below. The multiplicity of tracks and their azimuthal locations will be used to form the pretrigger decision, and, together with with signals from the TPC and other detector components, the various trigger definitions.

The Straw Chamber trigger information is read by a R/O controller in parallel with the TDC digitizer readout. This will enable us to later introduce a fourth level of triggering using a microprocessor to access the Straw Chamber digitized data and the full TPC trigger readout list in order to improve the trigger decision for high luminosity running. These data would be available within about 100 μs, thus allowing the dead time to be reduced by rejecting uninteresting events before the TPC signals stored in CCD's have been digitized.

Vertex Chamber Trigger Electronics

The rate of background tracks at PEP, both from physics and machine sources, is expected to be a steeply falling function of p_T. To reject low p_T backgrounds at the trigger level, the outer four layers (11-14) of straw tubes have been arranged to form a close-packed quadruplet; and two inner layers (3-4), each of which has exactly half as many straws as a quadruplet layer, have been arranged in phase with the quadruplet. Azimuthally-restricted coincidences between layers can then be used to require near-radial tracks, as expected for high-p_T particles in the 13.25 kilogauss field of the TPC's superconducting solenoidal magnet. For a track originating along the beam line, $\Delta\phi$, the change in azimuth between the track's positions in two different layers, is proportional to $1/p_T$. Hence a maximum-$\Delta\phi$ cut imposes a minimum p_T. In addition, radial tracking roads tend to reject tracks which do not originate from along the beam line.

We have devised a trigger which uses the four outer and two inner layers to implement such a cut. First, detailed timing coincidences between azimuthally aligned layers of the outer quadruplet are used to identify radial track candidates. Figure 4 shows the outer layers, labeled a–d, and a high p_T track, labeled #1. As seen from the expected timing of detector signals for such a track, as indicated in Fig. 4, a time coincidence between the 'a' and 'c' layers requires a near-radial track. The result is a very sharp p_T cut, and one which is adjustable by controlling coincidence widths. However, left-right ambiguities allow a substantial fraction of low-p_T particles to "sneak in". This occurs when a track crosses the plane formed by the sense wires, as illustrated by Track #2 in Fig. 4.

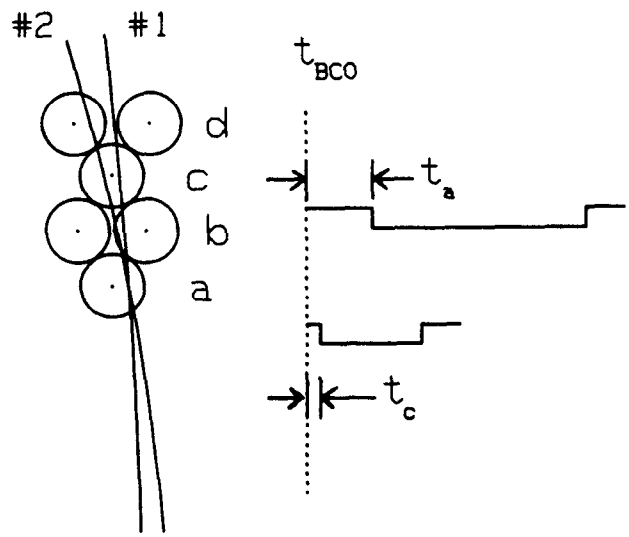

Fig. 4: Single-track trigger, quadruplet time-coincidence, which selects tracks of high-p_T, as illustrated by the 300 MeV/c track #1. Track #2 with a p_T of 125 MeV/c but the same drift times as track #1 in layers 'a' and 'c' illustrates the left-right ambiguity.

We then apply a constraint utilizing coincidences between inner and outer layers, with the straws subdivided by timing windows into subcells. For a given outer-layer subcell, specifying a limited range of inner-layer subcells implies a $\Delta\phi$ cut or, equivalently, a cut on the sagitta of a track defined by the outer-layer hit and the beam vertex constraint. This is illustrated in Fig. 5, which shows the same two tracks as in Fig. 4. The inner-outer coincidence logic (which by itself could be used for selecting tracks) can definitively reject low p_T tracks. However, because of the subcell sizes, its p_T threshold is not extremely sharp and can be varied in only a few quantized steps.

The use of the time-coincidence logic in conjunction with the cell-subdivision logic provides a sharp tunable transverse momentum threshold, without the low P_T acceptance arising from left-right ambiguity. Figure 6 displays the expected trigger efficiency vs. p_T for a nominal threshold of 200 MeV/c. (This curve and curves for a variety of other possible trigger definitions have been calculated by using a Monte Carlo technique to simulate hits in the Vertex Chamber for tracks passing through our detector.)

Implementation is via time coincidences, as described in the next section, and table look-up, keying on outer layer hits, in one 16384 x 4 RAM for each straw in layer a or b of the quadruplet. The extra three RAM outputs will encode supplementary track definitions which can be used in higher-level logic.

Because there is a possibility that high backgrounds could sometimes make the use of the inner layers difficult, we have also designed an alternative requirement which is capable of resolving most of the ambiguous tracks selected by the quadruplet timing logic. By additionally requiring a hit in the intermediate layer, e.g. layer b in Fig. 4, within a time window of the beam crossing, one rejects ambiguous tracks which either pass through the gap in the intermediate layer or arrive late. This combination provides considerable low-p_T rejection, although not as much as that illustrated in Fig. 6.

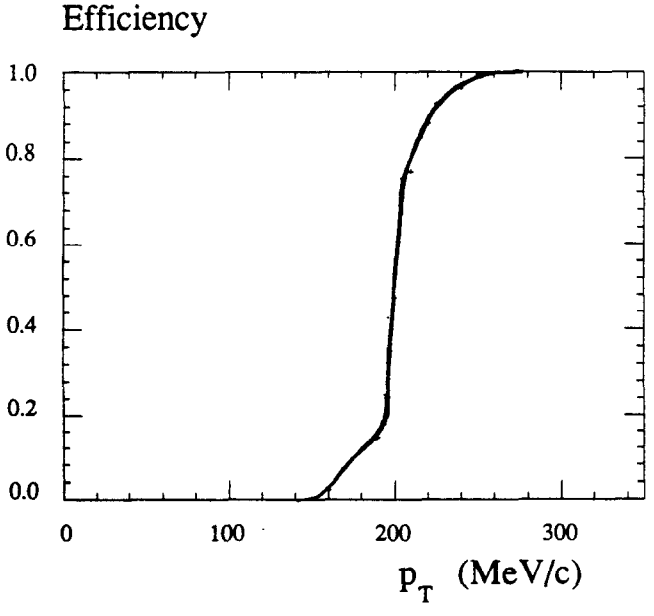

Fig. 6: Expected trigger efficiency as a function of transverse momentum, for a nominal threshold of 200 MeV/c.

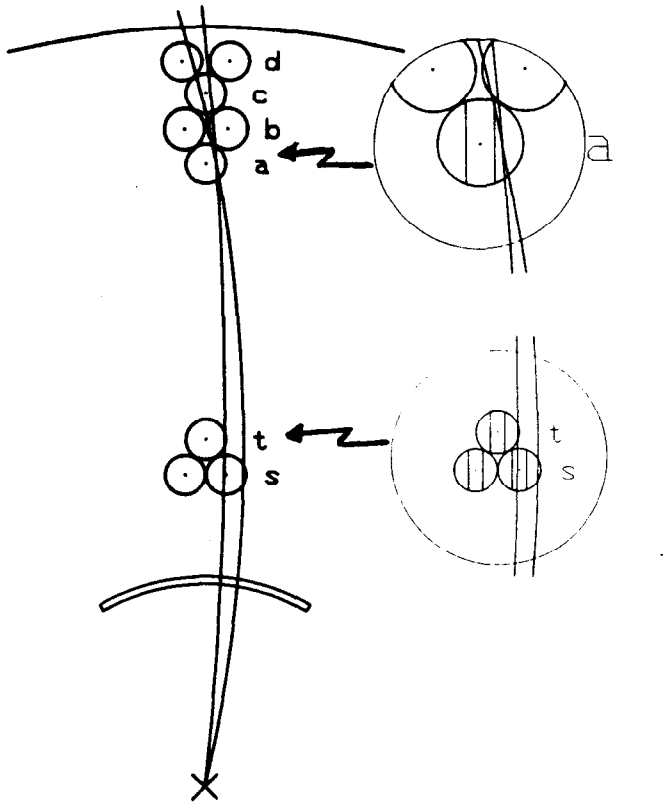

Fig. 5: Vertex Chamber single-track trigger, inner-outer coincidence (or sagitta restriction). The two tracks are the same as those shown in Fig. 4.

Variable Coincidence Width Circuitry

Implementation of the time-coincidence logic has one significant complication. The large electric field variation in the cylindrical straw tubes leads to a non-saturated drift velocity which varies with distance from the sense wire. To define a constant radial tracking road in the outer four layers of the chamber, we have designed a coincidence circuit in which each input pulse width varies as a function of the pulse time. (The function is different for each of the layers a to d, because each has a different ratio of azimuth to drift distance.)

The variable coincidence is accomplished with the circuit of Fig. 7. A ramp representing the variation of pulse width with position in the cell, or drift time, is generated on an external board and buffered to all variable coincidence channels. The ramp is applied to the base of transistor Q101a which forms a coupled emitter pair with transistor Q101b. The emitter of Q101a follows the ramp and charges up the timing capacitor, C104, which has its other side held by a Schottky diode. The Schottky diode was chosen to reduce the error introduced by diffusion capacitance. When the data pulse comes into the gate of the MOSFET, Q102, the base of transistor Q101b is pulled down. This in turn pulls the capacitor down, driving the input of the high speed comparator negative, thus changing its output state. The Schottky diode turns off, allowing the pull-up resistor R109 to discharge the capacitor at a nearly linear rate, until it passes back through the threshold of the comparator, completing the pulse width generation. Notice that while the capacitor is discharging, its other end is held fixed by the emitter of Q101b. Thus, the output width is derived from the ramp

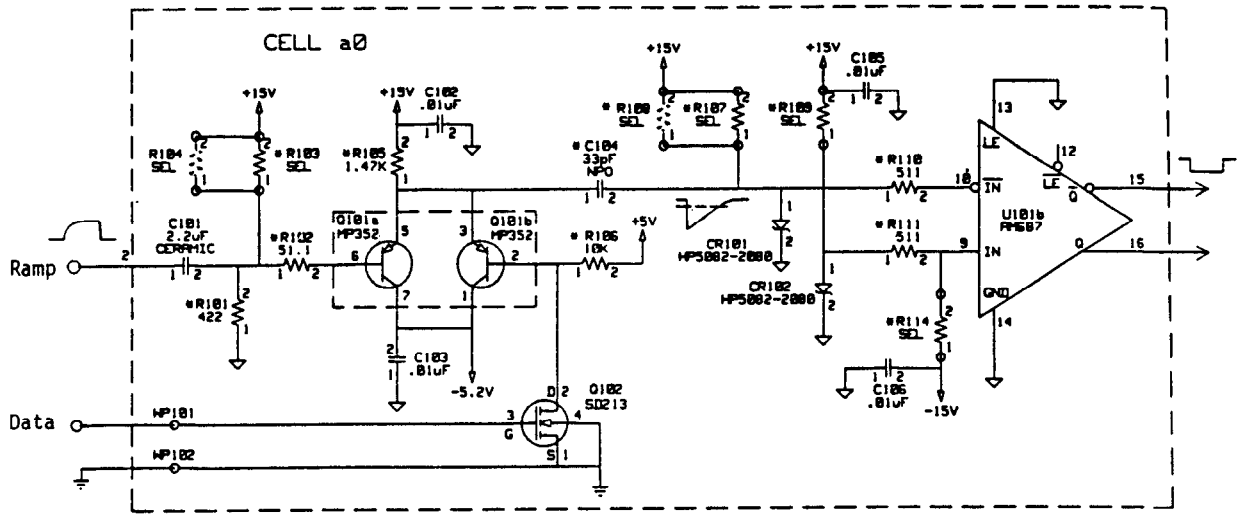

Fig. 7: Variable Pulse Width circuit.

input at the time of the data input and is then used in circuitry (not shown) to form the time coincidence.

As with the TDC's, the 96 channels of fast trigger logic on 48 circuit boards were designed at LBL and produced by private industry.

Test Results

The TDC's have been tested and calibrated using a high accuracy test pulse system and software which has evolved from the TPC detector calibration system. The test pulses are derived from an extremely stable, 100 MHz oscillator and are sent at 10 ns increments covering the full range of the digitizer. Figure 8 displays the calibration result for a quadratic fit of one channel of the 1024 channel system. We obtain resolutions of better than 150 ps with a maximum deviation from linearity of less than 0.1% of full scale. Also, a stability of less than 150 ps has been measured for over a week of operation. The calibration software is capable of performing polynomial, multilinear or spline fits to the calibration data, and automatically adds pointers and new calibration parameters to a time-ordered data base when individual boards are replaced and recalibrated.

We have used a single exponential waveform to control our variable coincidence logic and have tested its operation over the expected drift time of the straw tubes. Digital test pulsing with separate time controls for each layer has been used to test the trigger logic in situ. The final pulse-width control waveform may be more complicated. It will be adjusted by component selection for the desired p_T threshold after the chamber drift velocity is measured, while the trigger logic settings will be programmed through computer controls into the trigger RAM's as we obtain experience with the high-luminosity PEP storage ring.

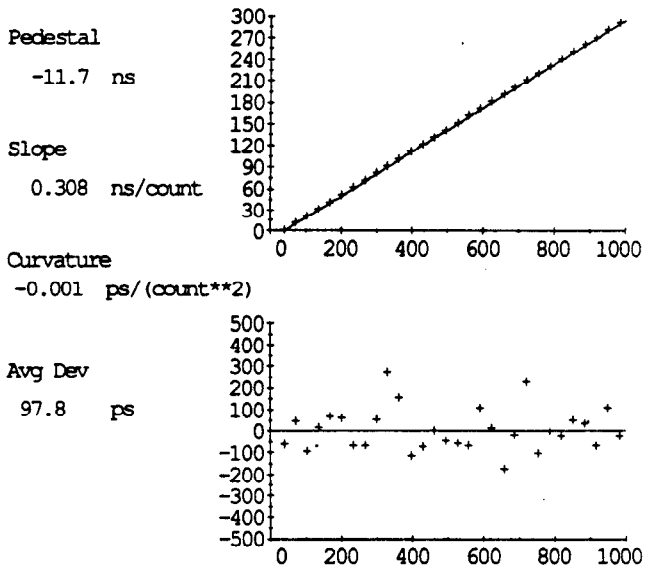

Fig. 8: A typical TDC electronic calibration result. The upper plot shows time in nanoseconds vs output channel, while the lower shows the deviation in picoseconds from the quadratic fit.

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References

1. "Letter of Intent for PEP/TPC High Luminosity Running and TPC Vertex Chamber Proposal", Internal TPC report TPC-LBL-85-20 (1985).

2. W.W. Ash et al., SLAC-PUB-4311 (1987), Submitted to Nucl. Instrum. Methods.

3. LeCroy Corporation, Spring Valley, N.Y.

4. M. Ronan, "The PEP-4 (TPC) Trigger System", Internal TPC report TPC-LBL-87-12 (1987).

5. M. Ronan, J. Millaud and T. McGathen, IEEE Trans. Nucl. Sci. NS-29, 427 (1982).