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RADIATION DAMAGE STUDIES OF A CUSTOM-DESIGNED VLSI READOUT CHIP*

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ABSTRACT

Two structurally similar versions of an NMOS custom VLSI circuit, manufactured at different foundries, have been irradiated with a ^{60}Co source up to doses of 100 krad. Large differences in their behaviour after irradiation have been seen which are thought to be due to the fabrication processes. These differences are observed in test structure measurements and overall chip performance. An increase in circuit noise causes one version of the chip to be unusable after radiation doses of 20 krad.

Introduction

We are planning to use a custom very large scale integrated circuit ("Microplex") [1-3] as a multiplexing readout for silicon strip detectors to be used in the Mark II experiment at the SLAC Linear e^+e^- Collider. The radiation levels expected during normal operation are less than a mrad/hour, but beam tuning and instabilities may cause short periods with levels at many orders of magnitude higher. This paper represents a continuation of the work presented in reference [4], where it was shown that version 2 of the circuit could survive doses up to 100 krad if not powered during irradiation. A more recent version of the Microplex circuit, version 3, has since been manufactured and tested. We present here a comparison of the radiation hardness of the two versions.

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Circuit Description

The Microplex chips were fabricated according to 5 μm NMOS design rules. The main features of the circuit are shown in figure 1. The chip integrates and stores the charge from 128 input channels via a charge sensitive amplifier onto double correlated sample and hold circuitry. The signals are then multiplexed to a pair of output buses under the control of a shift register. There are also several test structures on each chip. The changes to the circuit in the design of Microplex 3 were minor. These changes are not thought to be relevant to the radiation hardness properties, except that the position of a gate in the shift register was changed so that Microplex 3 could operate with the substrate bias at ground rather than a bias of ~ -3V, as required for Microplex 2. However, the fabrication processes were different. Most of the details of the manufacturing steps for Microplex 3 are not known to us. However, two known differences which may possibly be significant are

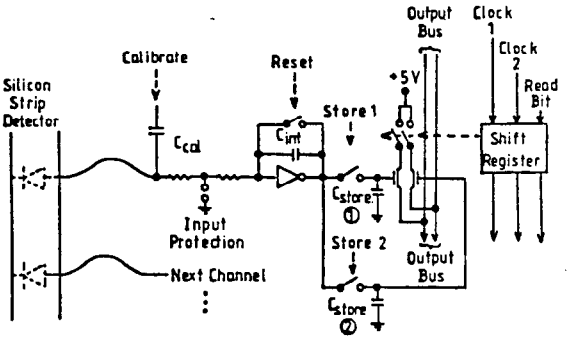

Figure 1. Block diagram of the Microplex circuit

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that Microplex 3 has a field oxide of twice the thickness of Microplex 2, and that Microplex 2 has no protective overglass, while Microplex 3 has a silicon nitride scratch mask covering the chip. Note that the thicker field oxide required the lengths of several of the capacitors on Microplex 3 to be doubled. The Microplex 2 chips were manufactured at the Stanford Integrated Circuits Laboratory, Stanford University, while Microplex 3 were made by Gould-AMI, Santa Clara.

The analog and digital sections of the circuit operate independently. The analog section will be powered for several microseconds around the time of a beam crossing, when a signal is expected. The digital section is powered on later, if readout is required. Radiation damage is therefore only expected to occur in the digital section while it is turned off. Furthermore, if radiation levels are high, then all power to the ciruit will be cut off. Hence, most of the radiation dose is expected to be received while the circuit is unpowered and the measurements presented here reflect this expectation.

Description of Measurements

The overall circuit performance and the characteristics of several test structures on each chip were measured as a function of radiation dose up to 100 krad. The chips were irradiated with a ^{60}Co source of average strength 460 ± 50 rad/hour over the time of these measurements. For the results presented here, unless specified otherwise, all connections to the chip, including the test structure contacts, were grounded while being irradiated.

The test structures used were MOSFET's of several sizes. The threshold voltages of each structure at different radiation doses were measured from the characteristic in the saturated region. The characteristic was measured using standard CAMAC modules controlled by a VAX 11/750 computer. For all measurements, the drain was held at +2V and the source and substrate were connected to ground. The gate voltage was varied in steps of 0.02V and the drain-source current measured from the voltage drop across a resistor. A straight line fit over 40 points (0.8V) to the square root of the current versus the gate voltage defined the threshold voltage as the intercept of the fitted line at the gate voltage axis. An example is given in figure 2, where the characteristic for an enhancement MOSFET with a channel width of 100 μm and channel length of 5 μm (W/L = 100/5) and the resulting linear fit are shown.

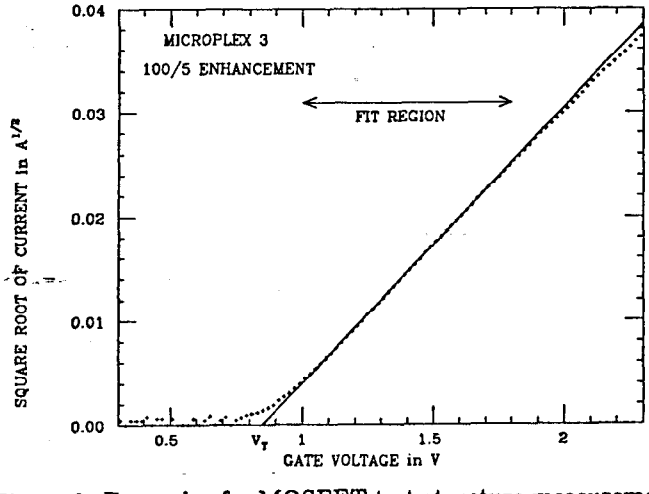

Figure 2. Example of a MOSFET test structure measurement to determine the threshold voltage, V_T. The MOSFET had a width of 100 μm and a length of 5 μm (100/5). The straight line shows the linear fit.

In addition, a gain cell was formed from two of the MOSFET test structures, a 100/5 enhancement and a 25/5 depletion connected as shown in figure 3. This gain cell structure is used in each stage of the analog amplifier. The operating point of the gain cell, defined as the voltage at which the input and output levels are equal, was measured. The gain of the cell at the operating point was also measured.

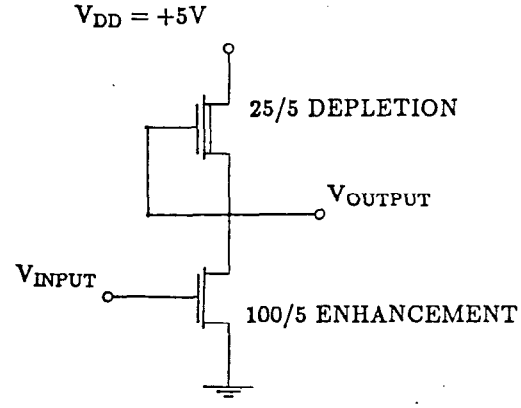

Figure 3. Diagram of the gain cell structure made from an enhancement and a depletion MOSFET.

The overall chip performance was evaluated by applying a calibration pulse via a capacitor at each channel input. The digitisation and readout were again performed using a CAMAC system. The chips were not connected to silicon detectors for these tests. The size of the calibration pulse used was 600 mV. This corresponds to a signal of $\sim$ 40 thousand electrons for a Microplex 2 chip and $\sim$ 20 thousand electrons for Microplex 3. The noise of each channel was defined as the root mean square of the fluctuations in the pedestal level and the signal as the pedestal-corrected mean pulse height of the channel.

Test Structure Results

The threshold voltages for 100/5 enhancement, 5/5 enhancement and 25/5 depletion MOSFET test structures as a function of radiation dose are shown in figure 4 for two typical chips. The chip-to-chip variations were bigger for Microplex 2 than Microplex 3 and this was characteristic of all measurements. The most obvious difference between Microplex 2 and 3 is that the enhancement threshold voltages decrease monotonically with dose for Microplex 2, but have a minimum before a slow increase for Microplex 3. It is also seen that Microplex 2 shows a decrease in threshold voltage of $\sim$ 3V for the smaller enhancement MOSFET, and $\sim$ 1V for the larger one, while Microplex 3 has approximately equal changes for both enhancement MOSFET's. Hence, it is seen that Microplex 2 shows significant edge effects. In addition, large drain-source leakage currents, between 10 and 100 μA, were observed in Microplex 2. These leakage currents had a strong dependence on the substrate bias and decreased to a negligable size for the bias values used when actually operating the chip (see below).

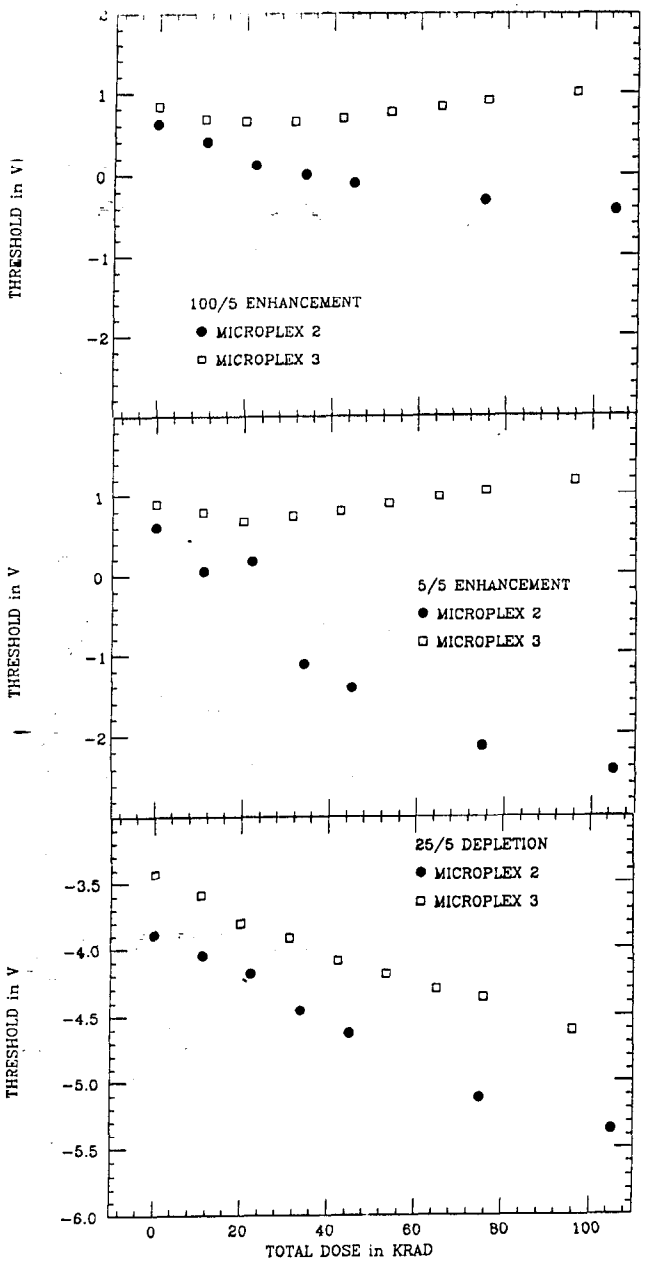

Figure 4. Threshold voltage as a function of radiation dose for 100/5 enhancement, 5/5 enhancement and 25/5 depletion MOSFET test structures on Microplex 2 and 3.

The operating point of the gain cell as a function of radiation is shown in figure 5. The changes are consistent with the measurements of the individual structures. The gain of the cell at the operating point as a function of dose is shown in figure 6. Both versions show a decrease in gain of $\sim$ 40 - 50% after a dose of 100 krad.

Damage to the Digital Section

The damage to the digital shift register was characterised by the register output, the Read-Bit-Out (RBO). During correct operation, a single bit is clocked through the shift register and emerges at the register output after all channels have been multiplexed to the buses. However, if the register is faulty, then either multiple or no RBO's are produced. This is thought to

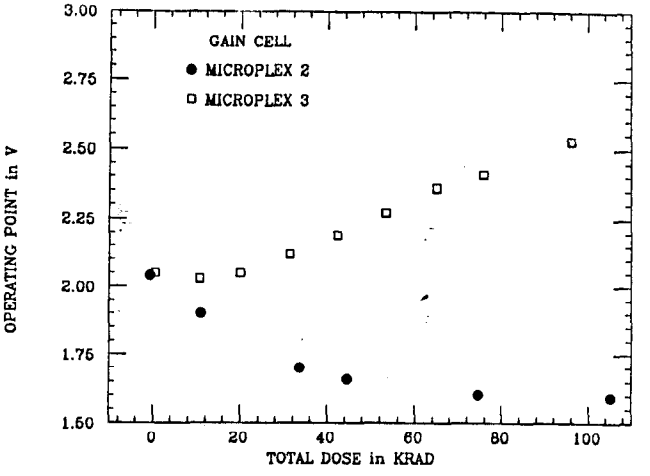

Figure 5. Operating point as a function of radiation dose for gain cell test structures on Microplex 2 and 3.

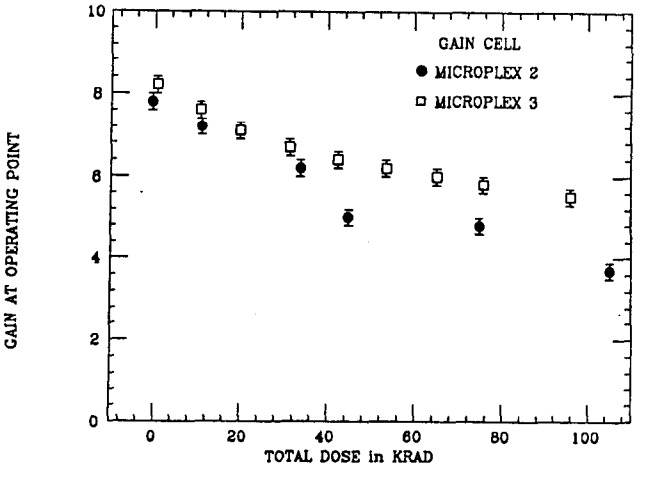

Figure 6. Gain at operating point as a function of radiation dose for gain cell test structures on Microplex 2 and 3.

be because the threshold shifts have caused the logical state of one or more stages of the shift register to be incorrectly set. This bit will then either turn on a channel which is supposed to be off, or vice versa. In practice, the correct functioning of the shift register is controlled by the substrate bias. The substrate bias used is always negative, and increasing the magnitude of the bias voltage increases the thresholds of all the MOSFET's on the chip. Therefore, the radiation-induced threshold voltage shifts can be compensated for by changing the substrate bias. Because of these effects, the shift register will only operate correctly over a certain range of substrate bias voltages and this range will change with radiation dose. It was found that Microplex 2 always required a minimum non-zero substrate voltage, even without any irradiation, but then would function correctly up to the highest values used, ~ -20V. In contrast, Microplex 3 would only operate with a bias between ground and some maximum value. These limits on the substrate bias, a minimum for Microplex 2 and a maximum for Microplex 3, are shown as a function of radiation dose in figure 7. It is seen that the minimum substrate bias needed for Microplex 2 increases steadily with radiation dose. This is to compensate for the decrease of the thresholds due to radiation. Similarly,

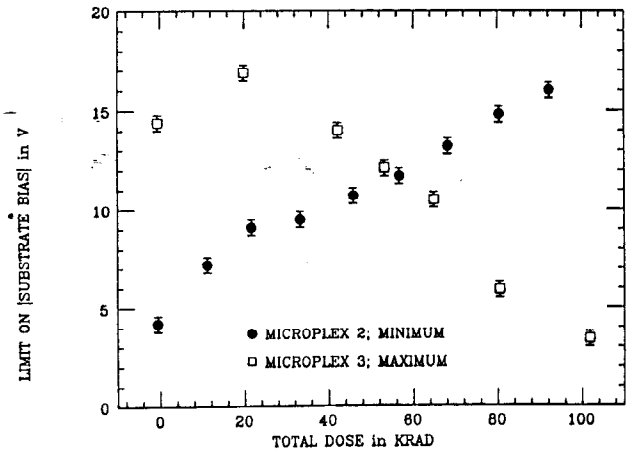

Figure 7. Limits on the substrate bias required for correct functioning of the shift register. The value represents the minimum magnitude needed for Microplex 2 and the maximum for Microplex 3.

the maximum voltage allowed for Microplex 3 decreases because the threshold voltages mainly increase. Hence, the shapes of the curves are qualitatively consistent with the measured MOSFET threshold changes. For radiation levels up to at least 100 krad, it is seen that satisfactory digital operation is possible with substrate bias adjustment for both versions.

Damage to the Analog Section

Radiation damage to the analog section also results in very different behaviour for the two versions of the chip. After modest doses of 10 krad, Microplex 3 chips were observed to have an amplifier output level close to 0V, with a small observable signal. The amplifier was not operating in the linear region and this meant the signal gain was decreased by an order of magnitude from its unirradiated value. This effect did not normally occur in Microplex 2, although one chip tested showed similar behaviour. For the damaged chips, a pulse was applied to the substrate such that the falling edge occured in the time interval when both parts of the double correlated sample and hold circuit were integrating charge. The pulse capacitively couples to the amplifier stages, the dominant effect being to the first stage, as it is then amplified. This effectively adds a large signal, which shifts the input level so that the amplifier is operating in its linear region. This "signal" is cancelled by the differential output. The pulse size required to enable the circuit to function correctly is shown as a function of radiation dose in figure 8. There was considerable freedom to select the combination of constant substrate bias and pulse magnitude, so the values shown are the ones used for the noise measurements described below. The size of the pulse used is seen to increase steadily for Microplex 3 chips, up to a value of $\sim$ 0.25V at a dose of 100 krad. No pulse was required for most Microplex 2 chips, as mentioned above. This effect in Microplex 3 is not simply related to the threshold shifts measured and is not understood. However, the damage can be compensated for by pulsing the substrate voltage up to radiation doses of at least 100 krad.

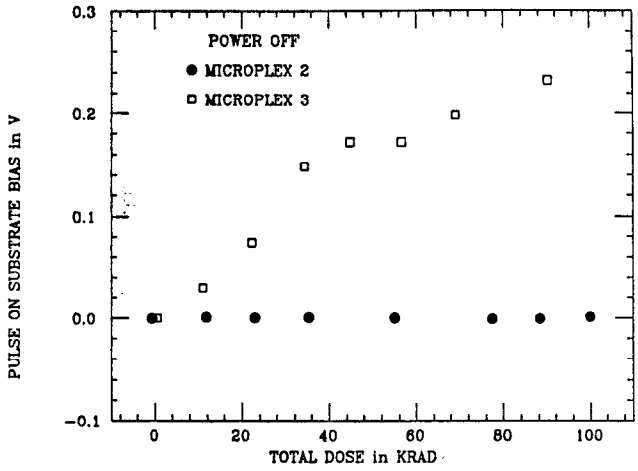

Figure 8. Magnitude of the pulse used on the substrate voltage to correct the amplifier operating level as a function of radiation dose.

Increase in Noise

There is another effect of radiation in the analog section, which is an increase in noise. The noise to signal ratio is a good measure of the equivalent noise charge (ENC) at the amplifier input, since in the linear region, changes in gain due to radiation cancel in this ratio. The ENC is therefore assumed to be proportional to the noise to signal ratio. The ENC of the unirradiated Microplex 2 chips is $\sim$ 500 electrons and for Microplex 3 is $\sim$ 300 electrons. The average ENC of the working channels on the chip, normalised to the value of the ENC of the unirradiated chip, is shown in figure 9 as a function of dose. The error bars indicate the rms spread in values of the individual channels around the mean. It is seen that the noise of Microplex 2 slowly increases by $\sim$ 20% over 100 krad, whereas Microplex 3 has a rapid rise by a factor of $\sim$ 4 over the same range. In practice, this would make Microplex 3 unusable after a dose of $\sim$ 20 krad, where the ENC has doubled. The increase in noise is not understood and there is no known way to reduce it on the present chips. This damage therefore represents the limiting factor on the radiation hardness of the chips.

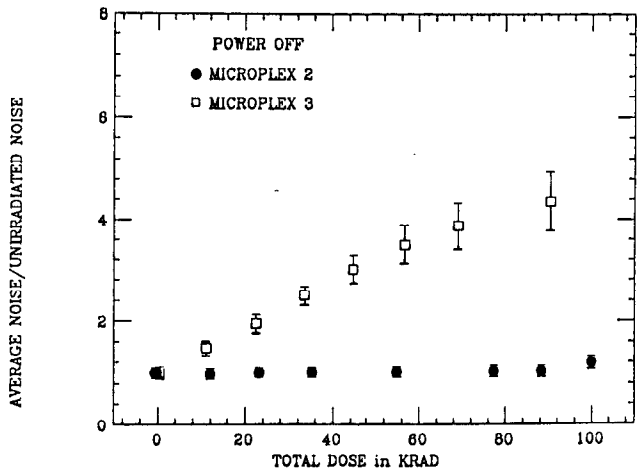

Figure 9. Equivalent noise charge for Microplex 2 and 3 as a function of radiation dose. The ENC is divided by the value for the unirradiated chip.

Powered Irradiation Studies

Since some irradiation may occur while the circuit is under power, damage to the circuits under this condition was also studied. Specifically, the analog section was turned on and the digital section was grounded. However, to avoid possible damage from heating, the power was pulsed with a 25% duty cycle at a frequency of 50 kHz.

The results of the digital section were unchanged, as would be expected, but the analog section behaved differently. The magnitudes of the substrate pulses used is shown in figure 10. Note the change in scale compared with figure 8. Both chips now require pulses, but with opposite polarities. The output of Microplex 3 is at a low voltage, as for unpowered irradiation, while Microplex 2 saturates with a high output level. In addition, the amplitudes of the pulses required are larger.

Figure 11 shows the normalised ENC values as a function of radiation dose. Microplex 2 shows a faster increase in noise than for the unpowered case, which would make it unusable for radiation doses above ~ 60 krad. The rate of increase in noise of Microplex 3 is only slightly higher than for the unpowered case. Extrapolating these values to a 100% duty cycle, Microplex 2 would be expected to be useful up to ~ 16 krad, and Microplex 3 up to ~ 13 krad, if powered continually during irradiation.

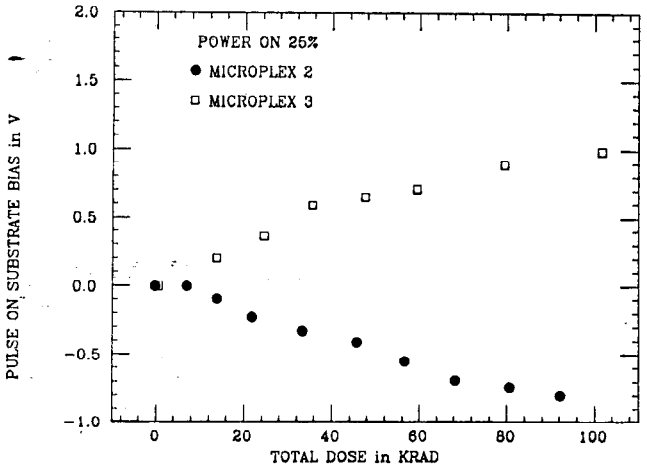

Figure 10. Magnitude of the pulse used on the substrate voltage to correct the amplifier operating level as a function of radiation dose. The chips were irradiated with power on at a 25% duty cycle.

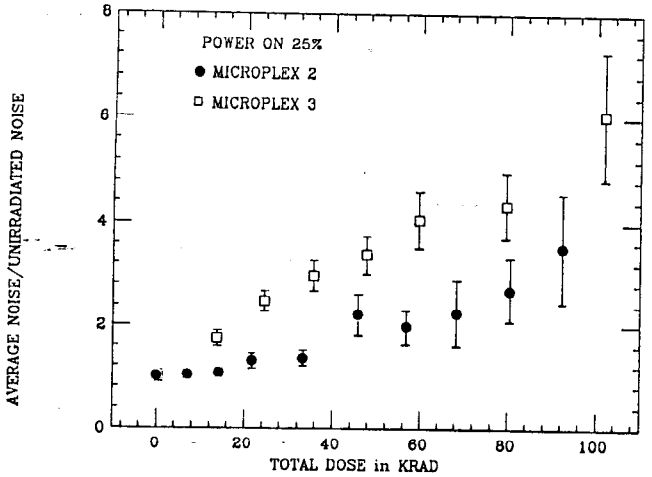

Figure 11. Equivalent noise charge for Microplex 2 and 3 as a function of radiation dose. The ENC is divided by the value for the unirradiated chip. The chips were irradiated with power on at a 25% duty cycle.

Conclusions

The two versions of the Microplex chip used here have very similar circuits, but show large differences in their radiation hardness properties. Test structure measurements show fundamental differences in the MOSFET responses to radiation. It is known that threshold voltage changes are a combination of two conflicting effects. For example, see reference [5]. Holes trapped in the gate oxide lower the threshold voltage, while interface state formation will increase the threshold. The relative magnitudes of these effects determine the overall threshold change which is measured. It is thought that the differences in the threshold shifts of Microplex 2 and 3 are due to different rates for these two processes. Furthermore, the digital operation, the analog gain and the circuit noise all showed qualitatively different dependences on the radiation dose for the two versions. The obvious conclusion to be drawn is that a given circuit can show enormous differences in radiation hardness because of the fabrication processes.

Some of the changes due to radiation can be corrected. It has been shown that damage to the shift register and the amplifier can be compensated for by adjustment of the dc level and pulse size respectively of the substrate bias. For both versions of the chip, whether unpowered or powered at 25% duty cycle during irradiation, these corrections work up to radiation doses of 100 krad. However, the increase in noise cannot be reversed. Only Microplex 2 can survive in a usable state up to at least 100 krad, if unpowered, and to ~ 16 krad if powered at 100% duty cycle. In contrast, the noise on Microplex 3 increases above a viable level after only ~ 20 krad, powered off and ~ 13 krad, powered on. For the future, therefore, we have modified the Microplex circuit to be fabricated in a process run which we hope will provide improved radiation hardness. The run will take place at the Center for Integrated Systems, Stanford University. It is hoped that this new chip will be be available for tests by early next year.

Acknowledgements

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