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# DEVELOPMENT OF A LOW NOISE PREAMPLIFIER FOR THE DETECTION AND POSITION DETERMINATION OF SINGLE ELECTRONS IN A ČERENKOV RING IMAGING DETECTOR BY CHARGE DIVISION*

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## Abstract

A preamplifier having 500 electrons noise (rms) has been developed for the detection and location of single electrons in a CRID detector at the SLD. A single channel contains preamp, RC-CR shaper, gain adjustment, driver, and calibration circuitry. Noise and linearity measurements are presented.

## 1. Introduction

This paper will describe the low noise electronics used to detect single photoelectrons in a Čerenkov Ring Imaging Detector (CRID)[1] being built for the SLD spectrometer[2] at the SLAC Linear Collider. The principle of operation of a CRID relies on optically focussing the Čerenkov light produced by relativistic charged particles passing through gaseous or liquid radiators onto a photon detector. The radius of the circle of Čerenkov light is a measure of the Čerenkov angle, which in turn is a measure of the velocity of the particle. The relationship between the velocity and the momentum of the particle permits an estimate of the particle's mass.

In our geometry,[3,4,5] the Čerenkov photons pass from the radiator through a thin quartz window into our detector, where they are converted to single photoelectrons by the photoionization of tetrakis dimethylamino ethylene (TMAE); a 0.1% component of our detector gas. Within this detector, the electrons drift at constant velocity to a proportional sense wire plane where they are detected.

For optimum performance, a CRID must reconstruct the position of the converted photon in all three dimensions. This will result in optimizing the spatial resolution of the isolated photoelectron. Many of the errors inherent to Čerenkov angle measurement have already been reduced by careful choice of geometry and detector segmentation. There are, however, sources of error such as diffusion, chromatic aberrations, and momentum smearing which contribute an irreducible total error of approximately 1 mm to this measurement. Thus, there is little to be gained by reducing other sources of error significantly below this value.

Two coordinates of the point of origin of the photoelectron are recorded as the wire address at which the electron is counted and its drift time. The proportional chamber employed as the detector for the CRID[6] has a wire spacing of 3.175 mm, corresponding to a "top hat" resolution ($\sigma$) of 0.92 mm. The maximum drift distance of our barrel CRID is 1288 mm. If the time measurement corresponding to this distance is segmented into 512 intervals, this corresponds to a 2.8 mm equivalent segmentation, essentially the same as in the wire spacing dimension when a 10% scale offset for a possible decrease in drift velocity is allowed.

The third coordinate measurement, that corresponding to the conversion depth of the photon within the drift volume, is measured by the use of charge division along the resistive anode sense wire of the proportional chamber.[7] It is this measurement which makes the most severe demands on the electronics, as here too, we require 1–2 mm resolution. Our wires, resistive carbon filaments 7 $\mu$m in diameter, are 10 cm long, resulting in a requirement of 1% spatial resolution for the measurement along the wire.

The signal to noise ratio is the crucial criterion in the design of the charge division electronics. We intend to run the gas gain of the proportional chamber so that an average photoelectron signal will produce $2 \times 10^5$ electrons. This choice is not completely arbitrary, as with more conventional chambers, in that a CRID using TMAE as its photoionizing gas must consider minimizing photon feedback in setting the gas gain. To achieve 1% spatial resolution requires a signal to noise ratio of at least 100:1, which then implies that the maximum acceptable noise level be held below 2000 electrons (rms).

## 2. The Circuit

The circuit shown in Fig. 1 has been measured to have a noise figure of 500 electrons (rms), predominantly due to our choice of the front end BF992 MOSFET, our circuit RC-CR shaping time, $\tau$, of 65 nsec, and an intrinsic capacitance of 10 pF. In our application, an amplifier will be attached at each end of the resistive anode wire, thus, an additional parallel noise source viz. the thermal or Johnson noise of the resistive wire must be added in quadrature to the amplifier noise. At a $\tau$ of 65 nsec, the 40 K$\Omega$ wire has approximately 980 electrons (rms) noise for a total noise figure of about 1100 electrons (rms).

Using the dual gate BF992, the input of our amplifier is a standard cascode configuration, wherein the voltage excursions of the first transistor drain are limited by the second transistor. The total open loop gain of the preamp is about 600.

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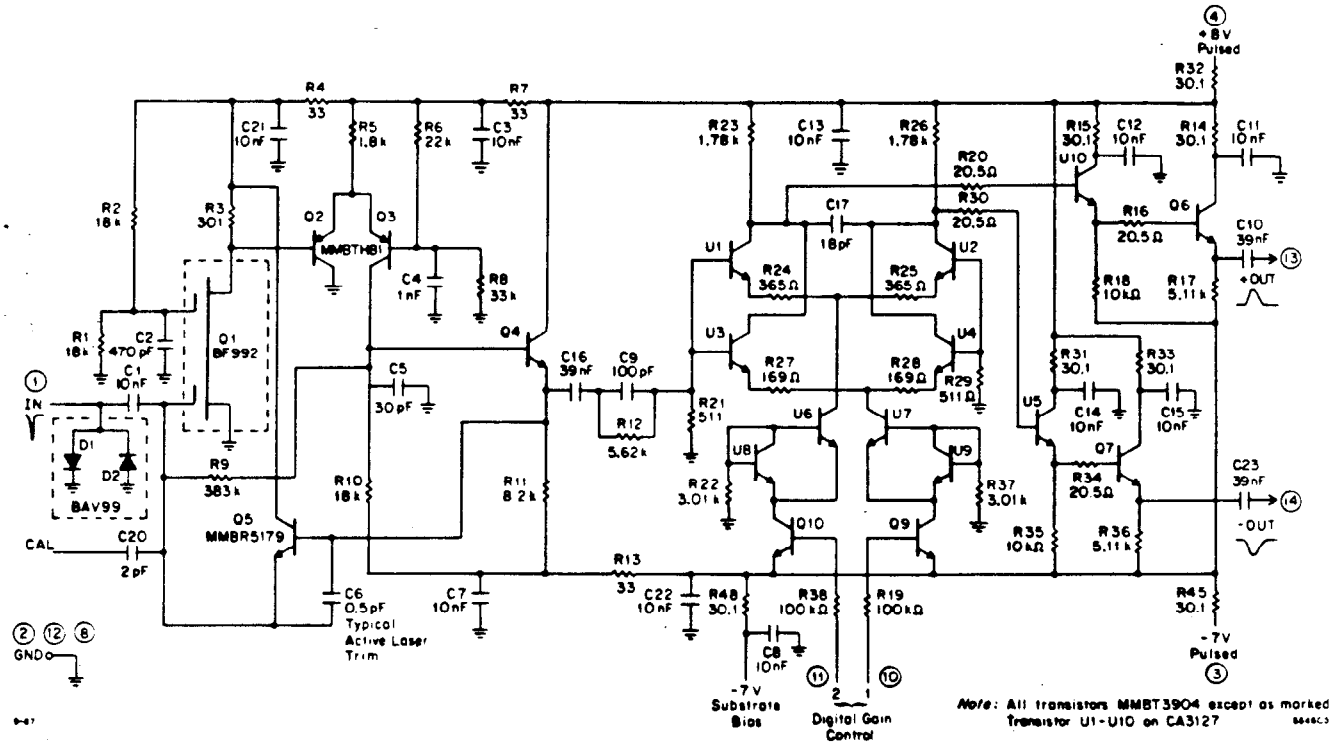


Fig. 1. Schematic diagram of the MOSFET preamplifier.

Charge to voltage conversion is effected by the parallel combination of the 0.5 pF capacitor C6 and the emitter-base capacitance of transistor Q5 which collectively act as a feedback capacitance of about 1.6 pF. In production, C6 will be laser trimmed to provide gain uniformity. Transistor Q5 is necessary to limit the voltage excursion of C6 at the detection of a minimum ionizing particle, which might have as much as 1000 times the charge of our normal single electron signal. The CRID preamplifier must have a fast recovery from such signals and to this end, the base emitter junction of this small geometry n-p-n transistor is placed between the first stage output and input. The first stage is biased so that when the output exceeds 1.4 volts in response to a large input signal, Q5 turns on and cancels the input signal. The non-linear transistor junction capacitance contribution to the feedback capacitance is minimized by being back biased by one diode drop and by the collector tie to the positive rail.

There are two shaping circuits which affect the performance of the amplifier. The first, the pole zero network (C9 & R12), cancels the exponential decay of the step function preamplifier output. This is followed by RC-CR shaping (C9 & R12‖R21; R26 & [2×C17 + Stray Capacitance]). To understand the pulse shape characteristics of our amplifier, its theoretical response to an input impulse has been compared to data taken using a number of our MOSFET prototypes. We have modelled our preamplifier's transfer function with four-time constants, corresponding to input stage integration, pole zero, RC-CR integration and RC-CR differentiation. We have also investigated the simplification of this transfer function when only the RC-CR integration and differentiation time constants are considered. The MOSFET data were then fit to both of the above response functions. The results of the fit are shown in Figs. 2(c) and 2(d). The full expression fits the data quite well, while the simplified expression is reasonable except for the pulse tail, where contributions from the long time constants, ignored in the approximation, make a significant contribution to the overall pulse shape.

Computer simulation of our circuit using SPICE[8] revealed that following the passage of a minimum ionizing particle having 32 pC of charge, or about 1000 times the normal single

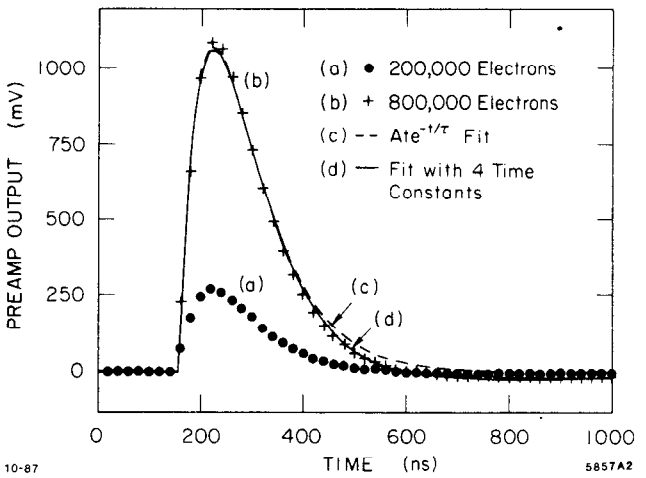


Fig. 2. (a) MOSFET preamp pulse shape for $2 \times 10^5$ electrons. (b) MOSFET preamp pulse shape for $8 \times 10^5$ electrons. (c) Fit of the data to the form $Ate^{-t/\tau}$. (d) Fit of the data to a four time constant expression.

photoelectron signal, the pulse returned to the base line in about 300 nsec, allowing the detection of a second pulse on a slowly varying base line. Figure 3 illustrates this SPICE simulation of the amplifier recovery. The signal collection time is 100 nsec. Preliminary measurements of this recovery time are in progress, and are not inconsistent with the SPICE simulation.

Input protection for the circuit is provided by the BAV99 diodes, and by Zener diodes within the BF992. Tests made in the laboratory have shown that the circuit is not destroyed by the pulse produced when 5 kV stored on a 10 nF capacitor is repeatedly shortened to ground and input to the circuit through 200 Ω.

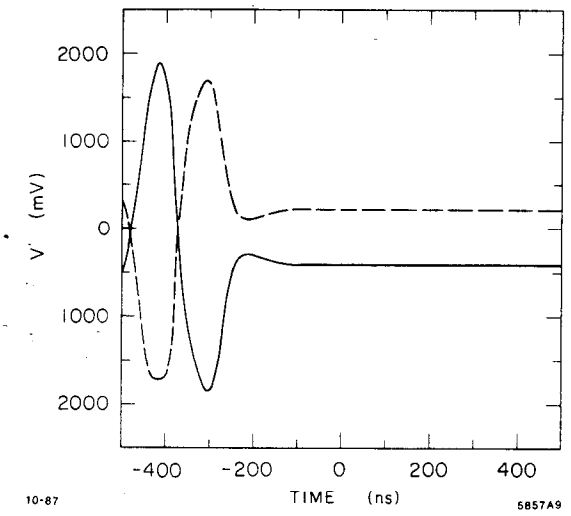


Fig. 3. SPICE simulation of the amplifier recovery for 32 pC of input charge.

The postamplifier will include a provision for gain adjustment. Gain control is achieved simply by building two possible pathways for the signal on each preamp, each having a different electronic gain. We can choose to send the signal through either path, or both, for three possible final gain choices.

The CRID preamplifiers will be subject to a very wide range of input charge: a variation of almost four orders of magnitude. To minimize neighboring channel crosstalk over this wide dynamic range, the individual amplifiers will be packaged as single channel hybrids. The PC board prototype of this circuit is shown in Fig. 4. Its dimensions are about 3.8 cm × 5 mm. This will eliminate on-board crosstalk and allow for the interposing of conductive screens to reduce radiative crosstalk. We have found that the maximum effect of a large input signal of about $10^8$ electrons on its nearest neighbor is equivalent to a signal of about $16 \times 10^5$ electrons. It can, however, be reduced by an additional factor of 15 with interposed grounded metallic screens for a total crosstalk rejection ratio of about 60 dB. The measured crosstalk is non linear; from signals less than $10^7$ electrons it is negligible.

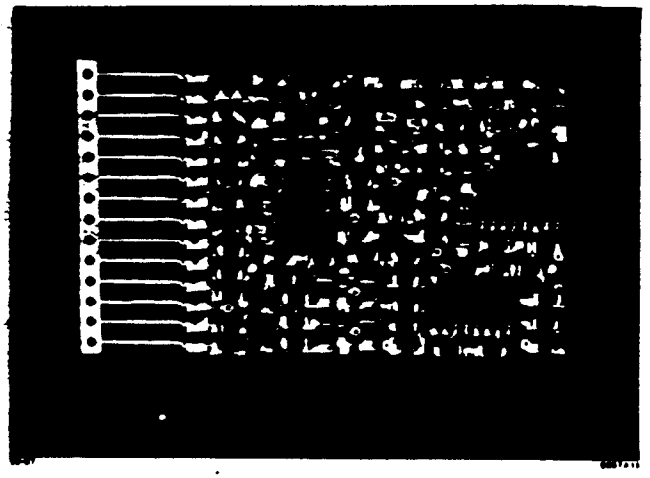

Fig. 4. Photograph of the MOSFET preamp PC board prototype.

The hybrids will use surface mount technology. Space considerations permit this technique and the cost implications are extremely favorable, as the fabrication yield will be high. The use of surface mount components, hermetically sealed and tested, also increases reliability. Under present investigation is the use of a semi-custom monolithic chip incorporating most of the circuit elements discussed above. This chip, packaged as a surface mount device would further reduce the complexity of the hybrid and increase reliability.

Circuitry for the calibration of the electronics, necessary to achieve 1% charge division resolution, is provided. A digitally pulsed voltage step created by a DAC settles in 10 nsec and is presented to the amplifier input. The circuit is shown schematically in Fig. 5 and resides on each of the preamplifier hybrids. During the fabrication process an active laser trim of R43 provides an accurate trim of the charge injected.

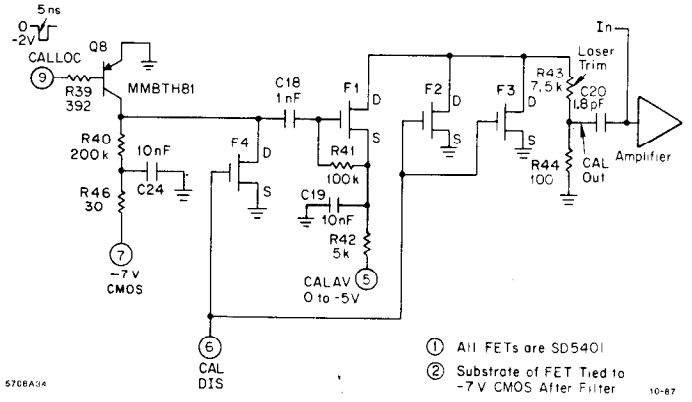


Fig. 5. The calibration circuit for the MOSFET preamp.

One channel of readout electronics is comprised of a preamplifier, shaper, gain stage, driver, and an analog memory unit. Figure 6 is a schematic representation of the readout channel in which the essential features are highlighted. The analog sampling of the waveforms relies on the use of the SLAC Microstore chip (AMU).[9,10] This chip is an array of 256 sampling cells, all of whose inputs are tied together through a series gate in each. Sixteen AMU chips are combined into an eight channel hybrid (HAMU)[11], with each channel serviced by two AMU chips. This provides a total of 512 sampling cells per channel. The multiplexed HAMU output signals, still analog voltages, are transmitted via an optical fiber link to 12 bit ADCs outside of the spectrometer iron. Provision for a DC calibration of the HAMU system is included in the system. Monte Carlo simulation studies have shown[12] that, for optimum system performance, the preamplifier shaping time should approximate the time between samples in the AMU. Thus, the maximum electron drift time divided by 512 samples determines the preamplifier shaping time $\tau$, and, therefore, the thermal noise in and the maximum pulse pair resolution of our system.

A mother board containing 186 amplifiers mates with the strip line inputs from the detector via zero insertion force sockets. Pulsed power is generated on the mother board for delivery to the hybrids. Local energy storage in the form of large capacitors is provided nearby. Surface mount components are used where available for the calibration circuitry on the mother board.

As the signal to noise ratio is of primary importance in the design of this system, the elimination of noise sources does not end with the design of the preamplifier. The mechanical design of the detector must be coordinated with the layout of the pc board mounting of the amplifiers to provide a separate, isolated clean signal ground to surround the sensitive low noise electronics.

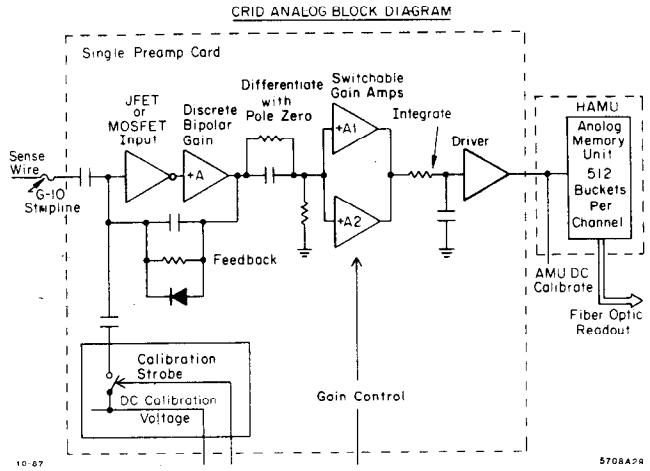


Fig. 6. A block diagram of the CRID analog readout channel.

## 3. The Measurements

Substantial progress has been made in determining the gain, linearity, noise levels, crosstalk and overdrive performance of the CRID preamplifier through a study of nine prototype preamplifiers.

Eight of the prototype amplifiers are variations of the circuit shown in Fig. 1 using the Phillips BF992 dual gate MOSFET, together with other surface-mount components in a layout suitable for hybridization. The ninth prototype utilizes a J309 JFET in the circuit configuration shown in Fig. 7. It has been used principally for noise comparison purposes, although a hybrid preamplifier using a JFET input transistor is under active consideration. Note also that the shaping time of the JFET prototype is 50 nsec.

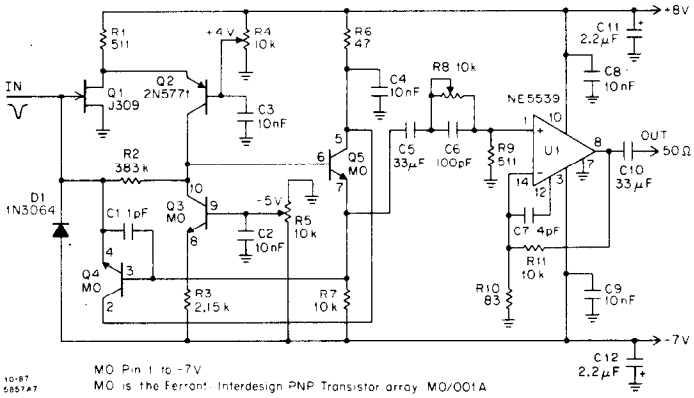


Fig. 7. Schematic diagram of the JFET preamplifier prototype.

A largely automated preamplifier test system has been constructed for measurements of amplifier charge gain and noise levels. A LeCroy 2261 Image Chamber Analyzer (ICA), operating at 50 MHz, with unity gain, 11 bit resolution and 320 time slices, provides high-speed sampling of the preamplifier output pulses, while the combination of the CAMAC packaged DAC and a charge injection circuit allow the preamplifier to be studied over the full range of input charge expected in operation.

In these tests, the outputs of the preamplifiers have been approximately matched, using a 50 Ω driver, to the 2 V dynamic range of the ICA. Since the HAMU also has a 2 V range, the total system charge-to-voltage gain is typical of that expected in CRID operation. Figures 2(a) and 2(b) show ICA digitizings of preamplifier output pulses corresponding to 200,000 and 800,000 electrons respectively. Figure 8 shows histograms of the variation of preamplifier output voltage with input charge for the three selectable gain settings of the BF992 MOSFET prototype. These characteristics were obtained automatically by applying the CAMAC DAC voltage to the charge injection capacitor in series with the input. The slope of each line gives the charge to voltage conversion gain. In the sample of eight MOSFET prototypes, the variation of gain at the same setting is less than 2%. In fact, the range of linear amplification extends considerably beyond that shown in Fig. 8, with preamplifier output saturation occurring only for charges in excess of $10^7$ electrons, even with the highest gain setting. This range is far beyond that expected in the single photoelectron pulse height spectrum.[7]

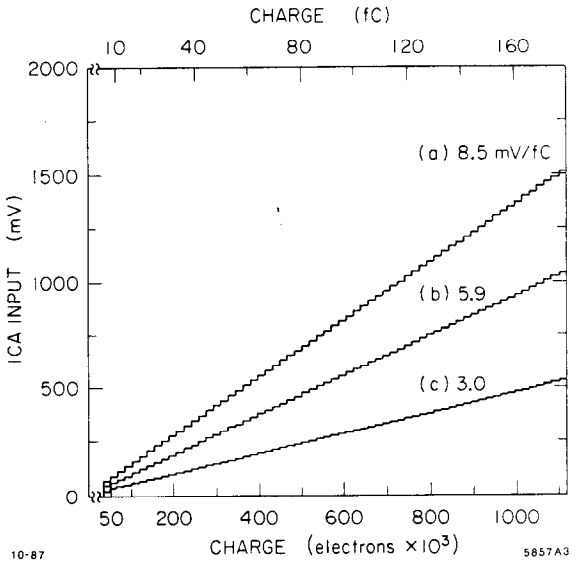


Fig. 8. Histogram of preamp output voltage vs. input charge for the three amplifier gain settings.

To measure the input noise characteristics of the MOSFET and JFET preamplifiers under various conditions of input loading, the charge injection capacitor is removed, and parallel capacitance, resistance, or CR combinations are added between the amplifier input and ground. The amplified input noise is measured with the ICA, using a software-defined "gate width". The gate width is chosen to be six times the amplifier shaping time, as measured from an independent fit to the output pulse shape using a single time constant. This interval contains about 98% of the pulse output charge. For the MOSFET and JFET prototypes, $\tau$ is measured to be 65 nsec [Fig. 2(c)] and 47 nsec, and the gate widths are set to 390 nsec and 300 nsec respectively. The equivalent noise charge (ENC) in electrons is given by

$$\langle ENC \rangle = \frac{[\sigma_V^2(AMP) - \sigma_V^2(ICA)]^{\frac{1}{2}}}{G \cdot e}$$

where $\sigma_V(AMP)$ and $\sigma_V(ICA)$ respectively are the standard deviations (mV) of the pedestal distributions seen in the ICA with and without the amplifier connected, based on comparable samples of at least 1,000 measurements; G is the charge gain of the amplifier (in mV/fC under the appropriate input loading conditions) and $e$ is the electron charge in femtocoulombs.

Figures 9 and 10 show the variation of ENC with added capacitance and/or resistance for the MOSFET and JFET

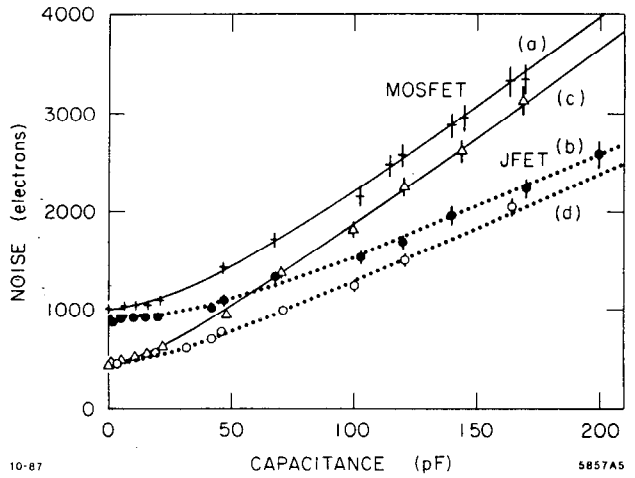


Fig. 9. Variation of $\langle ENC \rangle$ with added input capacitance for: (a) The MOSFET preamplifier with 40 KΩ resistance to ground. (b) The JFET preamplifier with 40 KΩ resistance to ground. (c) The MOSFET preamplifier with no additional resistance. (d) The JFET preamplifier with no additional resistance.

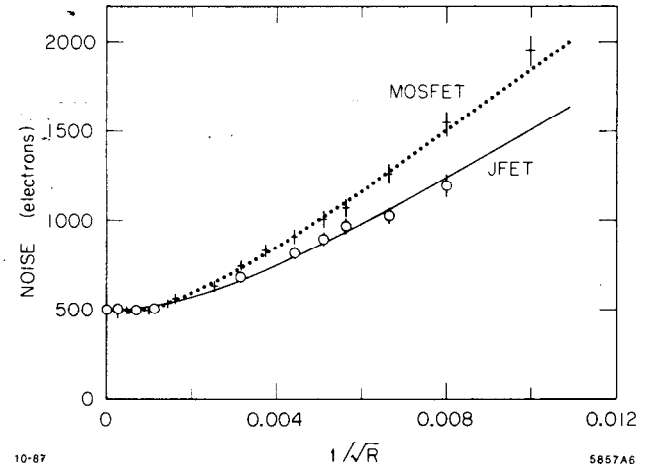


Fig. 10. Variation of $\langle ENC \rangle$ with added input resistance for: (a) The MOSFET preamp. (b) The JFET preamp.

preamplifier prototypes. Our measurements confirm that either input transistor would give acceptable noise performance for our application. Both amplifiers have about 500 electrons (rms) noise with no added resistance or capacitance and 1100 and 950 electrons (rms) respectively for 10 pF of assumed chamber capacitance, and an input resistance of 40kΩ—characteristic of a 10 cm long 7 μm diameter carbon sense wire. In Figs. 9(c) and 9(d) the noise measurement was made without the 40 kΩ input resistance. In the sample of eight MOSFET prototypes, the variation of ENC under identical load conditions between amplifiers was found to be about 10%. Approximately half of the measured ENC difference between the MOSFET and JFET preamps is a result of the slight difference in shaping times of the two prototypes. The measurements (a) and (b) of Fig. 9 have been fit to a general FET amplifier noise model[13] using the MINUIT[14] fitting program

$$\langle ENC \rangle = \frac{2.718}{e}\left(\frac{kT\tau}{2(R_{INT} \parallel R_{CH})} + \frac{eI_G\tau}{4} + \frac{kTR_{EC}(C_{INT}+C_{CH})^2}{2\tau} + \frac{A_f(C_{INT}+C_{CH})^2}{2}\right)^{\frac{1}{2}}$$

where $e$ is the electron charge ($1.602 \times 10^{-19}$ C) and $k$ is the Boltzmann constant ($1.381 \times 10^{-23}$ JK$^{-1}$). $R_{CH}$ and $C_{CH}$ represent the chamber resistance and capacitance respectively; in the amplifier tests these are simulated by added resistance and capacitance—the data points for the fit. T is the absolute temperature ($\sim 298 \pm 5K$) while $\tau$ is the measured amplifier shaping time. The free parameters in the fit are $C_{INT}$ and $R_{INT} \parallel R_{CH}$ representing the intrinsic capacitance of the amplifier and the resistance in parallel with its input (in operation the parallel sum of the amplifier intrinsic resistance and the 40 kΩ sense wire), $I_G$ and $R_{EC}$, the FET gate current and equivalent noise resistance; and $A_f$, the $1/f$ noise (Volt$^2$). For each amplifier, a good fit ($\chi^2$/DF of $\sim$ 1) was obtained with final parameter values within the ranges expected. $R_{INT} \parallel R_{CH}$ was fit to within 10% of the 40 KΩ resistance used to simulate the carbon sense wire, while the intrinsic capacitance of the amplifiers was found to be between 5 and 10 pF. The transistor parameters were also found to be within their expected ranges.[15] $R_{CH}$ for the JFET and MOSFET were found to be about 50 Ω. This was confirmed for the BF992 by an independent measurement of its transconductance (22 mS) at 1 MHz with a drain current of 6 mA. Similarly, the fit values for $A_f$ and $I_G$ were found to be in the ranges $10^{-13} - 10^{-12}$ Volt$^2$ and $2 \times 10^{-11} - 10^{-9}$ A respectively.

The final amplifier configuration under investigation is one which will eventually allow the use of a semi-custom monolithic integrated circuit array containing about 70% of the circuit elements described above. Schematically then, the amplifier hybrid will be comprised of the low noise input transistor, the calibration circuit, and the semi-custom element. To implement this idea, the preamplifier circuit using the JFET input was found to be superior to that using the MOSFET, as the dual gate of the MOSFET does not perform as well as a single transistor when designing solely with NPN transistors.

## 4. Conclusion

A preamplifier using a low noise dual gate MOSFET front end has been designed, built and tested. It performs well, having a noise level of about 500 electrons rms at a shaping time of 65 nsec. It is linear over its entire range to better than 1%. It has been used on our most recent CRID detector for the measurement of single photoelectron spectra. These results are being presented in a separate contribution to this symposium.[9] A second preamplifier using a JFET front end has been designed, built and tested and has been found to perform as well as the first.

## 5. MOSFET Preamp Specifications

| | |
|---|---|
| First Stage: | |
| 1. Input Signal (single p.e.) | = 32 fC ($2 \times 10^5 e^-$) |
| 2. Feedback Capacitor | = about 1.6 pF |
| 3. Equivalent Input Noise | = 500 $e^-$ (rms) @ 65 ns $\tau$ |
| 4. Signal Dynamic Range | = $10^3$–$10^6$ electrons |
| 5. Input Connection | = Strip Line on G10 |
| 6. Input Capacitance | = < 10 pF |
| 7. Input impedance | = 600 Ω (measured) |
| Post Amplifier/Shaper: | |
| 1. Gain (nominal @ gain = 1) | = 4.5 Differential |
| 2. Alternative Gain Settings | = x1, x2, x3 |
| 3. Pole Zero Cancellation | = $e^{-t/T_0}$; $T_0$ = 560 ns |
| 4. RC - CR Shaping | = $\tau_{Diff} = \tau_{int}$ = 65 ns |
| 5. Gain Degradation | = 1/$e$ (RC-CR) |

System Considerations:

| | |
|---|---|
| 1. Packaging | = Single in Line Hybrid |
| 2. Pins | = 14 |
| 3. Power | = +8 V −32 mA DC; −7 V −20 mA DC |
| 4. Power Duty Cycle | = 10% |
| 5. Pulse Pair Resolution | ≤ 400 ns after Min I; ≤ 200 ns after 1 $e^-$ |
| 6. Calibration Accuracy | = < 1% |
| 7. Linearity | = < 0.5% corrected |
| 8. Crosstalk | = < 2% (electronics only) |
| 9. Calibrate Modes | = Either end or both ends of wire via shift register |
| 10. Gain Sensitivity to PS Voltage | = 1/500 |
| 11. Strobe Power Recovery | = 54 dB offset from base line after 400 $\mu$s |
| 12. Environment | = 40°C |

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