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A SILICON STRIP VERTEX DETECTOR FOR THE MARK II EXPERIMENT AT THE SLAC LINEAR COLLIDER*

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Abstract

The design and status of a silicon strip vertex detector for the Mark II experiment at the SLAC Linear Collider are described.

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1. Introduction

In the near future the Mark II experiment will begin the study of the Z^0 at the SLAC Linear Collider (SLC). In order to study the decays of the Z^0 to short-lived particles, we are developing a silicon strip vertex detector (SSVD) for use in the Mark II detector. The physics motivation and preliminary design for the SSVD have been given in ref. [1]; in this paper we will describe the present design and status of this device.

We note that the SLC is a very good place for a high precision vertex detector. First and foremost, there is the potential for wonderful physics, as the Mark II experiment at the SLC is expected to provide the first detailed look at the Z^0. Second, the SLC is designed to have a small beam spot ($\sigma_{x,y} = 2\ \mu m$; $\sigma_z = 1$ mm) which should allow for a precise localization of the primary vertex. Third, there will be a small beam pipe radius (r = 2.6 cm). A vertex detector placed just outside the beam pipe will have a small lever arm for track extrapolation and multiple scattering, and thus, potentially, a small error on the impact parameter measurement. Moreover, a small radius device needs to cover only a relatively small area, which is a feature of particular importance for a silicon detector. (The SSVD will cover a total area of 500 cm^2 in three layers). Finally, the low beam crossing frequency of the SLC ($\leq$180 Hz) implies a low duty cycle and therefore low power consumption for the read-out electronics.

We further note that the SSVD is complementary to the Mark II vertex drift chamber (VDC), described in ref. [2], which is located at a larger radius. The VDC measures track angles precisely with a long lever arm, and provides good pattern recognition capabilities with many hits per track. The SSVD provides a few high precision points very close to the interaction region and very good two-track separation.

2. Design Constraints and Goals

In this section we list some of the constraints and goals that motivated our design:

(a) In order to achieve high efficiency in the detection of charm and bottom particles, the impact parameter resolution should be $\leq$20 μm for particle momenta above 1–2 GeV/c.

(b) The SSVD must fit into the available (small) space. This space consists of a well in the beam pipe with a 2.6 cm radius and a length of 28 cm. The outer radius is limited by the inner wall of the vertex drift chamber at 4.4 cm.

(c) The solid angle coverage should be $\sim$80% of 4π sr so as to correspond to the good tracking region of the central drift chamber.

(d) In order to reduce multiple scattering, gamma conversions, and particle interactions, the amount of material should be minimized.

(e) The detector and the associated read-out electronics must be able to withstand the radiation environment of the SLC. The calculated dosage is 20 rads/year for normal SLC operation [3]. However, background levels are notoriously difficult to calculate (especially for a new machine design such as the SLC), so we would like our detector system to be radiation resistant at levels at least two to three orders of magnitude higher than the calculated value.

(f) The tracking efficiency should be high and track angles should be measured for matching to tracks observed in the vertex and central drift chambers. Track-angle matching will reduce the background due to accidental hits in the SSVD. Thus at least two separated tracking layers are required.

and

(g) For high tracking efficiency in the jet-like events expected in Z^0 decays, the track separation resolution (in azimuthal projection) should be better than

5 mr. At the inner radius of the SSVD, this corresponds to a two-track spatial separation of $\leq$150 μm.

In order to satisfy the severe design constraints and goals given above, we have adopted a solution in which we will use silicon microstrip detectors read out with a custom-designed integrated circuit (the "Microplex" chip [4]). A custom read-out chip is required as the space constraints rule out the option of using conventional electronics.

There is one desirable goal—two-dimensional coordinate information—which we will not attempt to implement in this first-generation colliding beam silicon vertex detector. Only azimuthal cooordinates will be available.

3. Beam Test Results

In order to confirm that our proposed detector technology is capable of meeting the requirements on spatial resolution, two-track separation, efficiency, and separation between signal and noise that we will require in the final vertex detector, we constructed a telescope of three fixed-target-style silicon detectors. Each detector had strips of 25 μm pitch read out with two Microplex read-out chips. This telescope was tested in a 15 GeV e^+ beam at SLAC with tracks at normal incidence. These tests are described in reference [5]; here we give only a brief summary of the results:

- the efficiency of a single detector was (99.99$\pm$0.01)%;
- the background noise rate was less than 10^{-5} per strip per event;
- the ratio of the total signal to the noise in a single channel was 17:1;
- the spatial resolution was better than 5 μm; and
- the two-track separation resolution was better than 150 μm, with no deterioration in spatial resolution.

Encouraged by these results, we proceeded with the design of the SSVD.

4. The Silicon Strip Vertex Detector

4.1 General Plan

The basic layout of the SSVD is shown in Fig. 1. It consists of 3 layers of silicon detector modules with 12 modules per layer and 512 strips per module for a total of over 18,000 channels. The layer radii are 30, 34, and 38 mm, and angles relative to the beam axis down to 40° are covered.

4.2 The Silicon Detector Module

Fig. 2 shows the plan for a detector module. The silicon detector is wire-bonded to four Microplex read-out chips, two at each end. Each Microplex chip reads out 128 alternate detector strips.

For ease of installation in the mechanical support structure, as well as in the Mark II detector, and to avoid possible ground loop problems, there is only a single external cable which enters the module at one end. This cable carries the control, calibration, output, and power lines for the read-out electronics, as well as the bias voltage for the detector. A shielded thin flat cable, fabricated from 4.3 μm thick copper laminated on 25 μm kapton, brings signals from one end of the detector to the other. A particle at normal incidence will pass through 0.15% radiation lengths (r.l.) for this cable plus 0.32% r.l. for the silicon detector, for a total of 0.47% r.l. per layer.

The hybrid circuit contains a differential amplifier and line-driver for the multiplexed output signals. In addition, a bank of capacitors and a power switch supply the pulsed power at each beam-crossing for the analog section of the Microplex chips.

4.2.1 The Silicon Microstrip Detectors

A description of the three silicon detector types (one for each layer) is given in Table 1. In order to cover production angles down to 40°, active detector lengths

up to 90 mm are required. Thus to avoid the problems associated with connecting two short detectors together to form a longer detector, we proceeded with the development of detector fabrication on 4-inch diameter wafers. Previously, fabrication was only available on wafers up to 3 inches in diameter.

We have recently tested a batch of twelve prototype silicon detectors (four of each size) fabricated on 4-inch wafers [6]. The leakage current per strip I_{leak} was measured at a bias voltage about 10 V above the depletion voltage and at a temperature of 25°C.

We consider a strip to be acceptable provided that $I_{leak} \leq 200$ nA; above this value of leakage current, the shot noise contribution begins to become non-negligible, and the dynamic range of our electronics is exceeded. We find that 99.9% of the strips are acceptable. Moreover, 99% of the strips have $I_{leak} \leq 10$ nA. Hence our testing so far indicates that satisfactory detectors up to 9 cm in active length can be made.

We have also investigated the effects of radiation on detector leakage current. A single layer-3 detector was irradiated up to 220 krad in a ^{60}Co radiation well. There was no detector bias voltage applied during the irradiation. We found that the strip leakage current increased linearly at the rate of ≈ 90 nA per Mrad. Taking account of the strip volume (this is useful if the damage is a bulk effect) we can express the leakage current increase as $\approx 10^{-4}$ A per cm^3 per Mrad. These results imply that radiation exposures up to two Mrad should give acceptable strip leakage currents.

4.2.2 The Microplex Integrated Circuit

The Microplex read-out chip contains 128 channels of charge-sensitive amplifiers with multiplexed analog output. The design has evolved from the original one (version 1—described in ref. [4]) to include double-correlated sampling (version 2—see ref. [7]), as well as options for sparse-field read-out and rapid turn-on

of the amplifiers (version 3). The fabrication technology is NMOS using 5 μm design rules.

We have investigated the radiation hardness of chip versions 1 and 2. The results are presented in reference [8]. Briefly: with all power off, three out of four chips survived more than one Mrad exposure in a ^{60}Co radiation well, but the fourth chip died after 74 krad; with power on the analog section of the circuit (but not the digital section), chip failure occurred after exposures in the range of 2.5 to 32 krad on a sample of 8 chips. The radiation hardness properties of chip version 3 are now under investigation. As version 3 was fabricated at a different silicon foundry than versions 1 and 2, its resistance to radiation due to processing may be different.

4.3 Mechanical Support and Alignment

In order to capitalize on the intrinsic detector module spatial resolution of ≤ 5 μm, it is necessary to have a mechanical support structure, in conjunction with an alignment strategy, that will provide known and stable positions of each module to much better than 5 μm. We do not intend that the mechanical support structure should set the placement of the modules to very high precision; this would be very difficult and costly to achieve. Instead, the support structure should provide *moderate* placement *accuracy* ($\sim$12 μm) with *high* placement *stability* ($\sim$2 μm). The actual positions of the modules are then *measured* to high precision ($\sim$2 μm) with the alignment procedure described in section 4.3.2.

4.3.1 The Mechanical Support Structure

Fig. 3 shows a photograph of the mechanical support structure. The SSVD will be made from two hemi-cylindrical structures; these will be independently mounted on the beampipe with a three-point suspension. Each hemi-cylinder will be composed of slotted aluminum end-pieces (fabricated with electrodischarge machining), plus inner and outer beryllium shells (each approximately

0.11% r.l. thick). A detector module will be inserted into opposing slots in the two endpieces. Two compressed-spring fixtures, one glued onto each end of the module, will locate and hold the module in the slots. With this system, we expect to obtain relative positions of the modules which will be accurate in the azimuthal direction to better than 12 μm, and which will have a long-term stability better than 2 μm.

4.3.2 Alignment

The basic elements to be aligned are the 36 detector modules, not the 18,000 individual strips. The inter-alignment of the 512 strips on an individual silicon detector is provided by the photolithographic process, as developed for integrated circuit fabrication, and is accurate to better than 1 μm over the detector area. This brings an enormous simplification to the alignment procedure.

The initial step in the alignment strategy concerns the relative alignment of the 18 modules that make up one of the two hemi-cylindrical sections of the SSVD. This will be achieved by (a) optical position measurement of the modules during the assembly; (b) relative position measurements for the completed system using a high energy charged particle beam or a collimated x-ray beam; and (c) checks on the alignment, after installation in the Mark II detector, with tracks from Z^0 decays.

The next step is the alignment of the SSVD hemi-cylinders relative to the vertex and central drift chambers (VDC and CDC). This will be done with high momentum tracks from Z^0 decays and cosmic rays. In order to compensate for possible movement of the SSVD with respect to the VDC and CDC during the time necessary to accumulate enough tracks to give the desired accuracy, the relative position of the SSVD and VDC will be monitored with capacitive probes. These probes will be mounted on the outside of the SSVD and will match with ground pads placed on the inner wall of the VDC.

The final step is the measurement of the position of the interaction point (IP). This can only be done with Z^0 decays, using tracks that originate from the primary vertex. The events $Z^0 \rightarrow e^+e^-$ or $\mu^+\mu^-$ are particularly suitable for this purpose. The electron and muon tracks are (a) guaranteed to come from the IP and (b) have very high momentum (46 GeV/c) which reduces the error on track extrapolation due to multiple scattering to a negligible amount.

One further point needs to be mentioned concerning the IP position measurement. Although the IP is only 2 μm in radius, the stability of its position is unknown. The SLC feedback system that keeps the electron and positron beams in collision, only insures that the two beams have a small relative displacement; there is nothing to prevent the beams from moving together. Therefore, changes in the IP position may need to be measured with beam position monitors placed near the IP [9].

4.4 Impact Parameter Resolution

The expected impact parameter resolution σ_b for the SSVD (using the hits from the VDC and CDC as well), as a function of track momentum p, is shown in fig. 4. This is for particles at a production angle of 90°. The calculation is based on the SSVD geometry and material, and assumes an intrinsic spatial resolution of 5 μm. It also takes account of the 0.36% r.l. thickness for the beam pipe.

The curve shown in fig. 4 is specified by:

$$\sigma_b = \sqrt{5^2 + (37/p)^2}$$

with p expressed in units of GeV/c and σ_b given in μm. The "5" comes from the intrinsic resolution and the "$37/p$" is due to multiple scattering. This result satisfies the design goal for σ_b as given in point 2a.

5. Status and Summary

Fixed Target Style Detectors: a telescope of three detectors has been tested in a beam and gave clean separation between signal and noise, a spatial resolution better than 5 μm, and a two-track separation better than 150 μm. One of these silicon detectors was placed at the center of the Mark II detector and successfully took data on cosmic ray events.

The Silicon Detector Module: all the separate parts for a number of prototypes are in hand and working, including silicon detectors fabricated from 4-inch diameter wafers. A prototype module is being assembled and will soon be tested both electrically, and with 60 keV x-rays from an ^{241}Am source (60 keV corresponds to 77% of the signal from a minimum ionizing particle at normal incidence). The effects of radiation damage on the custom-designed read-out chips are being studied.

Mechanical Support and Alignment: a prototype set of slotted aluminum end-pieces has been made with electrodischarge machining. Compressed-spring fixtures for holding the silicon detector modules in the slots are being tested. A prototype capacitive probe system for monitoring the changes in relative position of the SSVD and the vertex drift chamber is being assembled.

The Silicon Strip Vertex Detector: there are many challenges ahead but we expect to have the final SSVD ready for installation in the Mark II detector at the SLC by the spring of 1988.

Acknowledgements

We warmly acknowledge the engineering and design help of Walter Nilsson (U.C. Santa Cruz), Leonardus Hubbeling (CERN), Michael Studzinski and Annegret Wagner (SLAC).

References

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[6] These prototype detectors were fabricated by Hamamatsu Photonics K.K., Hamamatsu City, Japan.

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Figure Captions

1. The layout of the Silicon Strip Vertex Detector.
2. The plan for a silicon detector module.
3. A photograph of the prototype mechanical support structure. Shown from left to right are a simplified dummy detector module, two slotted end pieces joined by an inner shell, and an outer shell.
4. The impact parameter resolution σ_b as a function of the track momentum. The tracks are produced at 90° and are measured in the SSVD as well as in the central and vertex drift chambers.

Table 1

Properties of Prototype 4-inch Silicon Detectors

Detector Property	layer 1	layer 2	layer 3	units
layer radius	30	34	38	mm
strip pitch	25	29	33	μm
number of strips	512	512	512	
active length	72	82	90	mm
total length	75	85	94	mm
active width	13	15	17	mm
total width	14	16	18	mm
thickness	300	300	300	μm
strip width	8	8	8	μm
depletion voltage	~ 50	~ 50	~ 50	V
capacitance* (to other strips)	8.2	8.8	9.3	pF
capacitance* (to backplane)	0.6	0.8	1.0	pF

* calculated.

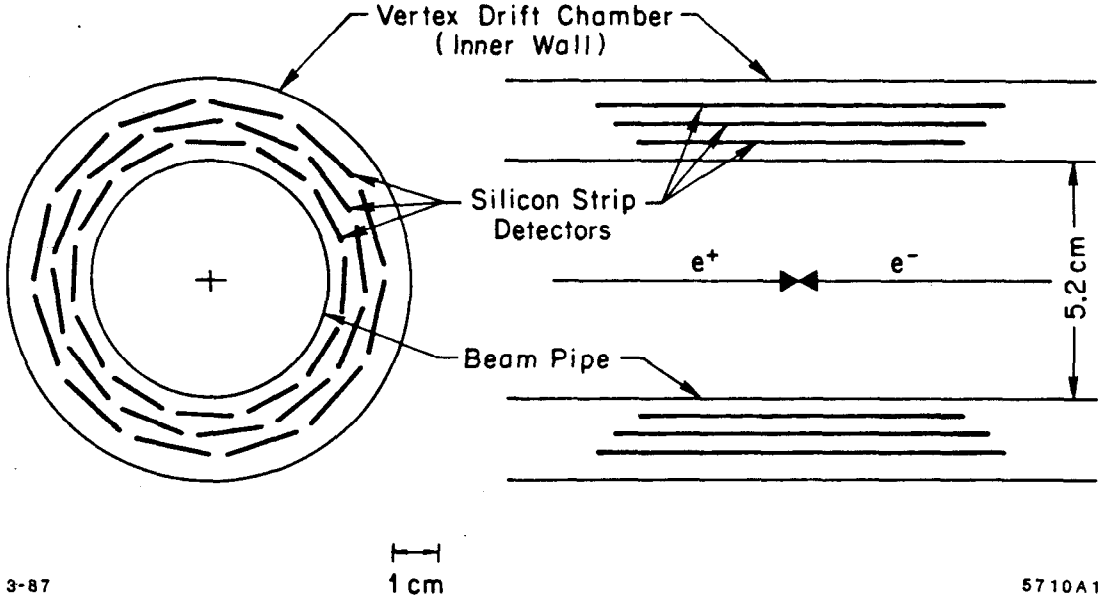
Vertex Drift Chamber
(Inner Wall)
Silicon Strip
Detectors
e+
e-
5.2 cm
Beam Pipe
1 cm
3-87
5710A1

Fig. 1

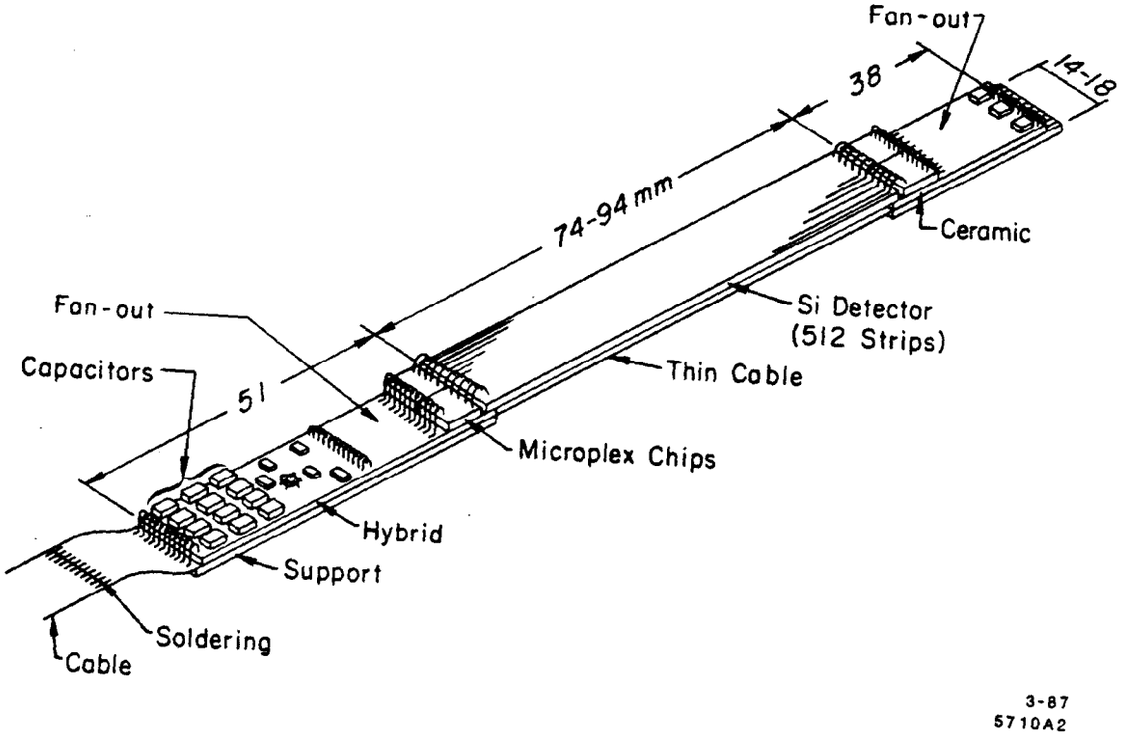
Fan-out
38
14-18
74-94 mm
Ceramic
Si Detector
(512 Strips)
Thin Cable
Fan-out
Capacitors
51
Microplex Chips
Hybrid
Support
Soldering
Cable
3-87
5710A2

Fig. 2

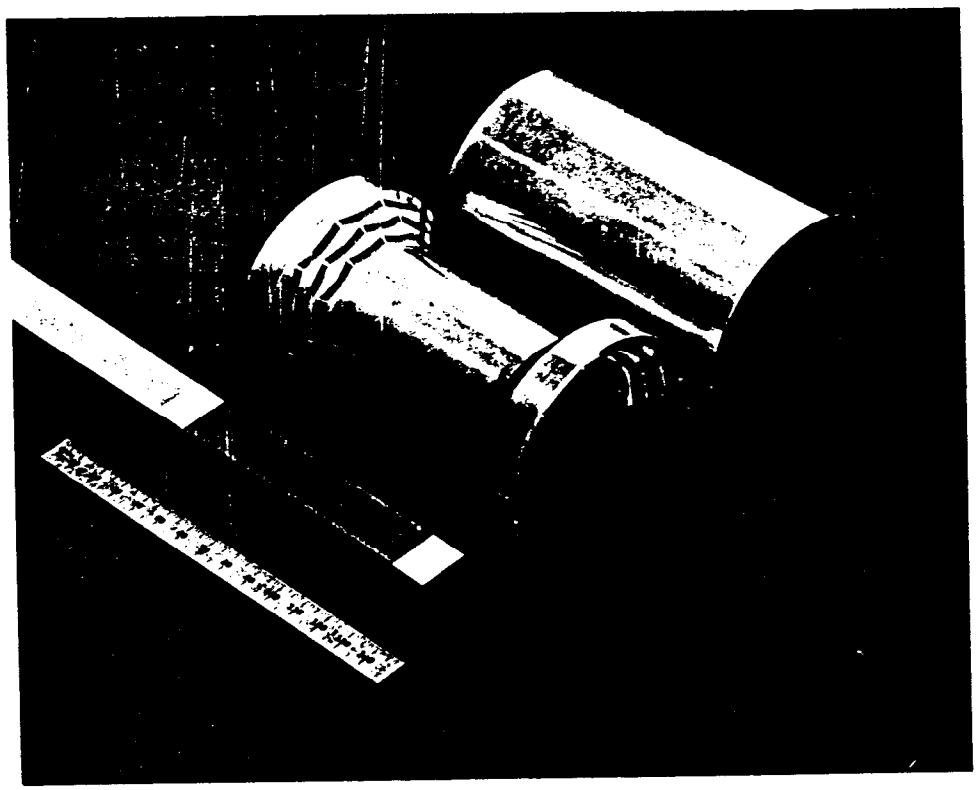

Fig. 3

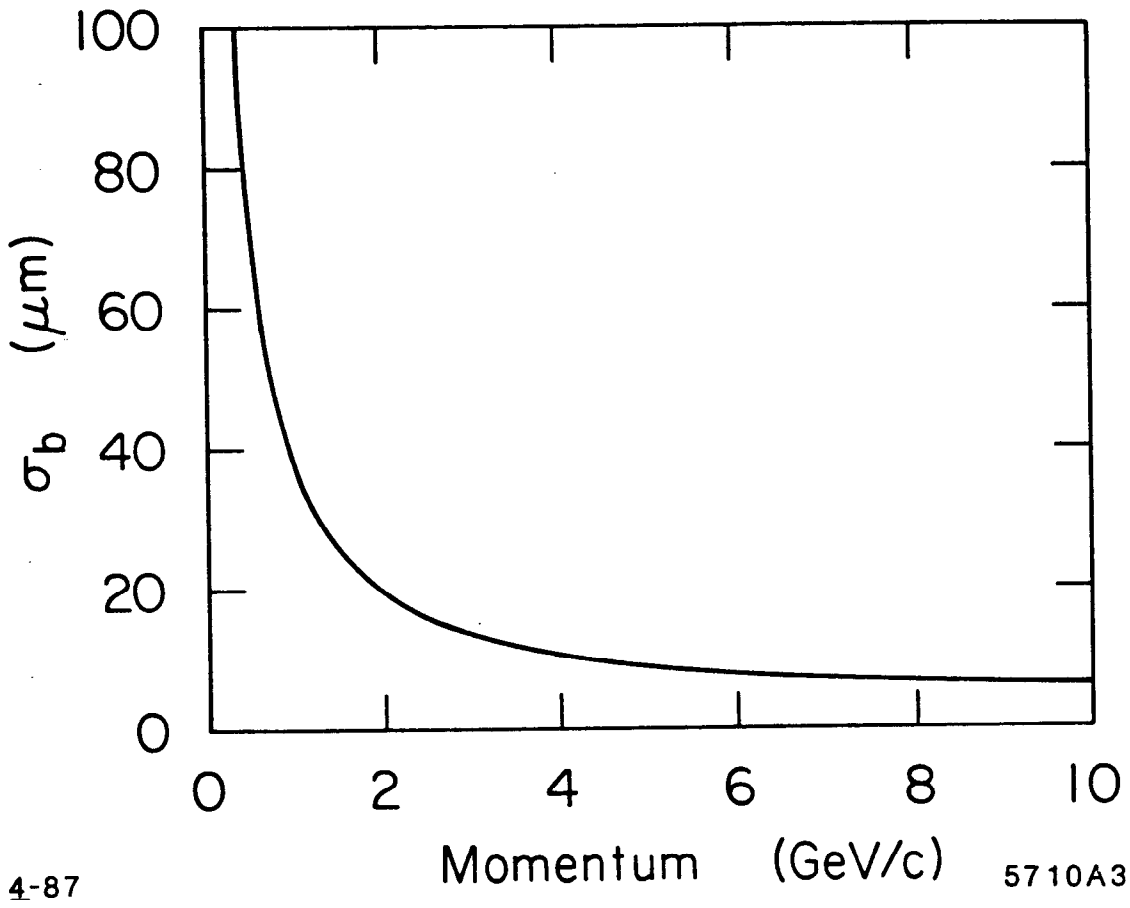

Fig. 4