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THE PERFORMANCE OF "VIRTUAL PHASE" CCDS AS DETECTORS OF MINIMUM-IONIZING PARTICLES*

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ABSTRACT

The Texas Instruments "Virtual Phase" CCD has been the basis of an ambitious design for a precision vertex detector to be used at the Stanford Linear Collider. The performance of this chip shows promise for future use in electron linear colliders. Experimental results are reported in addition to descriptions of the electronic readout and preliminary mechanical design.

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1. Introduction

The discovery that the lifetimes of the tau lepton[1-4] and heavy quark states with charm[5-15] and beauty[16-20] were of the order of 10^{-12} seconds has initiated an enormous interest in charged particle detectors with spatial resolutions smaller than $c\tau$. Silicon strip detectors have been successfully used in fixed target experiments[21-26] but suffer from the necessity of reconstructing three-dimensional trajectories from geometric projections. With increasing multiplicity at higher energies this process becomes more complex and prone to error. Several groups[27-31] have sought to overcome this limitation by employing mosaics of CCDs (Charged Coupled Devices) in place of silicon strips. CCDs provide a number of very desirable features which make them attractive for use at low duty cycle colliders such as the Stanford Linear Collider (SLC) despite their inherently long readout time.

In 1982 our group began to investigate the possibility of designing and building a CCD vertex detector to operate inside the upgraded Mark II detector[32] at the SLC. A number of constraints must be satisfied for any detector design, some imposed by general physics considerations and others by the chosen technology. These constraints place rather stringent limits on the final detector and an understanding of these problems is essential to the design process. The work described here represents a new attempt to resolve the competing demands for a light yet rigid structure using components which must be state-of-the-art and still maintain high reliability while operating in a radiation field of indeterminate intensity. After a considerable effort and achievement of most of the initial goals of the project, the development work described below was brought to a halt. The decision was based on considerations of cost, complexity, and engineering effort. In spite of this decision we hope that others interested in using CCDs for charged particle or X-ray detectors may benefit from our experience.

2. Physical Constraints

The principal purpose of a vertex detector is to identify charged particle tracks which emanate from a secondary interaction point spatially separated from the initial high energy collision. Since these separations are typically of the order of one millimeter, the inferred distances must be obtained by extrapolation of measured particle trajectories backwards to the point of origin. The best measure of whether or not a charged particle is associated with a secondary vertex is the impact parameter, b, shown in Figure 2.1. If the particle comes directly from the primary collision, b is zero; if from the secondary decay of a heavy particle with lifetime τ, b will take on a distribution of values with a maximum of the order of $c\tau$ independent of the velocity of the decaying particle. The experimental error in determining b sets the limit for distinguishing the by-products of c and b decay from the rest of the hadronic background.

The determination of the impact parameter requires at least two measurements of the trajectory to define the track slope. Due to the relatively long distance from the interaction point to the first detector the slope errors dominate the uncertainty in b. These errors arise from two sources: track measurement error and multiple scattering in the detector and materials of construction. For silicon detectors at the SLC, multiple scattering dominates. Even though the total energy in each collision is 90 GeV, the multiplicity is sufficient to keep the average particle momentum relatively low. The momentum spectrum for particles from B meson decay is shown in Figure 2.2. Since the typical momentum is only a few GeV/c the amount of material in the detector must be minimized over a substantial fraction of the trajectory. The statistically achievable limits on impact parameter resolution are shown in Figure 2.3 for a single layer CCD array in conjunction with the Mark II main drift chamber. The resolution along the direction parallel to the beam axis is a factor of two worse because the po-

lar angle is less well determined in the drift chamber than the azimuthal angle. These curves do not include any systematic errors due to alignment uncertainties that will dominate if the device is not properly calibrated.

Since the event multiplicity is high and the particle trajectories are tightly collimated in jets, the space angle between adjacent particles is small. The distribution is approximately exponential with a characteristic angle of 50 milliradians.[33] This is not much of a problem for CCDs which can resolve tracks 50 microns apart at distances of the order of centimeters from the interaction point, providing a considerable advantage over detectors with projective readout geometries.

If it were possible, the best location for a vertex detector would be inside the beam pipe, just beyond the stay-clear distance for the beam. Unfortunately the presence of large fluxes of synchrotron radiation creates a hazard which can be estimated but not fully known until the SLC achieves operational status. The expected radial distribution of synchrotron radiation photons is shown in Figure 2.4. Beyond 2 centimeters the problem appears manageable, particularly if assisted by some additional levels of masking along the beam pipe. At this distance the radiation exposure is far too low to damage silicon devices although severe missteering of the beams would lead to catastrophe.

3. CCD Selection

Starting with the premise that CCDs would be almost ideal detectors in the SLC environment, a list of requirements was formulated for the particular CCD chip to be used. The essential criteria were:

1. Relatively low cost since more than 100 devices would be required in the completed detector.
2. High signal-to-noise ratio to enable efficient track detection.
3. Thin devices to minimize multiple scattering in the detector.

4. High resistance to radiation damage.

5. Relatively few control lines to reduce the number of cables in the cramped vicinity of the installed detector.

The last two requirements provided a strong impetus to adopt the Texas Instruments type 4849 "Virtual Phase" chips[34–36] as the basis for this project. These devices are produced with an internal asymmetric potential well structure, shown in Figure 3.1, which allows track signals to be moved across the chip with only two external clock signals. The general physical layout of the chip is shown in Figure 3.2. The complex "Virtual Phase" well structure including the channel stops is created by a series of ion implants with varying concentrations. The parallel and serial clock electrodes consist of polysilicon layers insulated from the rest of the chip by silicon dioxide dielectric. This design practically eliminates the danger of shorts between overlapping gates, improving the radiation resistance of the device[37] while reducing the number of control lines for each device. The simpler electrode structure should allow the devices to be produced with higher yields and lower cost.

The development of the "Virtual Phase" CCD was originally motivated by an interest in producing an optical imager compatible with TV formats. Consequently the first chips acquired for this project exhibited depletion depths of only a few microns, sufficient for the complete absorption of visible photons. For charged particle detection the mean signal is proportional to the track length in the depleted region and deeper depletions were required for satisfactory signal-to-noise ratios. A cross-sectional view of a charged particle traversing the CCD is shown in Figure 3.3. Responding to similar interests by X-ray astronomers and others, Texas Instruments[38] produced a number of chips with greater than 12 micron depletion depth and excellent charge transfer efficiency. A minimum ionizing particle traversing any given pixel of these devices generates a quantity of charge randomly distributed according to a Landau function with a mean of 1000 electrons. In order for the Texas Instruments "Virtual Phase" CCD to per-

form well as a particle detector, the total noise per pixel must be limited to less than 50 electrons. Results obtained with these deeply depleted devices form the core of this report.

The CCD active area is segmented into 584 rows by 390 columns for a total of 227,760 pixels, each 22.4 μm square. The serial register at one edge of the chip accepts charge from each of the 390 columns and separately transports each charge bucket to a floating diffusion amplifier. Eighty-six percent of the total die area is sensitive to charged particles. The chip is fabricated on epitaxial wafers about 500 μm thick which could be thinned to reduce multiple scattering.

One consequence of the "Virtual Phase" technology is the large capacitance of the parallel clock structure that must cover the entire active area. At 7000 picofarads and clock voltage ramp rates of 100 volts per microsecond, instantaneous currents approach one ampere. Fortunately the low duty cycle of this waveform suppresses potential problems with thermal dissipation.

4. Electronics

4.1 Requirements of the System

A CCD based particle detector imposes the following stringent requirements on the electronics necessary for its operation:

1. The clocking waveforms must efficiently transfer the localized charge produced by a track across hundreds of pixels to the on-chip amplifier. Due to the small size of the signal, (~1000 electrons), losses from the charge packet must be minimized.

2. Total noise contributions per pixel must be held below 50 electrons to maintain a high signal-to-noise ratio.

3. The pixels must be transferred through the on-chip amplifier with the highest possible clocking frequency to avoid excessive dead-times. This implies a clocking frequency of at least 2 MHz at the SLC.

4. Due to the large number of CCDs in the proposed system, (~100), the various modules of the readout and control system must be easily replicated and computer controlled.

At the outset of our research, Texas Instruments strongly urged the use of tri-level clocking waveforms to reduce readout noise. Except for this suggestion the optimal waveforms were not known, so independent and interactive control of the timing and amplitude was necessary to optimize the parameters for each CCD in the detector system. The clocking waveforms required for efficient small signal transfer are shown in Figure 4.1. To further minimize readout noise, flexible control of the output signal sampling and integration times was also required. The output signal is shown in Figure 4.2 with the integration and sampling times indicated.

Since even a minimal CCD vertex detector must contain on the order of 100 devices, the electronics must be replicated on a large scale. Moreover, in order to optimize, monitor, and control such a large system, computer control of the readout and acquisition modules was essential. The large number of CCDs confined to a small volume at the center of a 4π detector and the enormous power ratio between the clocking and signal waveforms mandated that the entire system operate synchronously to avoid crosstalk.

4.2 Overview of the Electronics

To read out the CCD, one must supply three clocks to the device: a parallel row transfer, a serial register transfer, and a reset clock. The temporal ordering of the clocks evolves as follows: One parallel transfer cycle advances each row one step vertically with the uppermost row dropping into the serial register. A subsequent train of serial register transfer cycles clocks these pixels one-by-one

to the single on-chip amplifier which is reset with the reset clock after each pixel is transferred through it. Once the entire row has been clocked, another parallel row transfer cycle shifts the next row into the serial register and this pattern repeats until every pixel of the CCD is clocked out. For maximum flexibility, the readout system was designed to permit quite complex waveforms which could be interactively modified.

Waveform timing was controlled by a **phase control module** and waveform voltage level was controlled by a **function generator module**. The function generator consisted of a DAC driven by a RAM memory whose address was furnished by the phase control module. Each CCD readout waveform required one phase control module and one channel of a function generator module. The modular nature of the system could easily be adapted to other CCD systems with different clocking requirements. It was soon realized that variations in clocking waveforms from one CCD to another were limited to the voltage levels and not the timing. Hence, a small number of phase control modules would provide the timing base for the entire detector system, although each CCD would require two separate function generator channels to accommodate voltage level differences between devices for the parallel and serial clocks. A single reset clock could be shared by a number of chips.

The output signal of the CCD was pre-amplified before input to the analog-to-digital converter module (ADC). This module amplified and digitized the signal using an eight-bit flash encoder. Control of the sampling and integration times was performed by a phase control module. The 8-bit digitized output was stored in a frame memory module pixel by pixel. Once the entire CCD had been clocked, the data in the frame memory module was processed and results graphically displayed. The functional relationship between the various modules and control computers is shown in Figure 4.3. A more detailed description of each logic module is given below.

4.3 Readout Clocks

4.3 a. Phase Control Module

The heart of each phase control module consisted of two separate 64 K bit strings stored in fast (100 ns, 8K×8 RAM) memories. These strings defined the two timing channels for each controller, one of which was used for the normal readout sequence and the other used for fast clear of the CCD. Each bit in the string marked a voltage transition by incrementing an address counter used to drive the function generator lookup table. The address counter was reset by the detection of two contiguous logic "1" bits in the bit string. The phase control module also generated TTL outputs of each bit string for more complex control of the readout logic.

Both 64 K bit string memories were written and read via CAMAC allowing interactive control of the waveform transition times. The address counter of each channel could also be reset externally or via CAMAC. The phase control module was driven with a 10 MHz base clock, limiting the minimum pulse width to 100 ns. This limitation was well matched to the minimum rise and fall times of the function generator under load. For faster readout rates, look-ahead logic for the bit string memory permitted operation at higher base clock frequencies. Figure 4.4 shows a functional diagram of the phase control module.

4.3 b. Function Generator Module

As previously mentioned, the function generator module served as a lookup table for an address supplied by a phase control module. The function generator had four identical lookup memories (100 ns 8K×8 RAM), which defined the four channels of the module. The CCD output signal was sensitive only to changes in the clocking levels of greater than 0.3 volt. This level of sensitivity coupled with the 24 volt range required by the clocking gates, dictated the necessity for an eight-bit resolution in the clocking levels. In each channel, the byte representing the voltage level controlled a fast 8-bit digital-to-analog converter (DAC)

connected to a fast amplifier. To overcome the large capacitance of the CCD clocking gates the clocking waveforms were further amplified by a unity gain fast current driver. The resultant rise and fall times of the loaded output waveform of each channel were 50-100 V/μsec.

The large capacitance of the parallel transfer gate required additional current drive very near the CCD itself. The compact size of the CCD detector and the restricted access within the rest of the Mark II detector demanded that these current amplifiers be as small as possible. Such a circuit was fabricated using surface-mount components and found to work adequately. However most of the results presented here were obtained without this circuit by driving four 75 ohm cables in parallel directly from the function generator output. The analog output of each function generator channel ranged from -24 volts to +12 volts with gain and offset levels set by two potentiometers per channel. The function generator memories were written and read via CAMAC to allow interactive control of waveform voltage levels. A functional diagram of this module is shown in Figure 4.5.

4.4 Acquisition Electronics.

4.4 a. Preamp, ADC Module and Phase Encoder Module.

The on-chip amplifier response was about 1 μV per electron, implying typical output signals of 1 millivolt for minimum ionizing particles. The output signal was AC coupled through 50 cm of RG174/U cable to a low noise pre-amp which provided a gain of five. In turn the pre-amp was connected by approximately one meter of RG174/U cable to the **ADC module**. In this module the signal was further amplified by an additional factor of ten before processing in a correlated double sampling circuit. The double sampling[39,40] significantly reduced the fluctuation noise associated with the periodic reset of the CCD on-chip amplifier input node. The correlated signal was subjected to a final stage of amplification before digitization by an 8-bit flash encoder. The total system gain from the CCD output to the flash encoder was $\sim$ 1000.

Two designs for the ADC module were studied with different implementations of the correlated double sampling circuitry. Our first design used analog switches to sample and integrate the signal before and after reset as shown functionally in Figure 4.6. This method produced an electronics noise equivalent of $\sim$ 30 electrons although it was plagued by slow switching transients which limited operation to a readout rate of less than 300 KHz. The second design utilized an analog delay line to simultaneously provide to the inputs of a differential amplifier the signal before and after the reset pulse. This circuit is shown schematically in Figure 4.7. The delay line method operated at 450 KHz with an electronics noise equivalent of $\sim$ 50 electrons.

The ADC sampling and convert time and the width and relative positions of the correlated double sampling windows were controlled by an additional phase control module. A special module called a **phase encoder** was designed to receive the TTL bit string output of this phase controller as a timing input. On the occurrence of a transition in the timing string, the phase encoder incremented an internal address counter which selected the contents of a fast bipolar memory. The 16 bit control word at each address furnished the timing sequence for the ADC module. The phase encoder could be cleared either externally or via CAMAC. A functional diagram of this module is shown in Figure 4.8.

The ADC module was equipped with a programmable mask register to eliminate digitization of pixels from defective columns. The devices studied in this report typically had 1-2 of these "hot" columns. The output of the flash ADC was connected to the input of the frame memory module where it was stored pixel-by-pixel.

4.4 b. Event Buffering: CCD Frame Memory Module.

Event buffering was performed by two **frame memory modules**. Each module was constructed with 256 Kbytes of RAM, hence each memory module could contain the entire 228 Kbytes of a single CCD frame. Two memory modules were used to facilitate pixel-by-pixel signal-background subtractions and could

be read or written via 16-bit CAMAC transfers. Figure 4.9 shows a functional diagram of this module.

4.4 c. System Synchronization: Clock Gate Module.

In order to provide a synchronized clock pulse train to all modules, a **clock gate** was constructed that could be enabled or disabled from the front panel or via CAMAC. Each clock gate had master and slave circuits so that two modules could be used to construct a synchronized iteration loop structure with phase control modules to determine the loop count. A functional diagram of the clock gate module is shown in Figure 4.10.

4.4 d. Performance Monitoring: VHR DMA Module

Online monitoring of the CCD performance was critical for determining the optimal device operating parameters and understanding subtle performance characteristics. Pulse height histograms, row pulse height profiles and two-dimensional color-encoded pulse height maps were generated by the in-crate LSI-11 and displayed on an Intecolor VHR-19 high resolution color display terminal. By using local processing, these displays were created quickly, circumventing the I/O bottleneck to the host VAX. Almost all of the display computation required only integer arithmetic so the LSI-11 was comparable to the VAX in processing speed. Histograms were plotted on the VHR-19 terminal with the aid of the terminal's graphics command strings. Since the color-encoded maps required transfers of almost one quarter of a million pixels of information to the display screen, a CAMAC **VHR DMA module** was constructed to transfer data directly to the three VHR-19 color bit planes via a separate DMA channel. A complete map was generated in about 15 seconds from data stored in the frame memory modules.

5. Processor Control: Data Acquisition Software

Interactive control of the electronics was performed by a Digital Equipment Corporation VAX 11/750 computer. The enormous amount of data in each CCD frame (228 Kbytes) also required local computing capacity for analyzing full CCD frames autonomously. To achieve this, a CAMAC auxiliary controller module with an internal LSI-11 processor board was employed in the system. Most of the readout control and online analysis was performed with this in-crate processor. This allowed prompt analysis of performance resulting in fast optimization of operating parameters. Communication with the host VAX was restricted to the setting and reading of flags, initializing modules and the interactive control of the readout module's memories, all via CAMAC.

The requirements of the software associated with the CCD particle detector were two-fold: 1) monitoring and control of the operating parameters, and 2) acquisition and analysis of the output data. As mentioned before, at the onset of our research the optimal operating parameters of the CCDs supplied by Texas Instruments were not known and it was thought that differences in the optimal parameters from device to device were inevitable. Hence control software was developed to quickly and flexibly modify operating parameters such as the voltage levels and timing of the clocking waveforms. A version of the SLC Control Program[41] (SCP) was adopted for system control purposes to run on the host VAX. The SCP was a screen-driven menu selection program that permitted very general display and control of the operating parameters of the detector system. Effectively, every parameter of the system was controlled by one or more virtual touch panel switches whose images were displayed on a terminal display screen. Switch selection was performed with the terminal cursor control keys. For waveform control even the definition of the these software switches was interactively modified to match the specified number of voltage transitions. The SCP process directed the operation of the in-crate LSI-11 computer by passing messages to a CAMAC mailbox memory module and thus selected the displays generated on

the VHR-19 graphics terminal.

Acquisition and analysis software resided both on the host VAX and the in-crate LSI-11. The acquisition software on the VAX, operating as a background process, served as the interface between the user's SCP process and the acquisition electronics of the detector system. The large amount of data in one CCD frame necessitated minimizing the data transfers from the frame memory modules to the host VAX. This was accomplished by using the in-crate LSI-11 for extensive statistical analysis covering every single CCD pixel. Software on the LSI-11 generated pulse-height histograms to monitor the effect of changing operating parameters on the signal and noise peaks. The LSI-11 also generated false color pulse-height maps of the CCD so that the two–dimensional variations in response could be studied. These maps were also valuable for understanding the CCD performance as a cosmic ray track detector.

6. Mechanical Support

All CCD tests were performed with the chip mounted horizontally in a specially built cold box. The box consisted of a massive aluminum block with cavities on the top, bottom, and one side to allow testing with cosmic rays, radioactive sources, and optical patterns. Thermal insulation was provided by styrofoam on all six sides. This assembly was mounted on a vertical test stand which rigidly supported the scintillation counters and drift chambers required for the cosmic ray measurements. Inside the cold box, the chip was held in a zero insertion force socket fastened to a small printed circuit board. Control signals were introduced via 75 ohm multiconductor cable. The output signal was extracted on RG-174/U coaxial cable to a preamplifier about 50 cm distant.

The chip housing was cooled by a continuous stream of nitrogen gas from a 20-liter liquid nitrogen dewar with an electric heater at the bottom. The temperature was stabilized to an accuracy of $\pm 0.2^{\circ}$C by a feedback loop consisting

of a resistance thermometer, a proportional power controller, and an electric heater surrounding the gas inlet manifold. With this apparatus, the temperature could be controlled over the range -60° to +10°. At -20°C one filling of the dewar lasted about 24 hours.

7. Operating Procedures

Three distinct readout modes were adopted for the CCD system. The first was a fast test mode which reinitiated the readout cycle of the CCD after each complete scan. This mode was useful for debugging the system electronics. In this mode, no analysis of the data in the frame memory modules was attempted.

The second mode provided a fixed time exposure useful for tests involving X-ray and beta-ray sources. In this mode, the CCD was first cleared by the LSI-11 with a fast clear cycle and then exposed to the source for a time established by a delay gate generator. The fast clear cycle was a modified readout sequence in which many parallel row transfers occurred before each normal train of serial register transfers. This pattern was repeated until the whole CCD was completely swept of any previously generated charge. This clocking sequence was considerably faster than the normal readout since many fewer trains of serial register transfers were required. After integrating for a period of time determined by the delay gate generator, the LSI-11 initiated the normal readout cycle. When the entire CCD had been read and stored, the LSI-11 proceeded with an on-line analysis determined via user interaction with the host VAX. In this mode the user could select pulse height histograms, row profiles, the CCD pulse height map, or a subtracted frame analysis. If the latter option was specified, the LSI-11 independently loaded the two frame memories with sequential readout cycles. Subtracting one frame from another, pixel by pixel, permitted sensitive measurements of several different noise sources. For example, for determination of the X-ray energy resolution, the two frames were recorded with a radioactive source

shielded and unshielded by a mechanical shutter. Transfer of entire frames to the host VAX could also be requested by the user in this mode.

The third mode was a triggered sequence for cosmic ray tests. In this mode, the LSI-11 alternated between fast clear and integrate cycles until a trigger was received during the one second integration period. The trigger was a 4-fold coincidence of four scintillator counters which, in conjunction with the CCD and two proportional wire drift chambers, comprised a cosmic ray telescope. Upon receipt of a trigger, the LSI-11 began normal readout of the CCD and informed the host VAX of the occurrence. Following notification, the host VAX read, via CAMAC, the CCD frame memories and the drift chamber TDCs. The host VAX computed and returned the expected cosmic ray coordinates to the LSI-11 which then generated a display of the region of the CCD in the neighborhood of the computed track.

8. Results

Our study of the Texas Instruments type 4849 CCD was undertaken to determine its ability to perform as a vertex detector at the SLC so the following operating characteristics needed to be assessed:

1. The small signal performance characteristics of the CCD.
2. The maximum temperature at which the CCDs could operate and still have reasonable noise levels.
3. The readout speed that could be achieved with reasonable signal resolution and low noise levels.
4. The efficiency of the CCD performing as a charged particle detector.
5. The effect of high doses of radiation on the CCD.

The second and third points are related since the noise generated by dark current increases with temperature and decreases as $f^{-1/2}$ where f is the readout

frequency. Hence increasing the readout frequency will allow operation of the CCD at a higher temperature. The readout speed is ultimately limited by the maximum speed with which charge can be efficiently transferred from pixel to pixel which is on the order of 10 MHz. In the following sections we report the results obtained in our study of the Texas Instruments 4849 CCD and attempt to draw some conclusions relating to the five points enumerated above.

8.1 X-RAY SOURCE STUDIES

An ^{55}Fe X-ray source was initially used to study small signal response since a 5.9 KeV Mn K_α photon has a fair probability of being absorbed in the 12 μm depletion layer of the CCD. The primary electron produced in the photoionization process travels less than 1 μm in silicon, so the total signal is shared by no more than two pixels. In addition, the total signal charge is $\sim$ 1600 electrons which is about a factor of two greater than the signal expected from a minimum ionizing particle. Thus, the performance of the device as a particle detector may be estimated from its response to this monoenergetic signal.

A typical radiation source run was begun by reading out the CCD several times before source exposure and storing the average background signal for each pixel. The CCD was then exposed to the ^{55}Fe source for up to 1 second before the data was read out and transferred to the VAX where background subtraction was performed pixel-by-pixel. A number of such exposures could be made and the results summed to accumulate statistics. Figure 8.1 displays a typical histogram for a 30 frame run using a 20 μCi source at a device temperature of $-30°$C. The Mn K_α and K_β lines at 5.9 KeV and 6.4 KeV are easily resolved. The signals below the peak and above the noise background (the noise background below an ADC count of 20 has been suppressed) are due to charge sharing between pixels or to charge loss.

Charge sharing occurs when the electron cloud diffuses far enough to overlap the potential wells of two or more pixels. Loss of signal occurs when some electrons are not collected in the depletion layer of the CCD. This may result from

charge migration to the substrate or to a channel stop if the event is generated in or near it. These are referred to as partial events.

In order to calibrate the response of the system and to measure its energy resolution a sample of events was obtained in which the entire signal charge was isolated within a single pixel. To acquire this sample the standard deviation of the background variation over the entire chip was calculated and then only signals from those pixels which did not have any neighboring pixel with a signal greater than five times this standard deviation were saved. This algorithm effectively removed signals degraded by charge sharing. However, it would bias against events smeared by poor charge transfer efficiency. Since this efficiency was found to be very high by an independent method, it did not affect the energy resolution of the device. Signals for which charge was lost for some other reason remained in this sample. Figure 8.2 is a histogram of this data sample with Gaussian fits to the K_α and K_β peaks. The fit was performed from channel 104 to channel 128 and is skewed slightly low by the population of partial events. The K_α peak centered at channel 109 was employed to calibrate the response of the system in terms of electrons per channel. Since the mean excitation energy required for the production of an electron-hole pair in silicon[42] is about 3.8 eV, we expect each 5.9 KeV photon which interacts in the depleted layer to produce 1550 ± 40 electrons. This yields a system calibration of 14.2 ± 0.5 electrons per ADC channel. The K_β peak centered at channel 120 is also consistent with this value.

Since the silicon K_α line is at 1.7 KeV, we might expect to see a silicon escape peak in channel 78 corresponding to an energy deposition of 4.2 KeV. Figure 8.3 shows the histogram with the K_α peak truncated to enhance the structure of the noise floor. The silicon escape peak is clearly visible centered near the predicted bin. The root-mean-square width of the X-ray peaks correspond to a resolution of 43 electrons. The resolution expected from the $\sqrt{N}$ variation in the signal is 39 electrons, indicating that the noise contribution from the readout electronics is negligible. This was confirmed by measuring the width of the pulse height

spectrum obtained when the CCD was not exposed to a radioactive source.

We also examined the response of the CCD using a ^{57}Co source. It was necessary to reduce the gain by about 30% to keep the 14.4 KeV signal from exceeding the dynamic range of the ADC. Figure 8.4 shows this spectrum. The K_α and K_β lines at 6.4 KeV and 7.1 KeV are seen near channels 84 and 92 respectively and the 14.4 KeV nuclear transition is seen near channel 196. This data showed that the linearity of the system was excellent over the entire dynamic range.

8.2 Delay Line ADC Results

All results in this paper were obtained with an ADC module using the switched integration method for correlated double sampling at 200 KHz, unless stated otherwise. This rate is a factor of ten lower than required for an acceptable detector dead time at the SLC. In an effort to increase the readout rate of the CCD we built an ADC employing the previously described delay line technique. A 1 μsec delay line allowed operation of this ADC module at 450 KHz using a three level serial clock on the CCD. An ^{55}Fe spectrum obtained at this speed is shown in Figure 8.5. The delay line ADC ^{55}Fe K_α calibration was 15.0$\pm$0.6 electrons per ADC channel, with a root-mean-square noise of 51 electrons as compared to 43 electrons for the switch-based module. This implies an electronics noise contribution of 32 electrons, which would be adequate for a particle detector. Due to the low baseline variation of the output it was not necessary to reset the on-chip amplifier after each pixel, as will be evident from the discussion of background in the next section. Since the readout time is dominated by the *sum* of the pre-reset and post-reset integration times, removing the pre-reset integration time can double the readout rate[31] . Further increases in speed might be obtained with a shorter delay line with faster rise times, as well as a faster serial clocking waveform which could be realized with a two level clock. The effect of a two level serial clock and a shorter delay line ADC on small signals may be studied in the future.

8.3 Background Signal Studies

Even when there is no external signal source applied to the chip, a signal is produced at the output of the CCD. This background signal has two components: thermally generated dark current and "spurious charge". The number of thermally generated electrons in each pixel produces a background signal distributed according to Poisson statistics. Since statistical fluctuations are a source of noise over which the real signal must be discriminated, this background must be reduced as much as possible. The component of the background signal called "spurious charge"[43] is produced by impact ionization when holes near the Si-SiO_2 interface are suddenly accelerated by the large potentials present in transferring charge from one pixel to the next. Spurious charge does not increase with readout time and can be reduced to nearly zero by careful selection of the intermediate level in the clocking waveforms. This was the major reason for requiring complex tri-level waveforms from the drive electronics.

The dark current is produced by electrons thermally excited into the conduction band of the silicon and trapped in the potential wells of the CCD. This source of noise rises with the operating temperature. The serial architecture of the CCD readout requires that the charge from the nth horizontal row remain stored on the chip until the previous n-1 rows have been clocked through the on-chip amplifier. At a pixel readout frequency of 200 KHz, each complete serial register transfer cycle requires 2.5 msec so the charge associated with the nth row is augmented by the average dark current integrated over a time of (2.5 msec)$\times$n. For $n > 10$ we may make the assumption that the contribution to a charge packet from dark current while it is in the serial register is negligible relative to the contribution from dark current while it is on the array. The following relation then holds:

$$j_{Dark} = g\frac{\partial < s >}{\partial t}$$

where j_{Dark} is the dark current, $< s >$ is the output signal averaged over one row and g is the previously determined number of electrons per channel. The dark

current is expected to have the following dependence on temperature, T:

$$j_{Dark} = j_0 e^{-\frac{E_b}{kT}}$$

where E_b is the effective band gap. A plot of the dark current versus inverse temperature is shown in Figure 8.6. This plot indicates a dark current of approximately 500 electrons per pixel per second at 20°C.

It is desirable to run a CCD detector as close to room temperature as possible to reduce the complications of cooling the detector and to reduce the amount of thermal insulating material between the interaction point and the outer detectors. The response of the CCD maintained at 0°C to ^{55}Fe X-rays is shown is Figure 8.7. This response deteriorated rapidly with rising temperature however. Although a dark current of 500 electrons per pixel per second would contribute a tolerable level of noise at 20°C, other noise sources began to appear with rising temperature. For example, Figure 8.8 shows the signal across a typical single row of the CCD at a temperature of -30°C and +5°C. Several time varying dark current spikes, which are probably due to impurities or imperfections in the epitaxial layer of the CCD, were observed at temperatures above 0°C. These have the potential for faking real signals when a CCD is used as a particle detector. The effects became more severe the warmer the CCD was operated and it was impossible to obtain reasonable results above +10°C for this particular device.

8.4 Ruthenium Source Studies

To understand how the CCD would respond to charged particles, we exposed the chip to a 1 μCi ruthenium source. The end-point energy of this beta source is 3.54 MeV, so the more energetic electrons should produce an energy loss approximately the same as caused by a minimum ionizing particle. The single hit pixel pulse height distribution from a typical ^{106}Ru exposure is shown in Figure 8.9. The fit curve is a theoretical calculation of the expected Landau distribution[44] modified to include the atomic binding effects of the electrons in the silicon[45]

convoluted with the beta energy spectrum. As can be seen, the curve fits the data fairly well. Some discrepancy between theory and measurement is expected since the depletion layer may not be uniform across the CCD and split events are expected to increase the larger the energy loss in the silicon, pushing the peak of the data downward slightly. Since the peak of the modified Landau distribution varies approximately linearly with the active silicon thickness, it is possible to estimate the effective depletion depth of the CCD by finding the best fit to the data with all other parameters fixed. In fact this method is probably the most accurate way of determining the depletion depth of "Virtual Phase" CCDs. For the devices studied with an epitaxial layer of 15 μm, the average depth was approximately 13.5 μm.

8.5 Cosmic Ray Results

To study the feasibility of the CCD as a detector of minimum ionizing particles, a cosmic ray telescope was set up around the CCD cold box. It consisted of four scintillator counters and two small multi-wire drift chambers, situated above and below the CCD. The drift chambers consisted of nine wires each in the x and y directions. The wires were stacked in staggered planes to resolve the right-left ambiguity during track fitting. With this setup, a track could be interpolated to the plane of the CCD with a spatial resolution of 50 μm. When the system was taking cosmic ray data, it cycled between a "fast clear" mode to clear accumulated dark current and an integration mode which enabled the trigger for one second. When a cosmic ray external trigger occurred, the CCD was read out into a frame memory module, cleared, and read out again into a second memory following a delay equal to the integration time just prior to the trigger. This procedure provided an accurate measure of the dark current background, pixel-by-pixel.

We ran in this mode for approximately one month and accumulated about 180 cosmic rays whose tracks extrapolated through the CCD. Figure 8.10 shows the pulse height distribution for these cosmic rays. Only the maximum pulse

height in a window 20 pixels by 20 pixels about the extrapolated position of the particle is plotted here. Assuming a mean muon energy of 2 GeV, the expected Landau distribution,[45] fits the data quite well. From this calculated distribution we expect a maximum detection efficiency of 95% for a threshold set at 20 ADC units. The actual efficiency found, assuming a window of 20 pixels, was 70%. A large part of the discrepancy is thought to be due to soft components of the cosmic ray spectrum that scatter out of this window. To further study these devices as particle detectors would require running them in a particle beam of known momentum so that efficiencies could be thoroughly studied.

8.6 Radiation Studies

Application of CCDs in space satellites has motivated extensive studies of radiation damage.[46,47] The source of damage of primary concern for a vertex detector at the SLC is predominately γ radiation. This damage is principally due to two mechanisms. The first is ionization of the SiO_2 layer that insulates the clocking gates from the depleted layer, resulting in an offset in the clocking voltages. At low levels this can be compensated by an overall shift of the clocking voltage levels; the magnitude of the effect depends on how the clocking gates are biased during the irradiation. In our study, the CCD was DC biased at typical operating voltages. The second mechanism is the production of additional charge trapping states at the Si-SiO_2 interface which can cause an increase in the dark current as well as decrease the charge transfer efficiency.

The damage from ionizing radiation can be reduced by simplifying the CCD clocking gate structure, and employing "buried channel" technology. In a "buried channel" CCD, charge is transferred in a channel physically separated from the Si-SiO_2 interface, isolating the signal charge packet from any disrupting influences present at that interface. Since the CCDs studied in this report have both these features, it was expected that they would be exceptionally resistant to ionizing radiation.

The CCD was studied after a series of MeV γ radiation exposures to determine the maximum dose the device could survive as a small signal detector. The γ rays were supplied by a 11,000 Curie ^{60}Co source. Radiation dosage was calibrated to 5% with potassium nitrate dosimetry. The CCD was mounted on a circuit board and appropriate DC voltages were applied to each electrode to simulate operating conditions in a colliding beam environment. The device response was measured after accumulated dosages of 5, 15, 25 and 40 Krad. Three operating characteristics were monitored: 1) variation in the operating voltages for satisfactory performance of the chip, 2) degradation of charge transfer efficiency, and 3) increase in background signal.

The change in the optimal clocking voltages was insignificant up to the highest dose studied. No significant effect on the serial or parallel charge transfer efficiency, as measured by using the ^{55}Fe source, was evident. The dark current of the 40 Krad irradiated device did however increase by a factor of 5 although the current was still negligible at -30°C. The dark current dependence on temperature of the irradiated device as compared to a non-irradiated device is shown in Figure 8.11. The response of the 40 Krad irradiated CCD to ^{55}Fe X-rays at -30°C can be seen in Figure 8.12. This pulse height distribution was generated with the same algorithm as described in Section 8.1. The reason for the two-fold increase of the ^{55}Fe width is not known. The broadening is not due to an increase in the average dark current, which is still negligible at -30°C, or significantly worse charge transfer efficiency. The noise contribution from the on-chip amplifier was studied by decoupling the amplifier from the array by clamping the reset gate high while reading out the CCD. Very little increase in the amplifier noise was found in the irradiated device. Although no cosmic ray data was taken with the irradiated device, it is clear from Figure 8.12 that the device would still be a sensitive detector for minimum ionizing particles.

8.7 Summary of Results

In summary, we have shown that the small signal characteristics of the Texas Instruments 4849 CCD are adequate for the purposes of a charged particle detector and have verified this by successfully detecting cosmic rays. The performance of the CCDs we studied deteriorated rapidly above temperatures of 0°C even though the average dark current remained within acceptable limits up to +10°C. The maximum readout speed we were able to achieve with a three level clock was 450 KHz. This is about a factor of four too slow for application to a real CCD particle detector operating at the SLC but somewhat different clocking sequences would increase this readout rate significantly. Finally, a typical CCD was capable of withstanding exposure to 40 KRad of ^{60}Co gamma radiation and remain operational as a small signal detector. This implies that the Texas Instruments 4849 CCD would make a good candidate for a charged particle or X-ray detector in a relatively high radiation environment.

9. Vertex Detector Mechanical Design

In addition to the device tests outlined above we also initiated a mechanical design for mounting the CCDs in a three-dimensional structure around the interaction point. The essential feature of the design was a rigid structure with a minimum of supporting material. The basic elements consisted of 24 U-shaped ceramic sheets overlapped like a paddle wheel to surround the interaction point as shown in Figure 9.1. Each ceramic substrate carried five CCDs with the electrical connections bussed to either end by a two layer metallization fabricated by the Promex Corporation using standard thick film hybrid circuit techniques. The substrate was 400 μm thick aluminum oxide; a thinner material was intended for the actual detector. The geometric layout can be inferred from a photograph of the mask for the first metallization layer shown in Figure 9.2. Although one or

two of these hybrid structures were built and loaded with chips they were never performance tested.

The approximately cylindrical shape of the overall detector was to be provided by a bicone assembly, slotted to support the ends of the ceramic substrates carrying the CCDs and allowing penetration of the signal and clocking electrodes to the detector ends. A model of this arrangement was constructed and is shown in Figure 9.3. Two parts of the detector design were never well specified; the inner and outer heat shields and the endcap connector layout and gas manifold. The latter problem is probably the most difficult for any CCD vertex detector given the constrained volume surrounding the colliding beam interaction point.

10. Conclusions

The Texas Instruments "Virtual Phase" chip has been demonstrated to perform remarkably well as a detector of low energy X-rays and minimum ionizing charged particles. For X-rays energies up to 8 KeV the present devices with 12 micron depletion depth are almost ideal; greater depths would be useful for charged particles so that the readout requirements could be relaxed. The Texas Instruments devices appear to be less sensitive to ^{60}Co radiation damage than other types of silicon CCDs, consistent with the simpler electrode structure and the behavior of other MOS devices.

The electronic readout used in our development work could easily be expanded to serve the requirements of a complete vertex detector. The mechanical design is the one area which would require the most effort to yield a finished detector. Since the Texas Instruments chips perform well under relatively warm conditions, elaborate heat shields are not necessary, thereby simplifying the design.

In comparison to silicon strips, CCDs offer the possibility of true space point determinations which, if properly exploited, would immensely ease the compu-

tational burden of track reconstruction. However they are significantly more complex devices leading to inevitably greater difficulties in the management of a large number of signal and control cables in the crowded region near the interaction point. Their principle advantage is the additional independent measure of impact parameter which is likely to repay for the extra effort with greater statistics and less ambiguity.

At the conclusion of this project the entire development system of electronics, mechanical support, and software was turned over to a solid state X-ray scattering group led by Professor Roy Clarke. The apparatus described above will be used for detecting low energy X-rays in experiments at the Brookhaven Synchrotron Light Source.

11. Acknowledgements

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FIGURE CAPTIONS

Figure 2.1: The impact parameter, b, for a track associated with a secondary vertex. The event is shown in the plane perpendicular to the colliding e^+e^- beams.

Figure 2.2: The momentum distribution of charged particles from b mesons produced from e^+e^- collisions at $\sqrt{s} = M_Z°$.

Figure 2.3: The statistical limits on the impact parameter error as a function of the charged particle track momentum in the Mark II detector. These limits depend both on the performance of the CCD and the central tracking drift chamber (TDC).

Figure 2.4: The number of synchrotron photons within an annulus of 1 mm width as a function of the annular radius for one pulse at the SLC.

Figure 3.1: Profile view of the physical structure and electrical potentials within a "Virtual Phase" CCD for two phases of the clock waveform.

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Figure 3.3: A cross section of a CCD with a traversing minimum ionizing particle.

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Figure 4.3: Block diagram of CCD control and readout system.

Figure 8.7: A pulse height distribution produced by the CCD at 0°C exposed to an ^{55}Fe source.

Figure 8.8: Pulse height versus column number for a typical row, (row =100), at -30°C and +5°C. The CCD was not exposed to an external signal source. Column 302 consistently produced a signal at all temperatures, and was masked out in the hardware.

Figure 8.9: A pulse height distribution produced by the CCD at -30° and exposed to a ^{106}Ru source. Split events have been removed. The peak at low pulse is the edge of the falling noise distribution. The curve is a theoretical calculation of the expected distribution.

Figure 8.10: A cosmic ray track pulse height distribution produced by the CCD at -30°C. The curve is a theoretical calculation of the expected distribution.

Figure 8.11: The dark current per pixel as a function of the inverse temperature of the irradiated and non-irradiated CCDs.

Figure 8.12: A pulse height distribution produced by the irradiated CCD at -30°C exposed to an ^{55}Fe source.

Figure 9.1: A perspective view of 120 CCDs arranged in 24 over-lapping planes surrounding the interaction point. Five CCDs are bonded to each plane and successive planes are staggered along the beam direction to produce complete coverage for $|\cos\theta| \leq 0.7$.

Figure 9.2: The first metallization layer for the ceramic substrate designed to support 5 CCDs. Clock signals are introduced by the traces on the right and signals are removed from the traces on the left.

Figure 9.3: Three-dimensional model of the proposed CCD vertex detector structure. Twenty-four ceramic planes support 120 CCDs around the interaction point. The scale is marked in inches.

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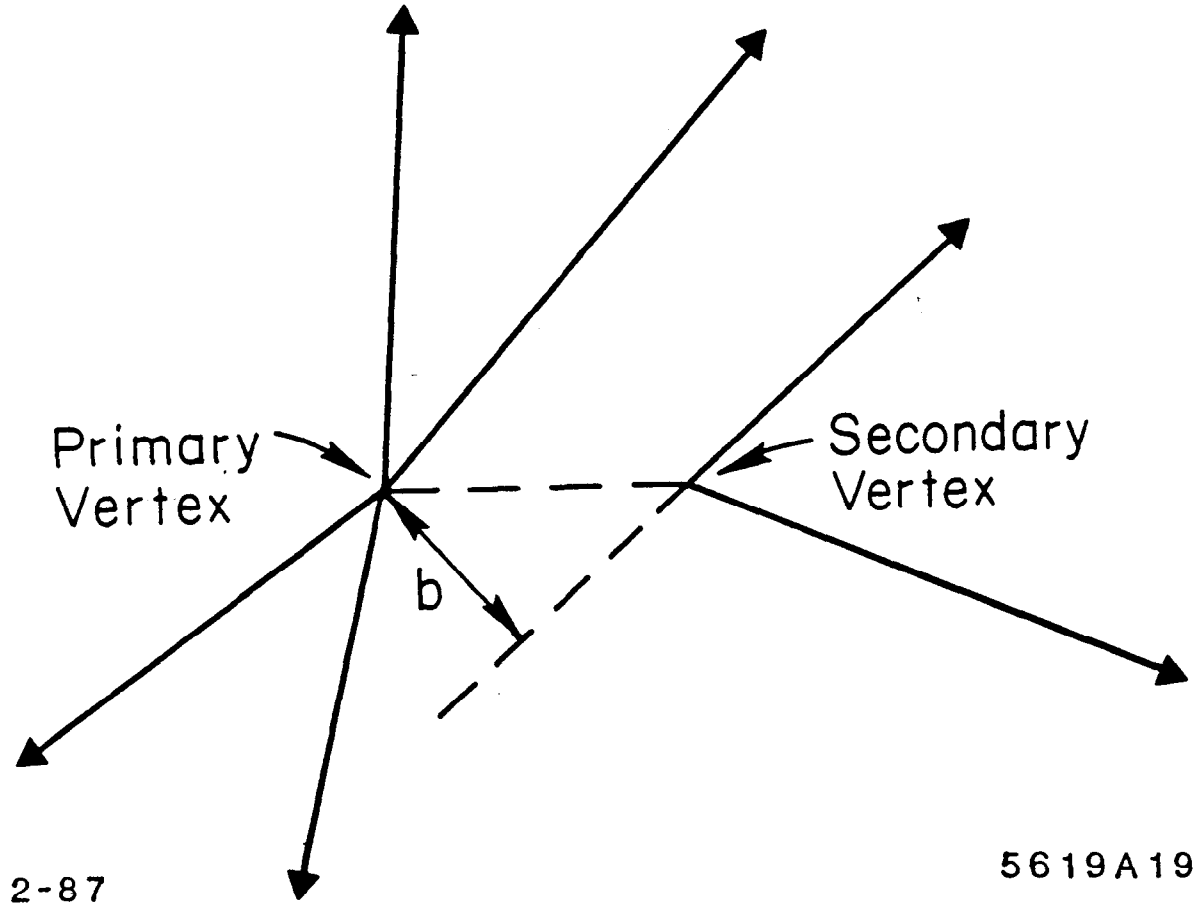

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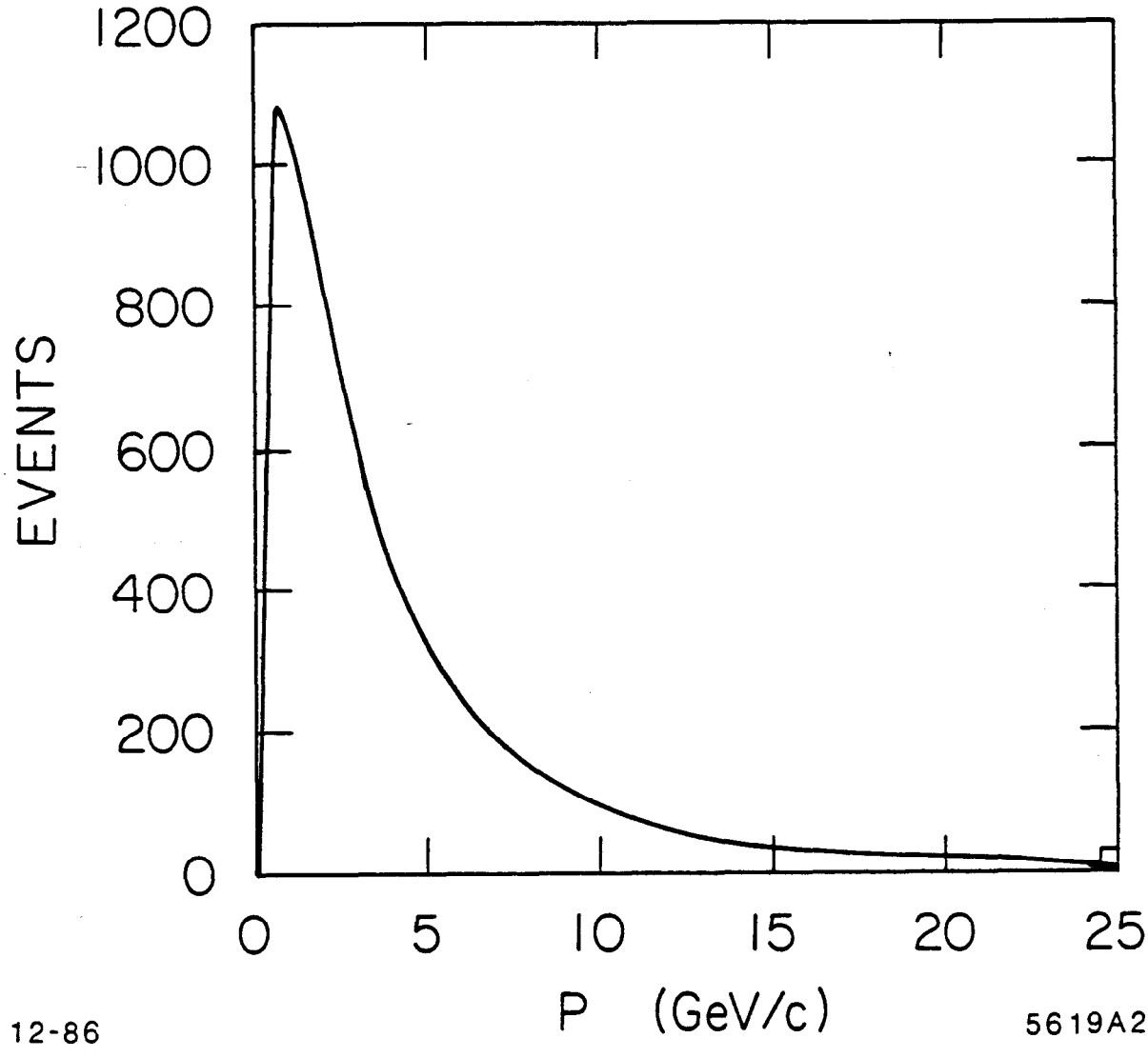

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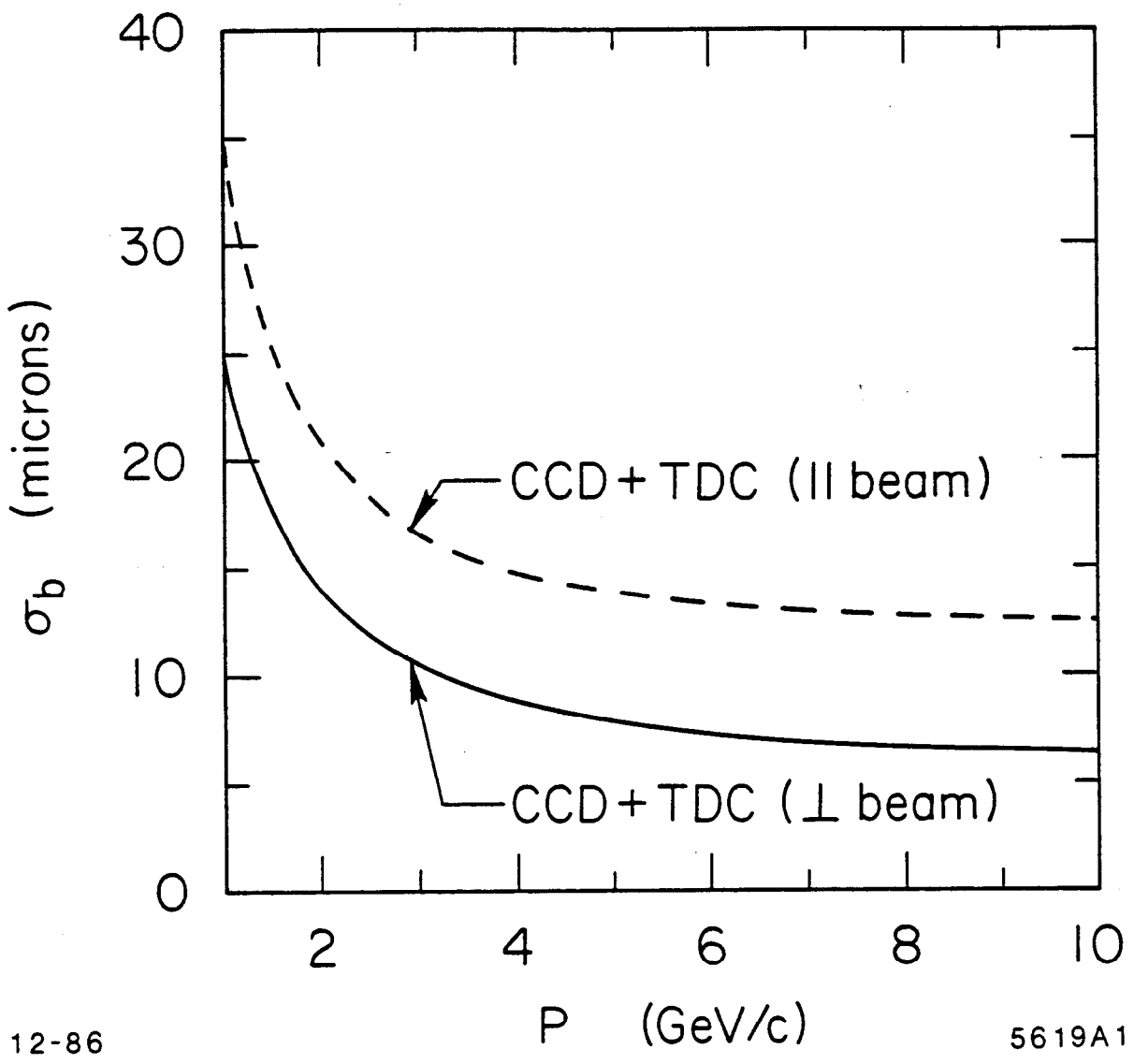

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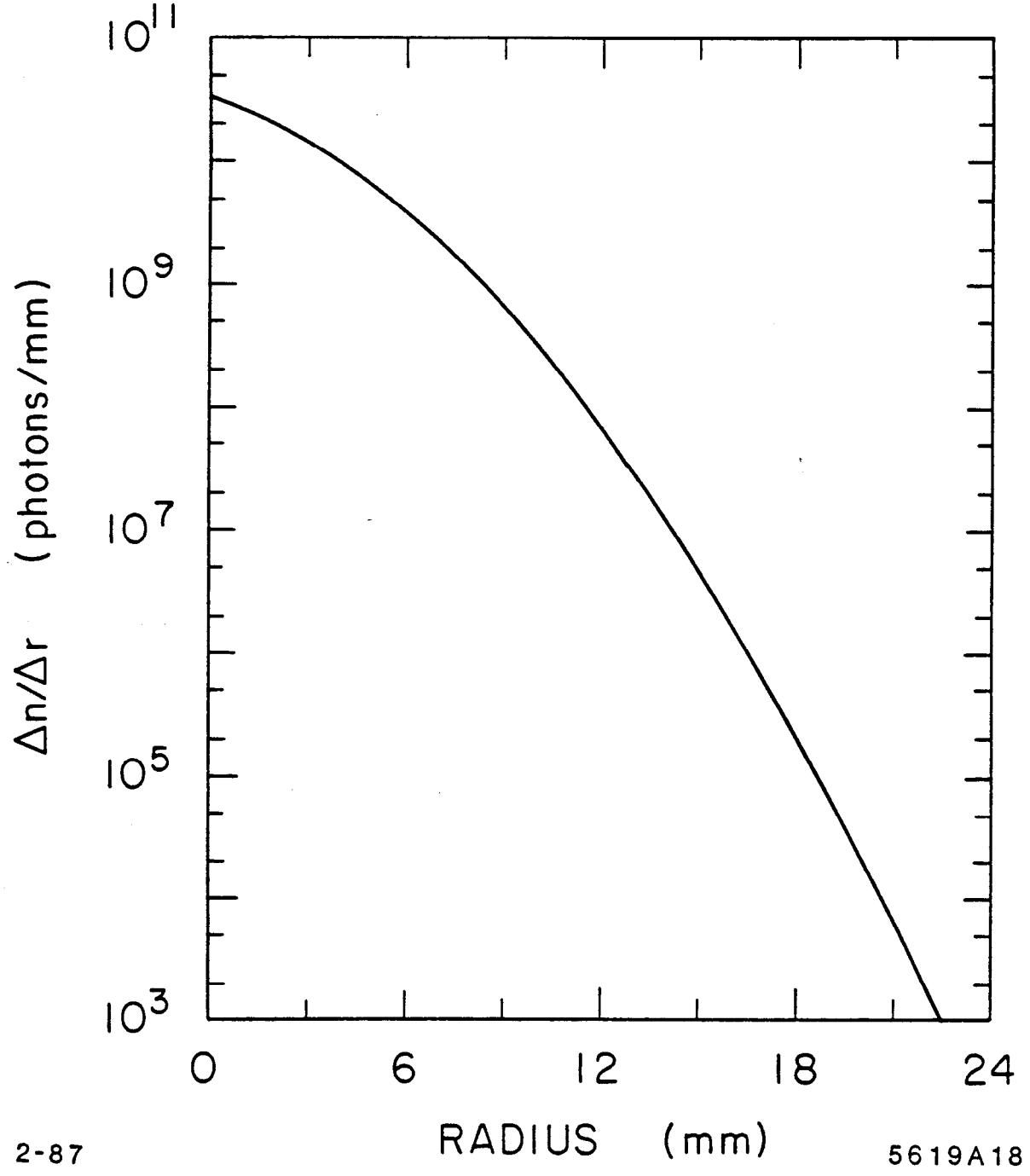

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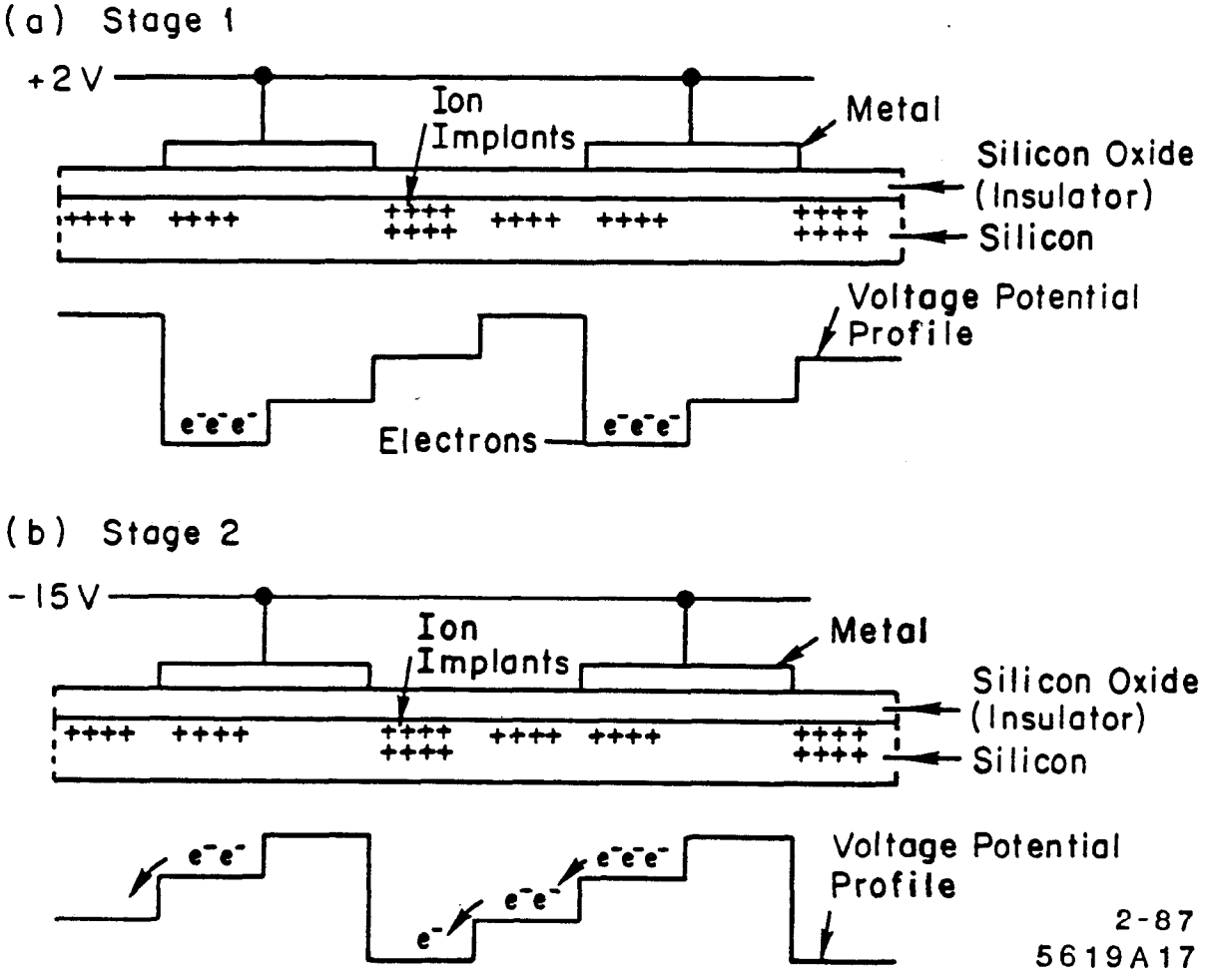


Figure 3.1: Profile view of the physical structure and electrical potentials within a "Virtual Phase" CCD for two phases of the clock waveform.

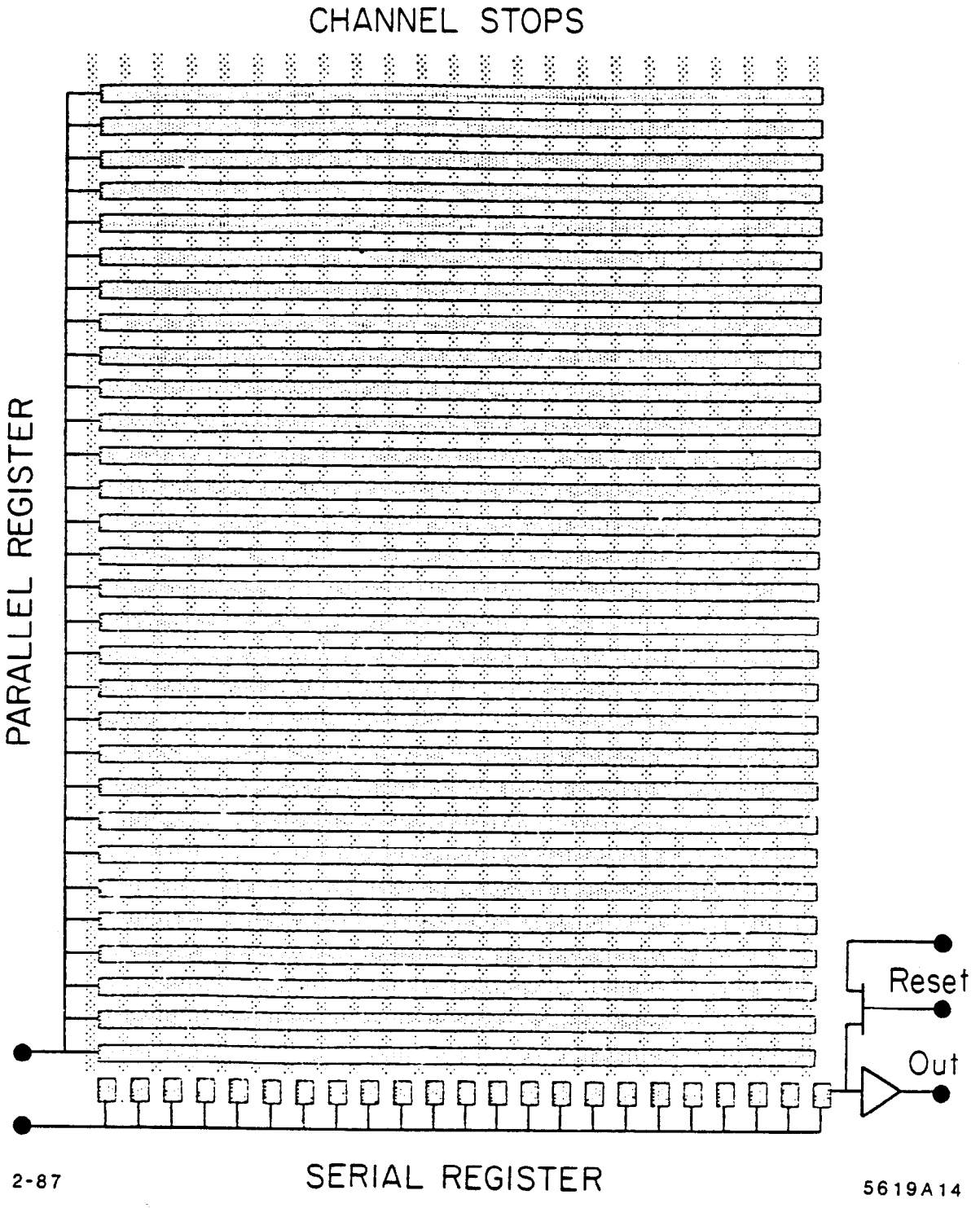


Figure 3.2: Schematic view of the electrode structure of the Texas Instruments "Virtual Phase" CCD.

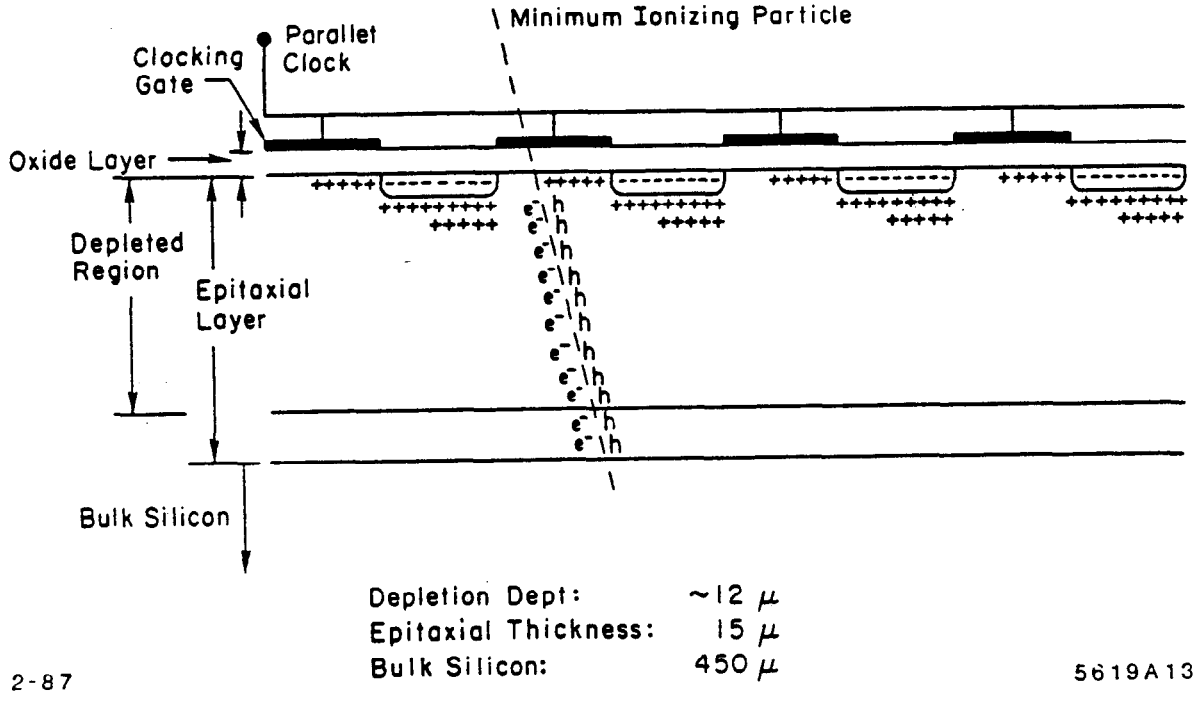
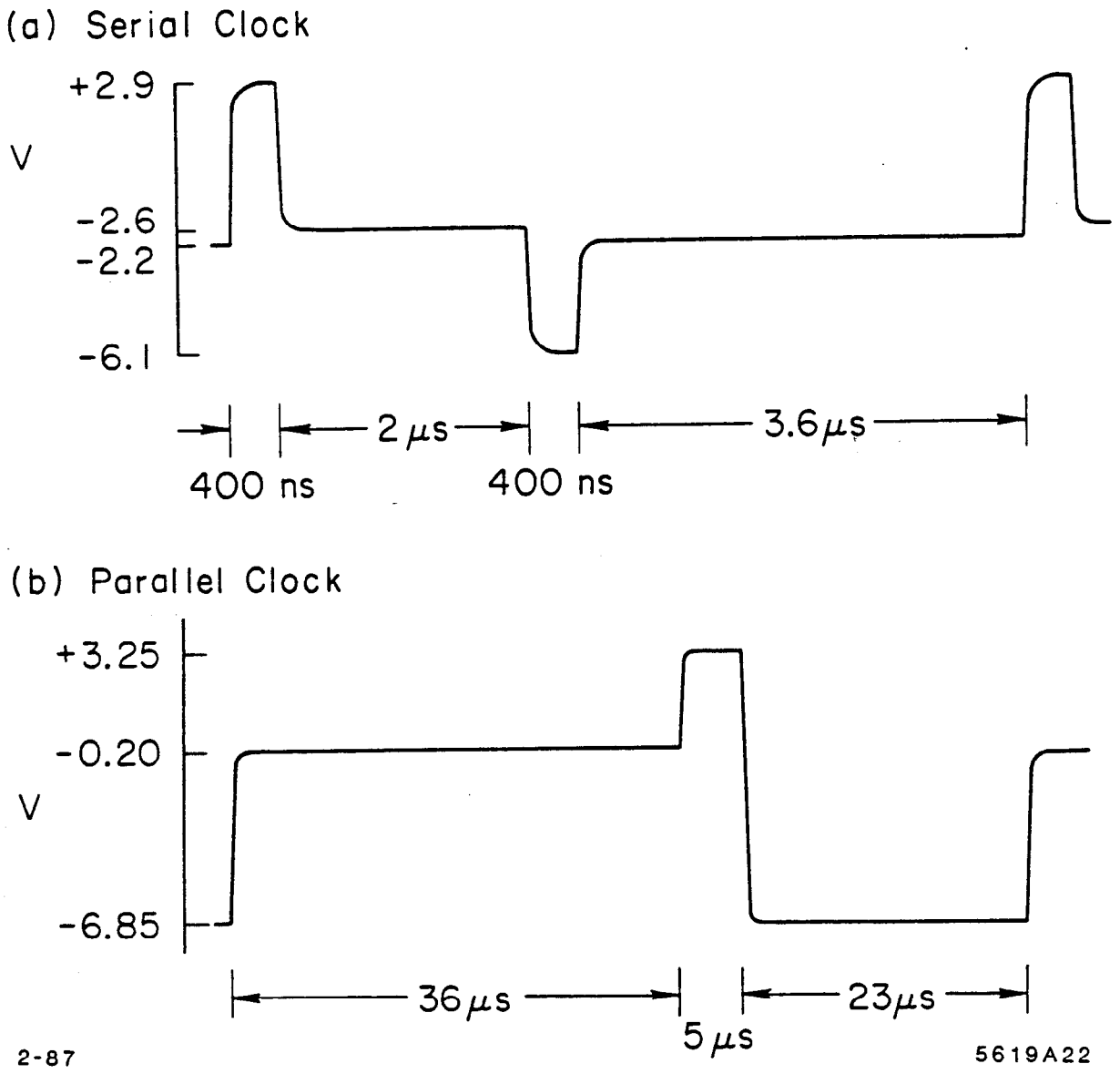


Figure 3.3: A cross section of a CCD with a traversing minimum ionizing particle.



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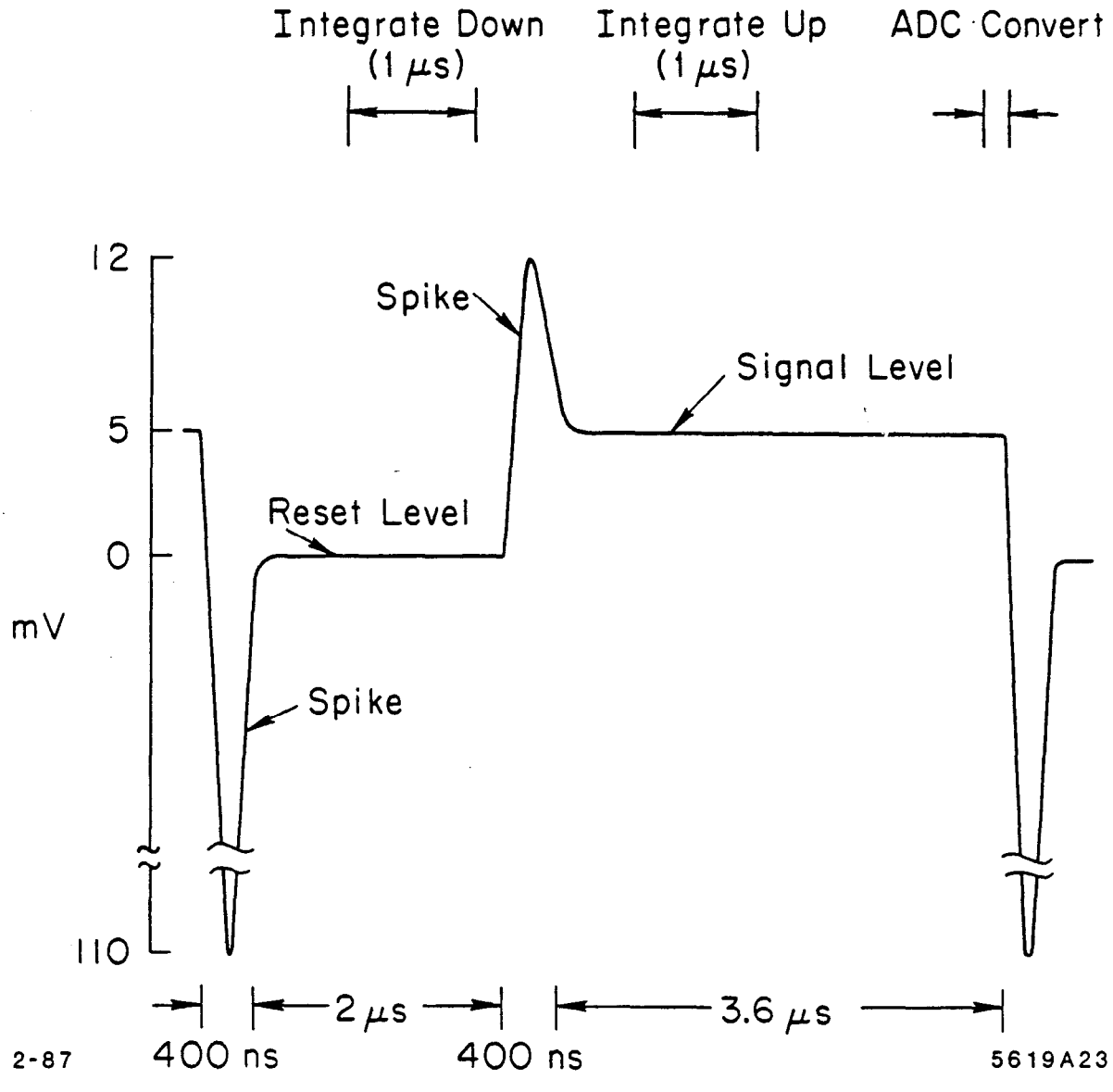

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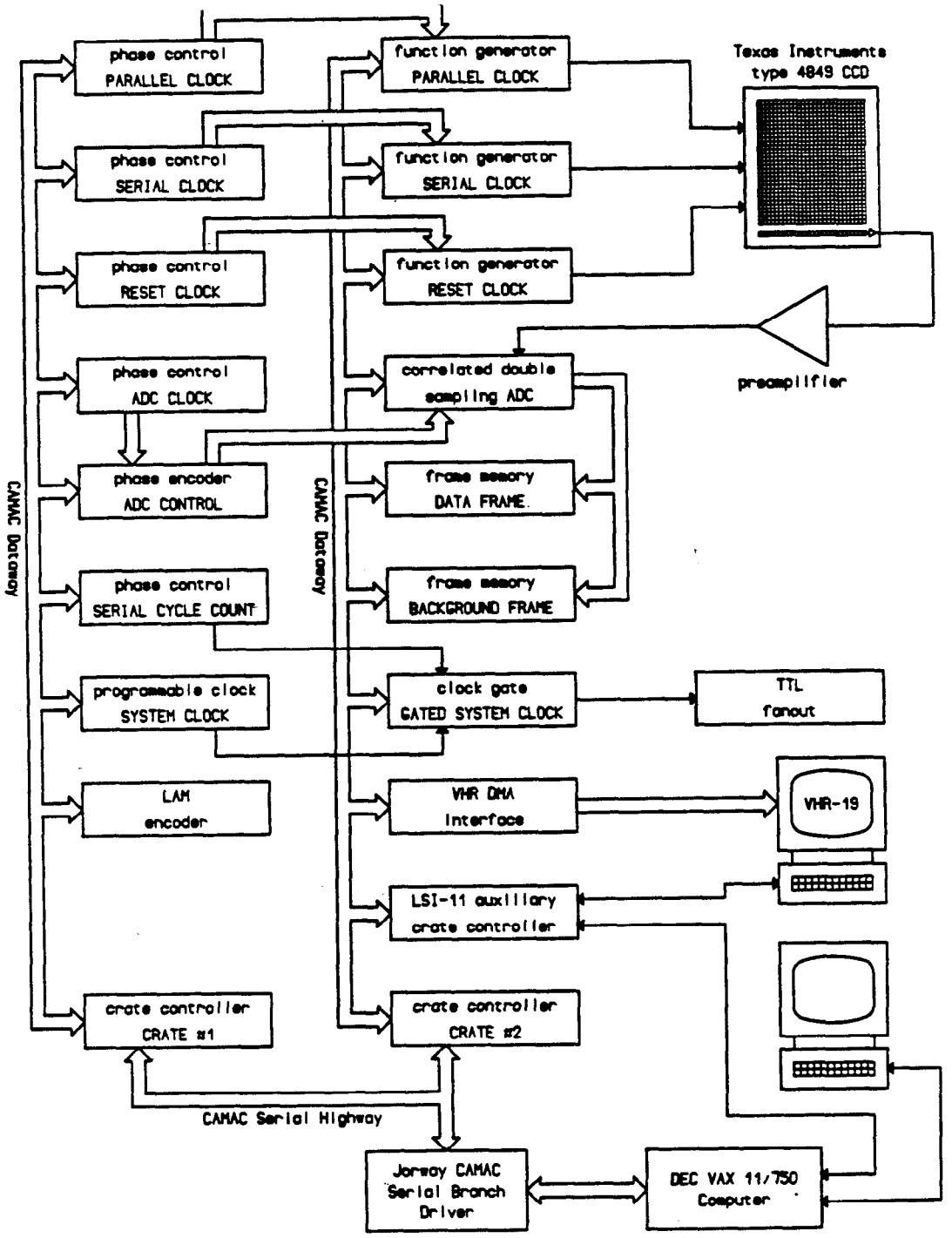

Figure 4.3: Block diagram of CCD control and readout system.

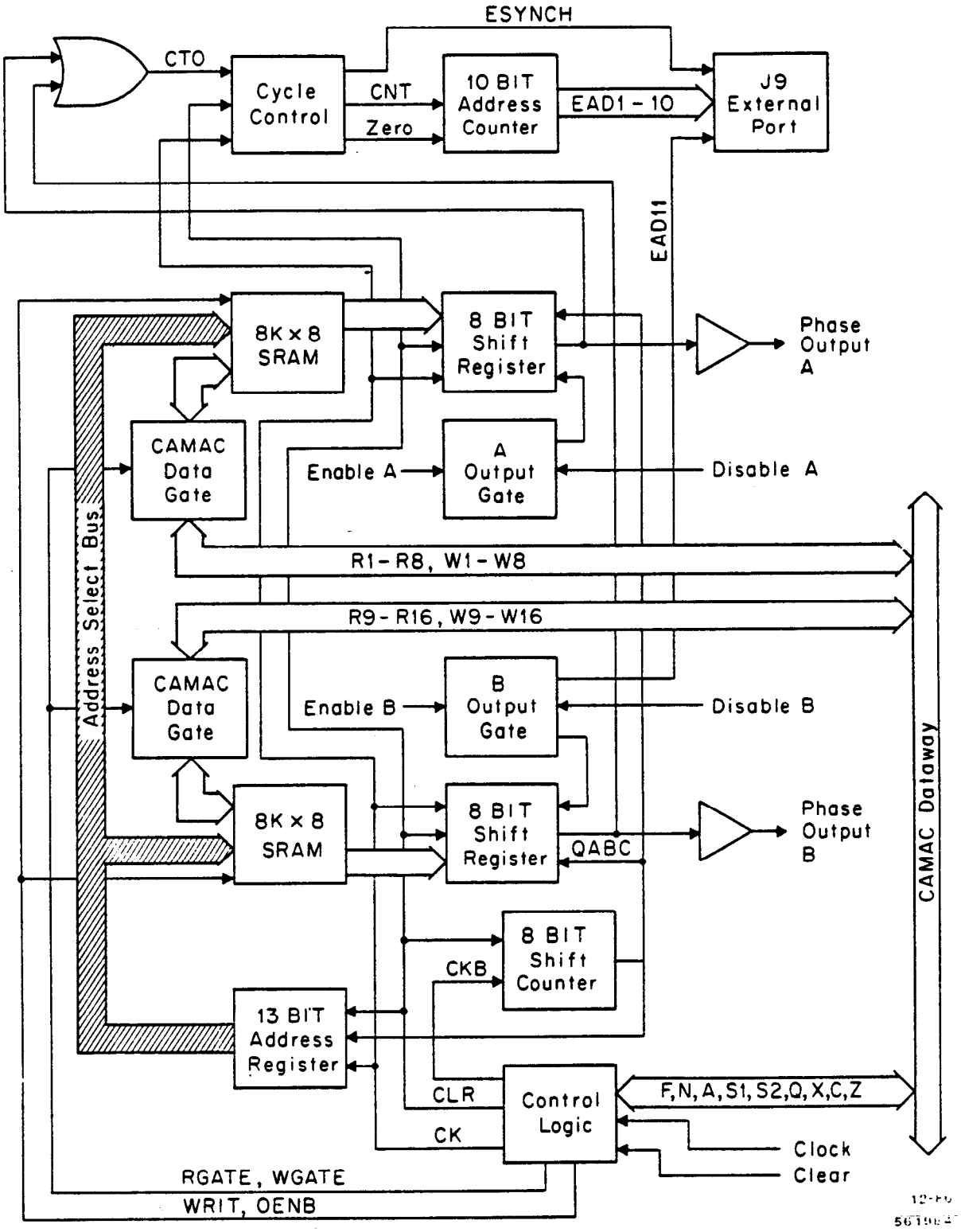

Figure 4.4: A functional diagram of the phase control module.

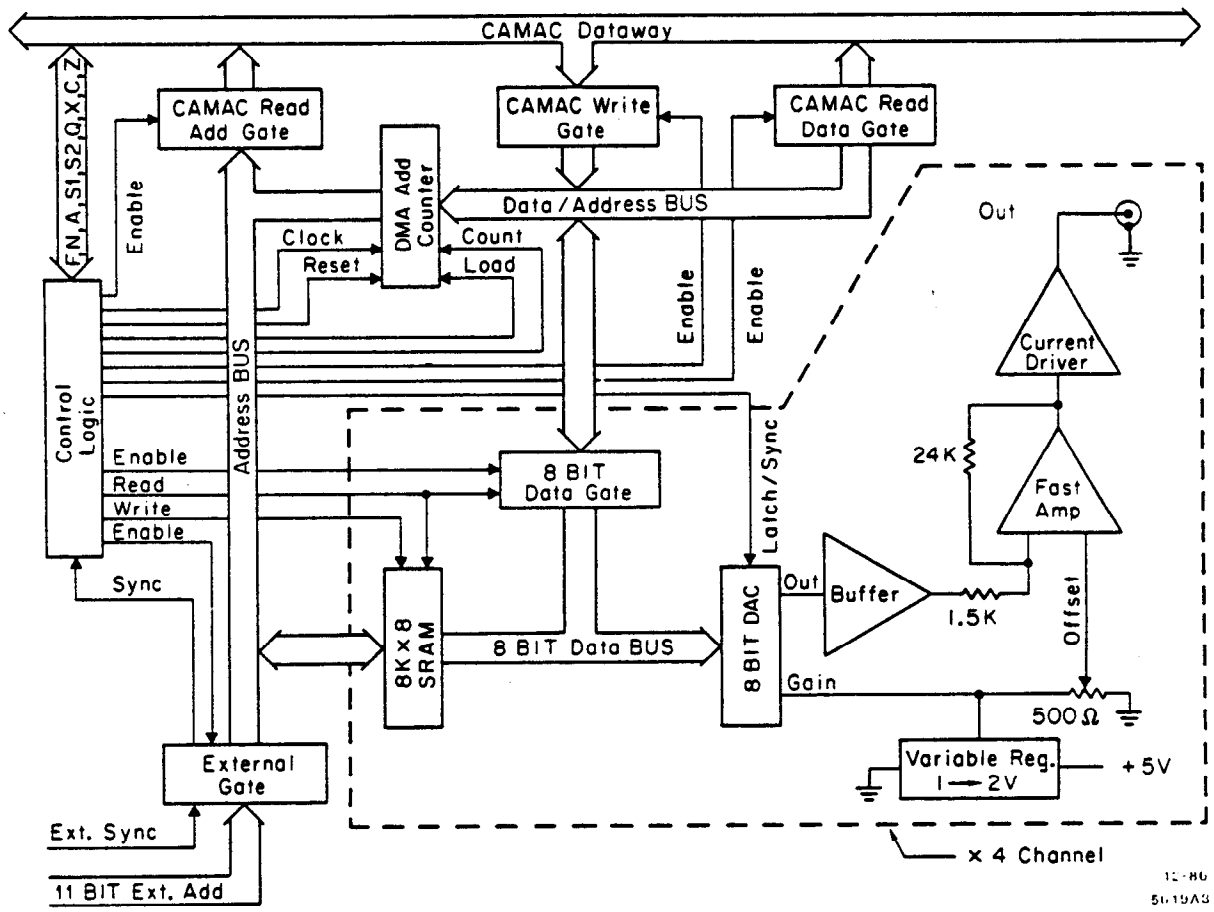

Figure 4.5: A functional diagram of the function generator.

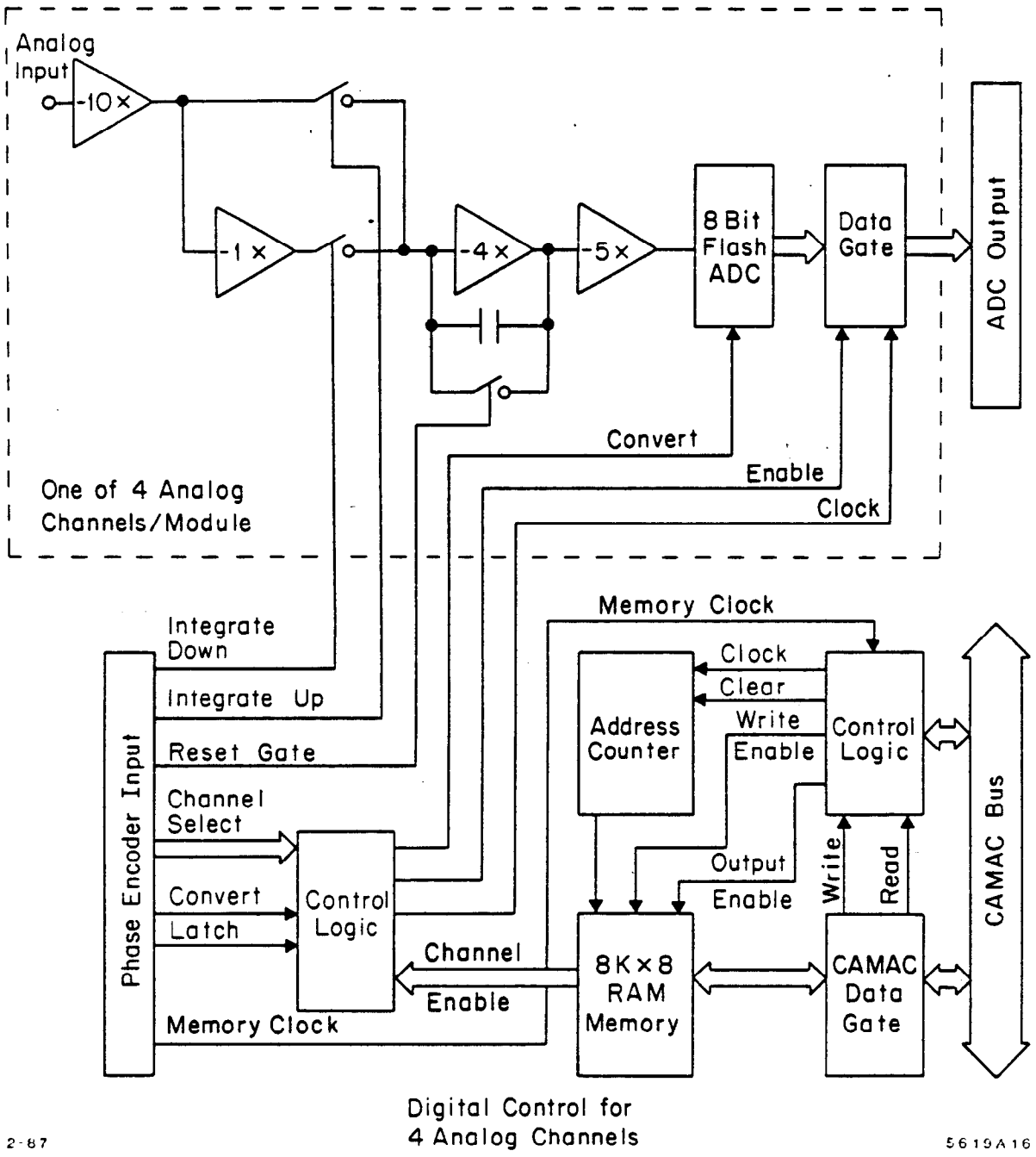

Figure 4.6: A functional diagram of the analog switch based ADC module.

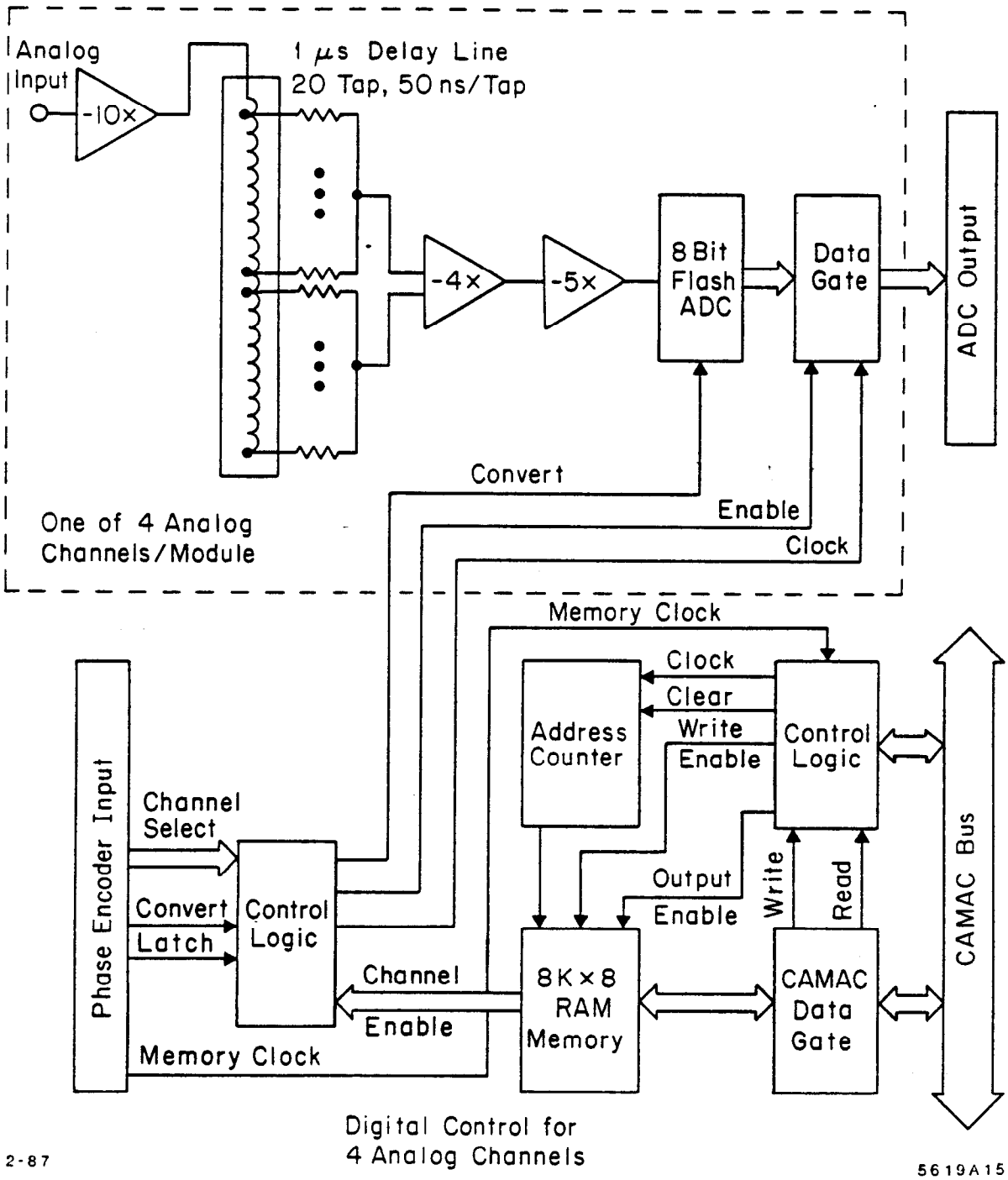

Figure 4.7: A functional diagram of the delay line based ADC module.

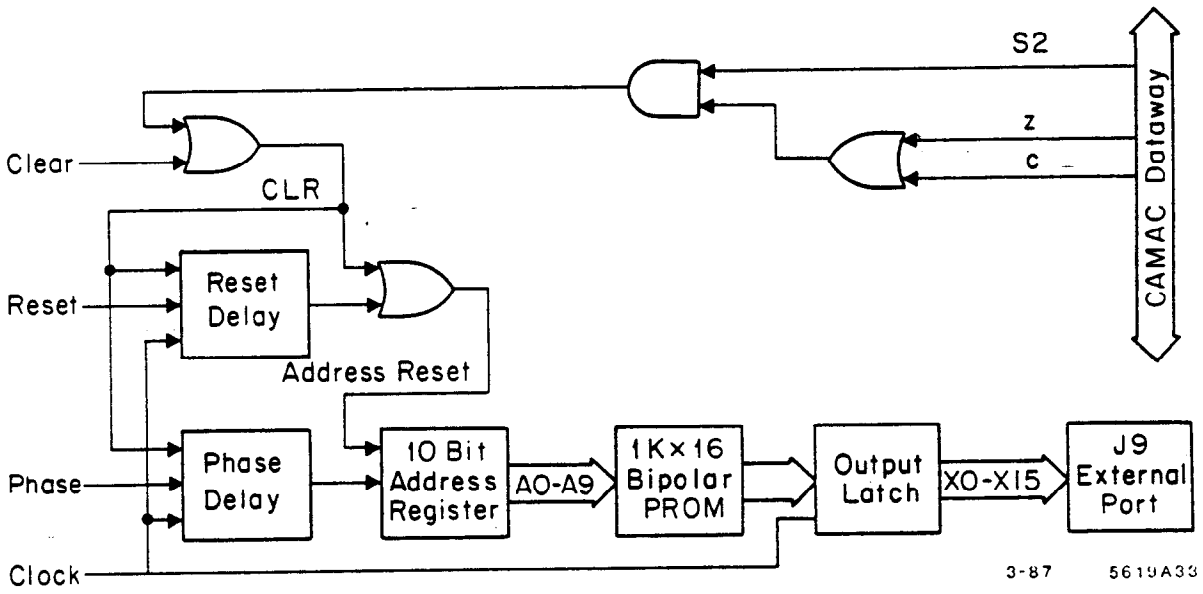

Figure 4.8: A functional diagram of the phase encoder module.

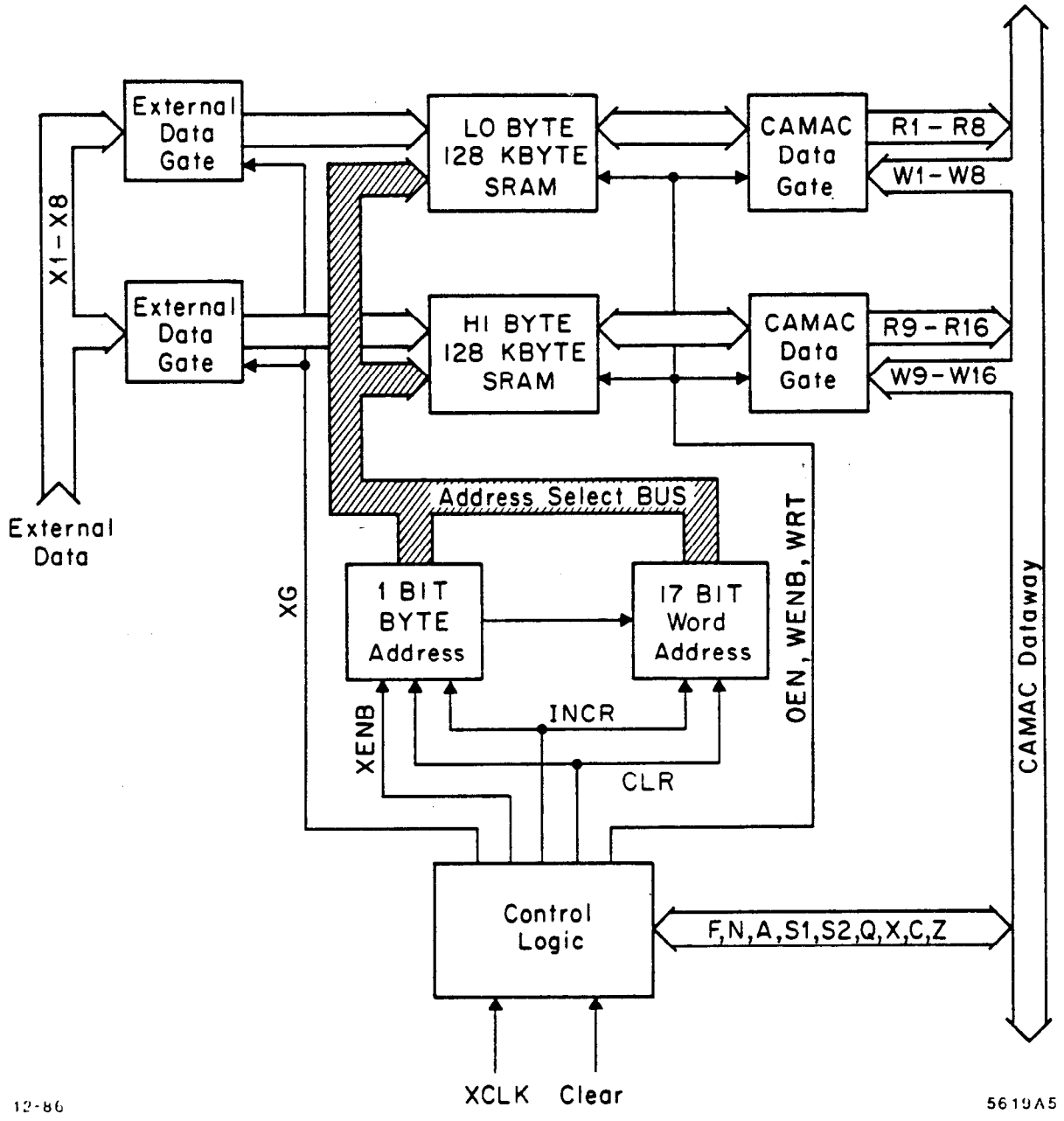

Figure 4.9: A functional diagram of the CCD frame memory module.

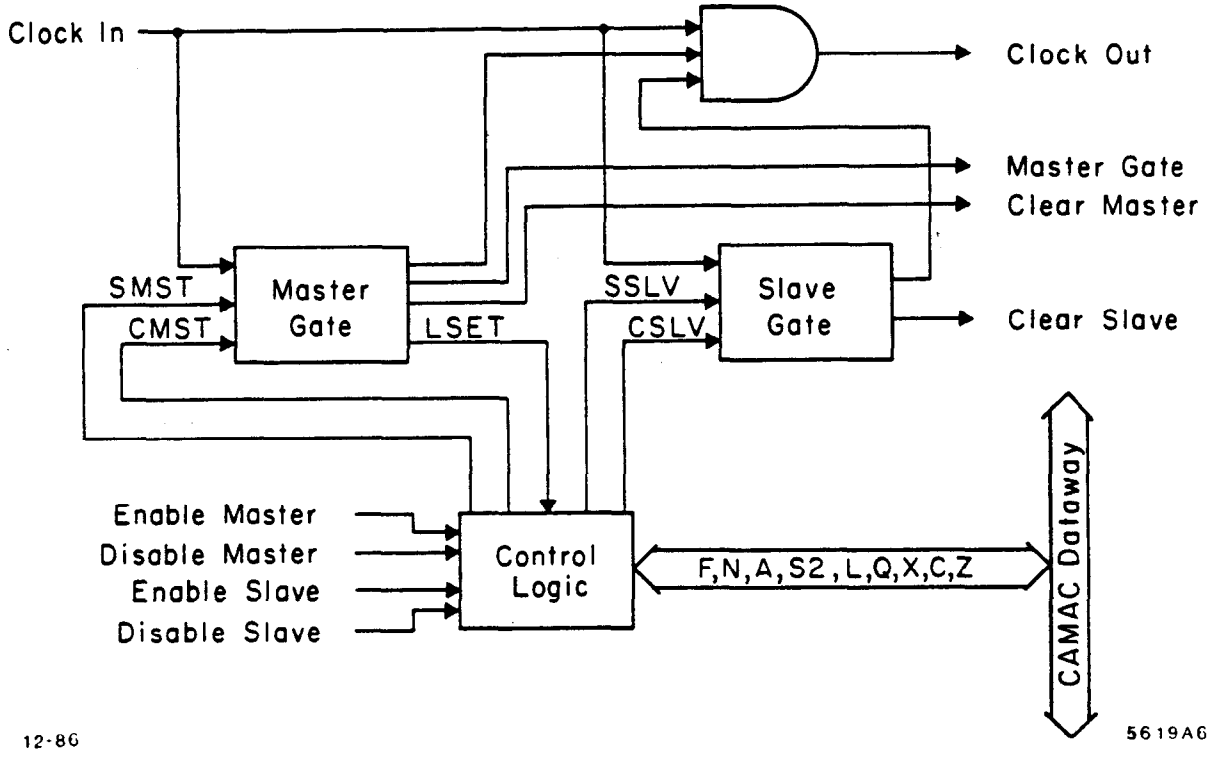

Figure 4.10: A functional diagram of the clock gate module.

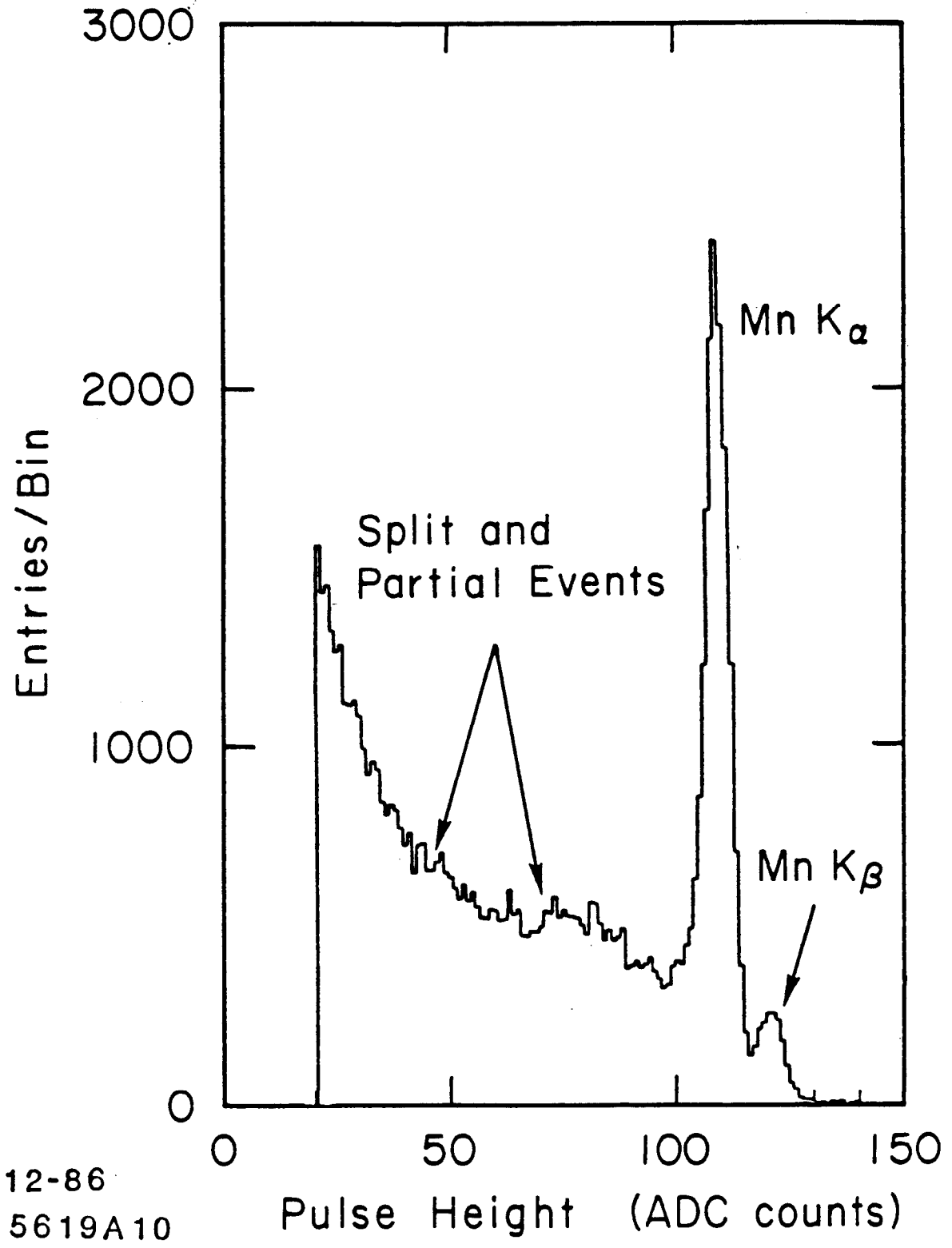

Figure 8.1: A pulse height distribution produced by a CCD at -30°C exposed to an ^{55}Fe X-ray source.

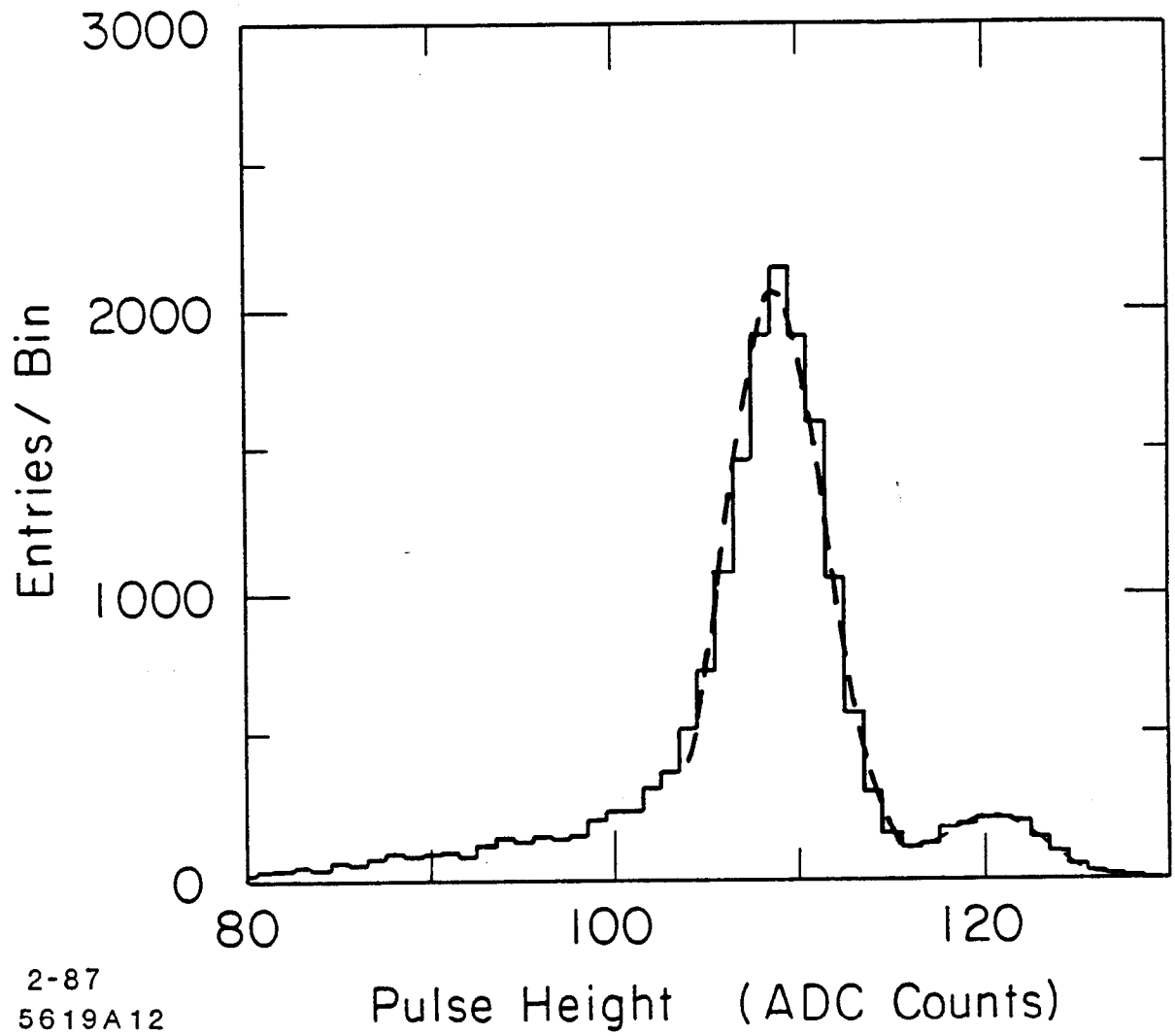

Figure 8.2: The pulse height distribution of Figure 8.1 with split events removed. Gaussian fits to the K_α and K_β peaks are shown.

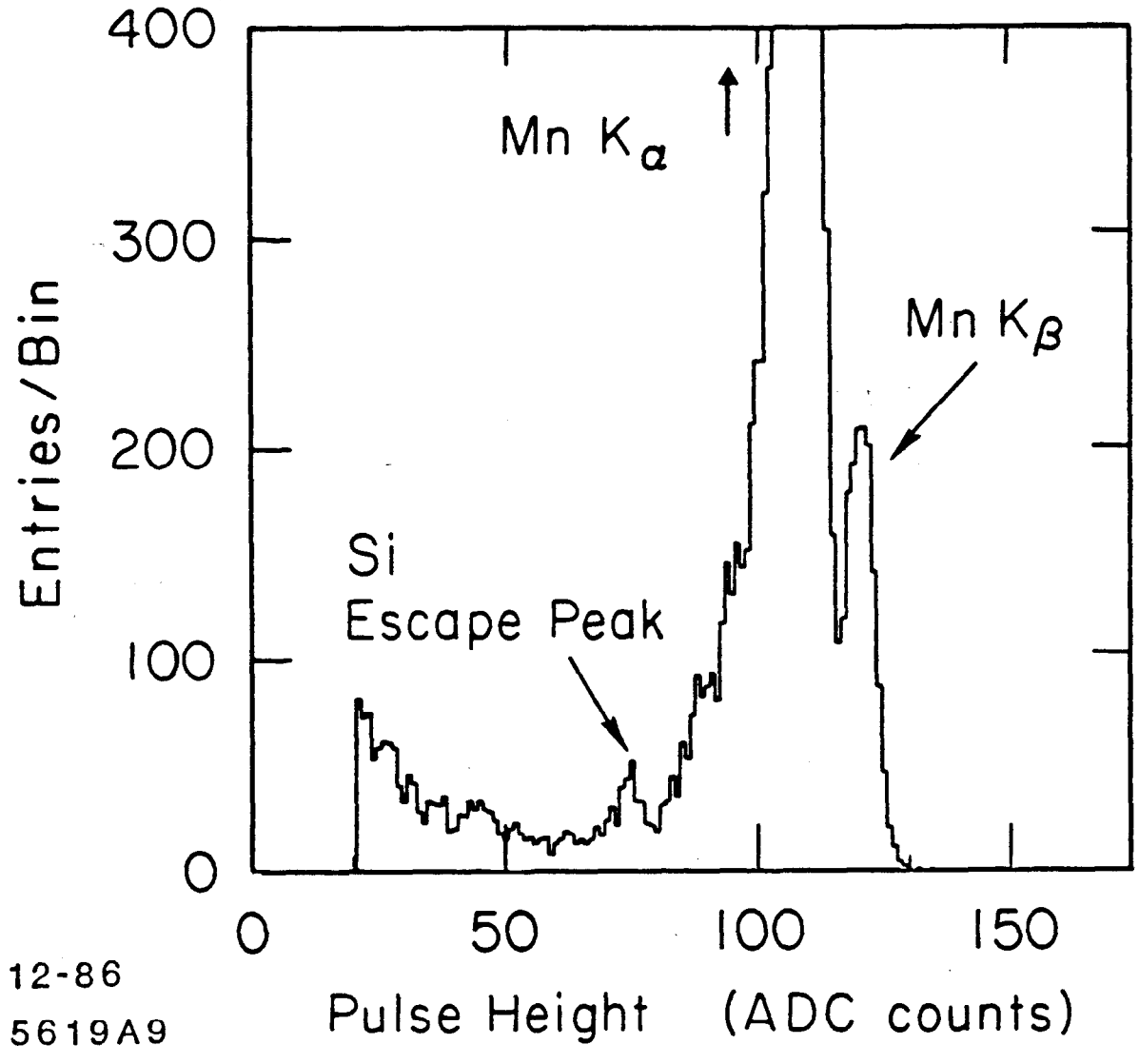

Figure 8.3: The pulse height distribution of Figure 8.1 with split events removed and the K_α truncated to show the structure of the noise floor. The silicon escape peak is indicated.

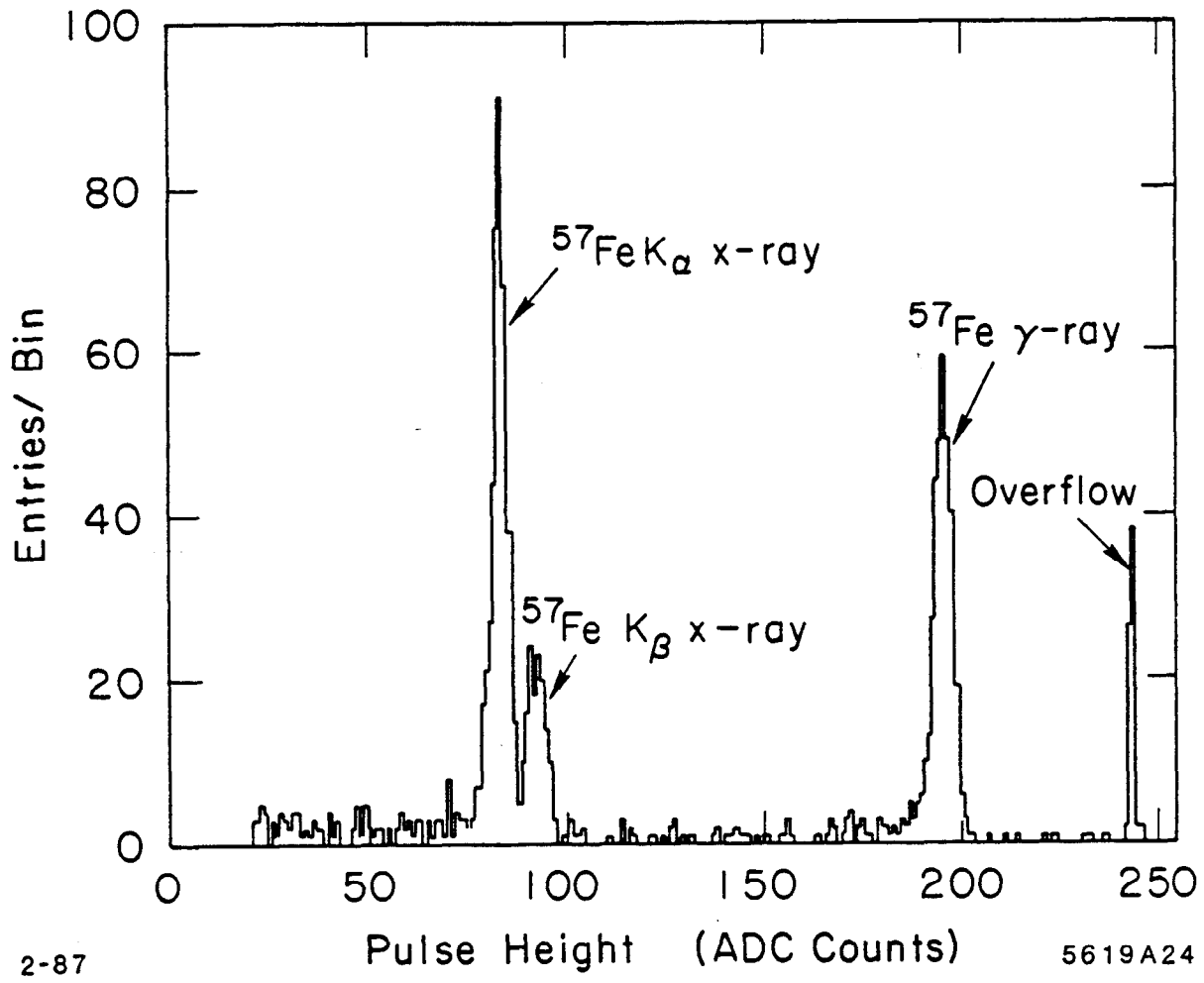

Figure 8.4: A pulse height distribution produced by a CCD at -30°C exposed to a ^{57}Co X-ray source.

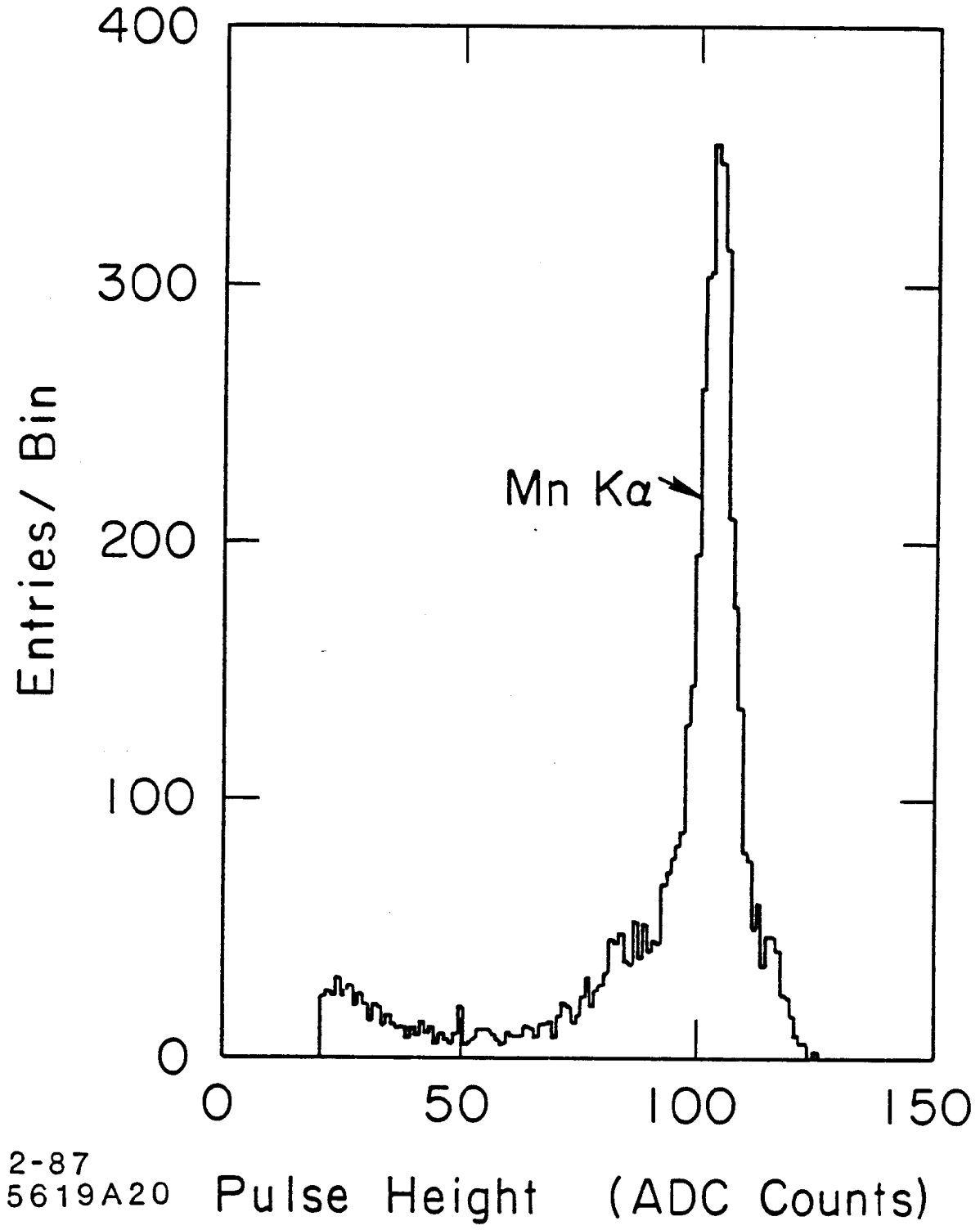

Figure 8.5: An ^{55}Fe pulse height distribution produced by a CCD at -30°C with a delay-line type ADC module.

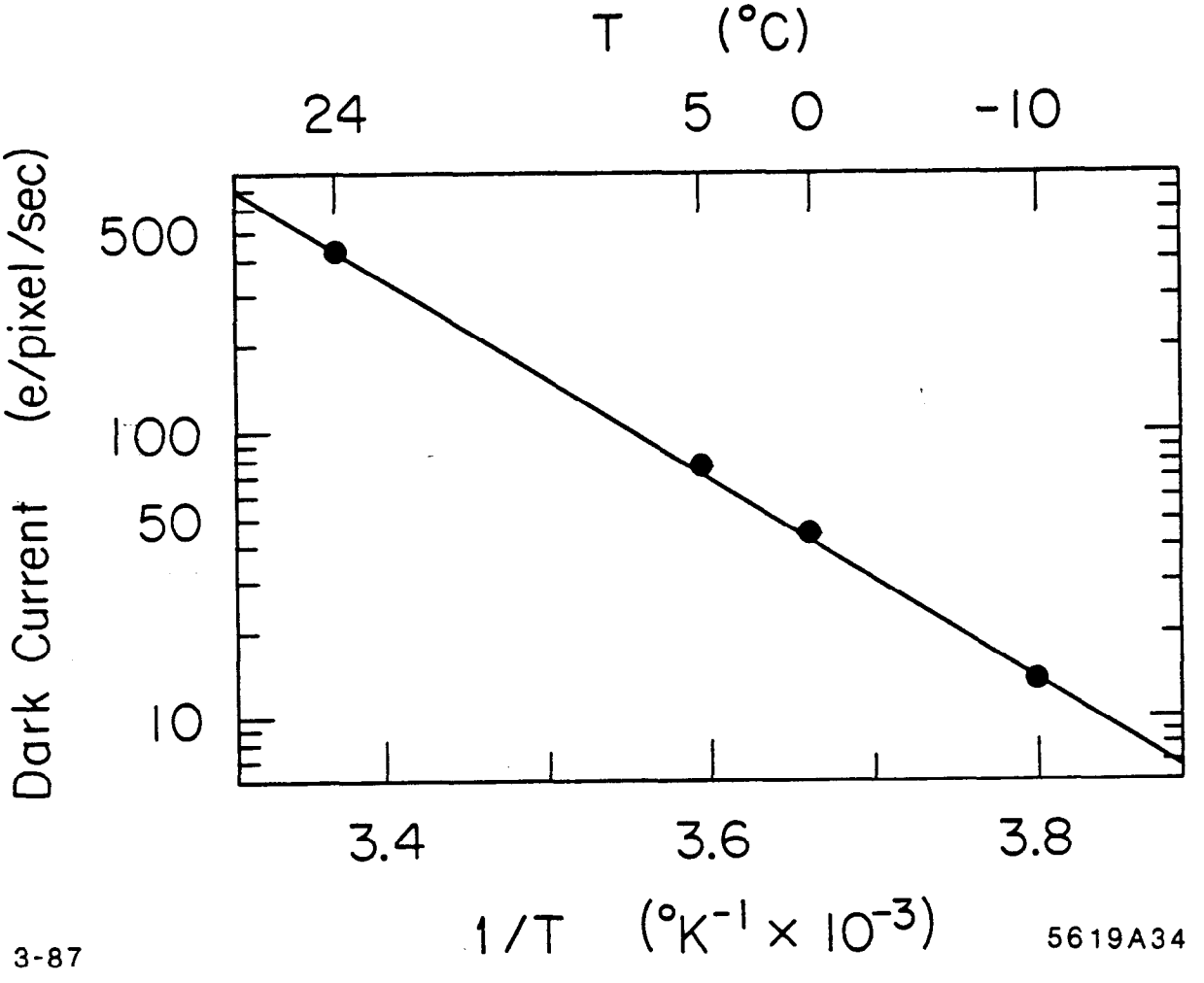

Figure 8.6: The dark current per pixel as a function of the inverse temperature of the CCD.

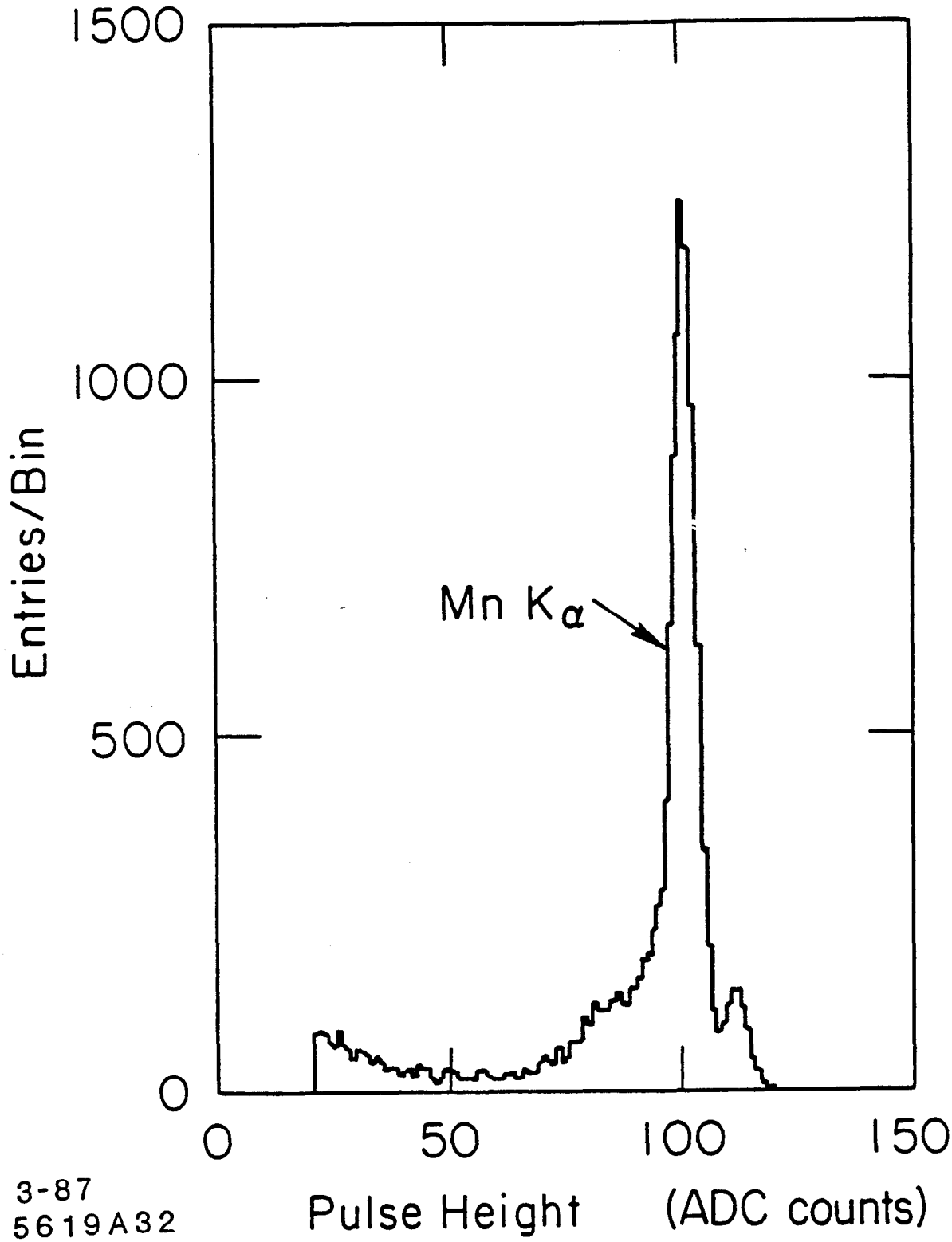

Figure 8.7: A pulse height distribution produced by the CCD at 0°C exposed to an ^{55}Fe source.

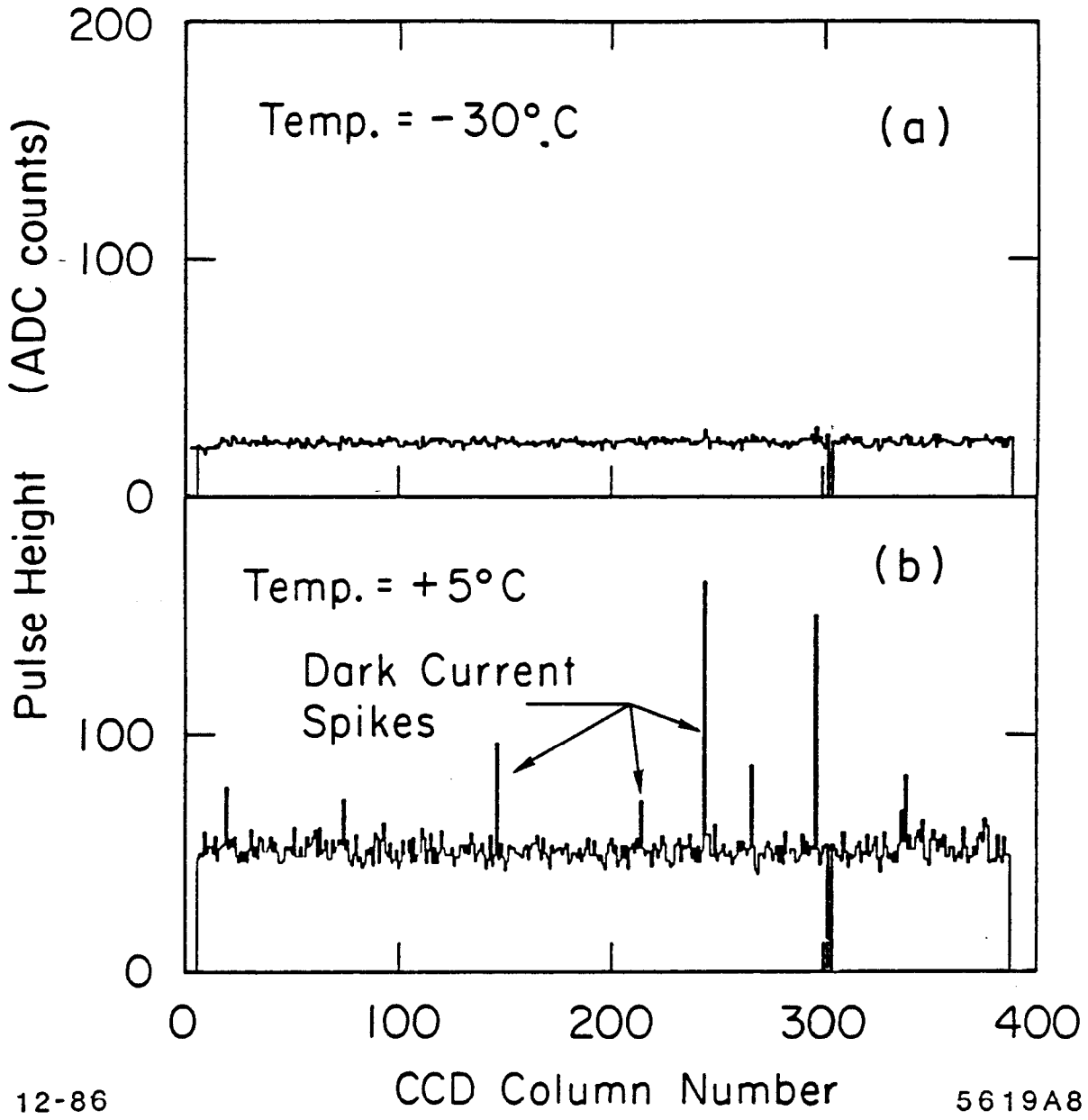

Figure 8.8: Pulse height versus column number for a typical row, (row =100), at -30°C and +5°C. The CCD was not exposed to an external signal source. Column 302 consistently produced a signal at all temperatures, and was masked out in the hardware.

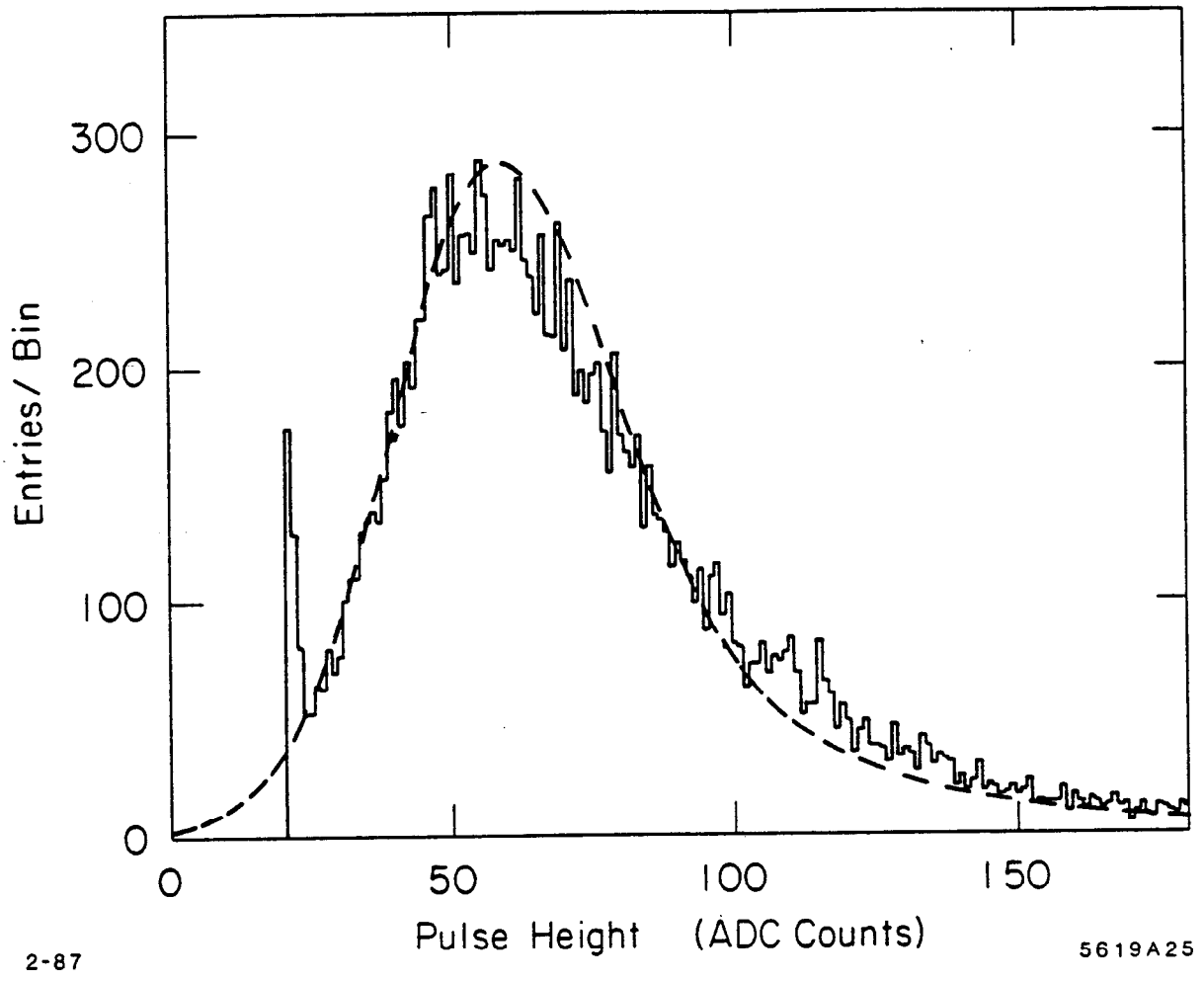

Figure 8.9: A pulse height distribution produced by the CCD at -30° and exposed to a ^{106}Ru source. Split events have been removed. The peak at low pulse is the edge of the falling noise distribution. The curve is a theoretical calculation of the expected distribution.

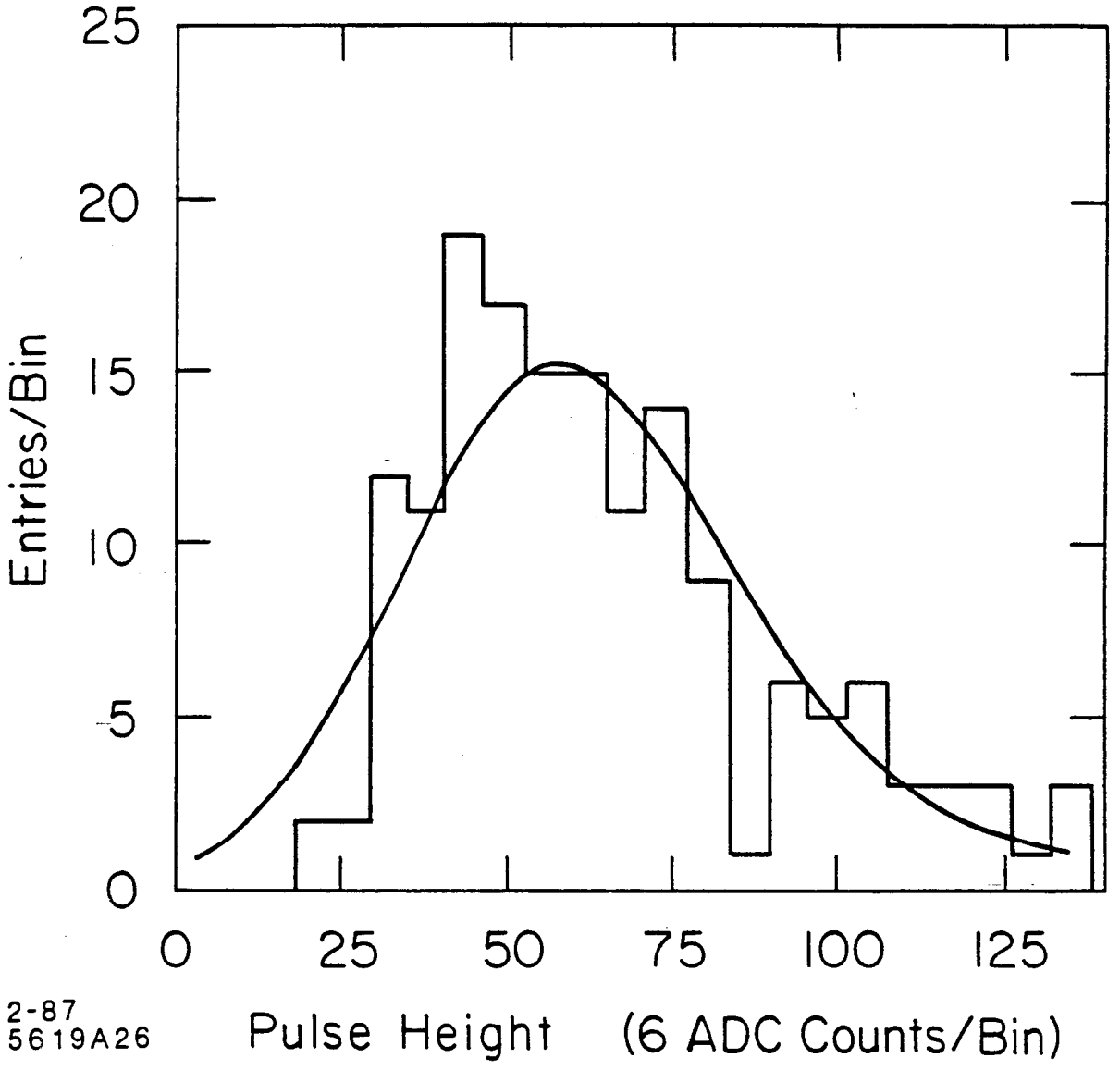

Figure 8.10: A cosmic ray track pulse height distribution produced by the CCD at -30°C. The curve is a theoretical calculation of the expected distribution.

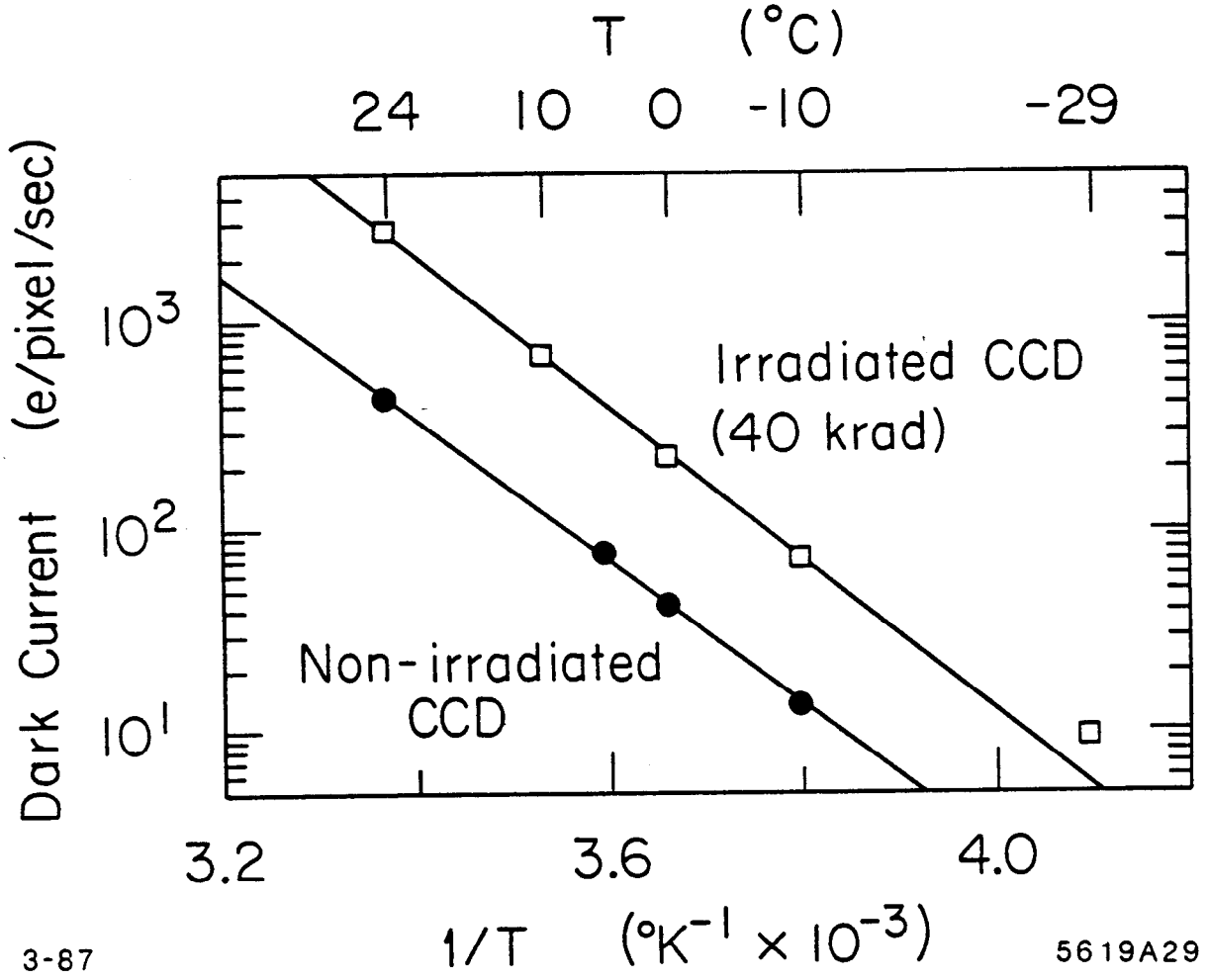

Figure 8.11: The dark current per pixel as a function of the inverse temperature of the irradiated and non-irradiated CCDs.

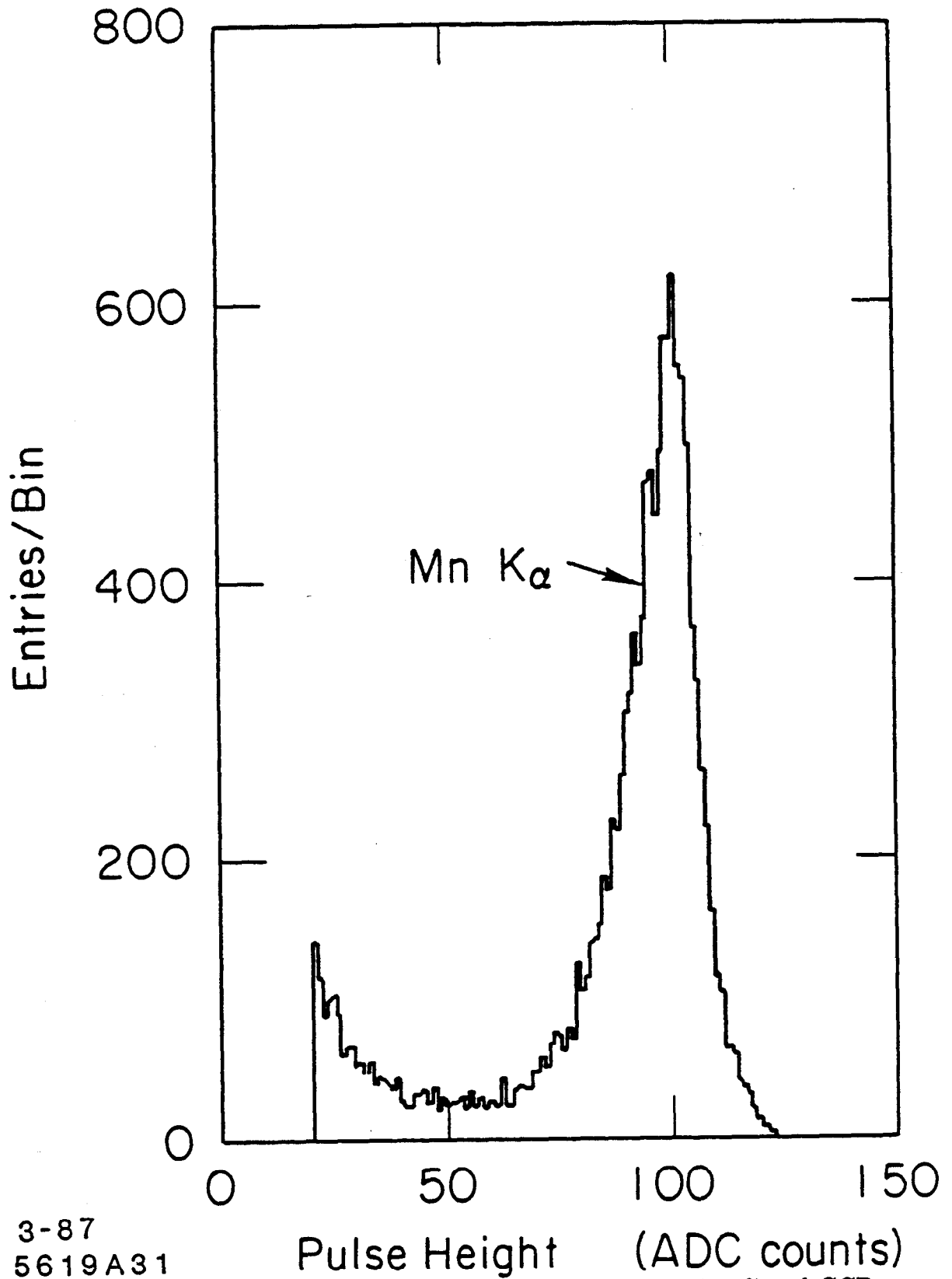

Figure 8.12: A pulse height distribution produced by the irradiated CCD at -30°C exposed to an ^{55}Fe source.

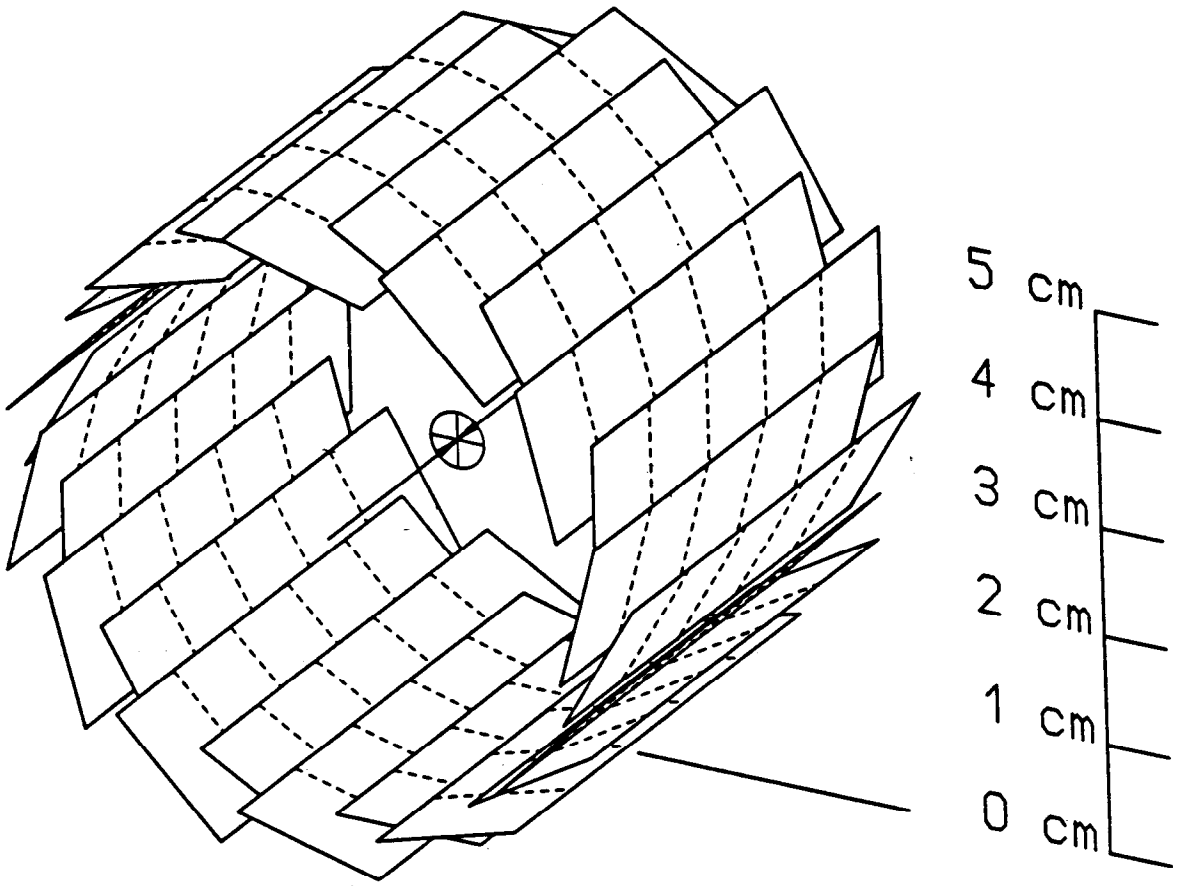

Figure 9.1: A perspective view of 120 CCDs arranged in 24 over-lapping planes surrounding the interaction point. Five CCDs are bonded to each plane and successive planes are staggered along the beam direction to produce complete coverage for $|\cos\theta| \leq 0.7$.

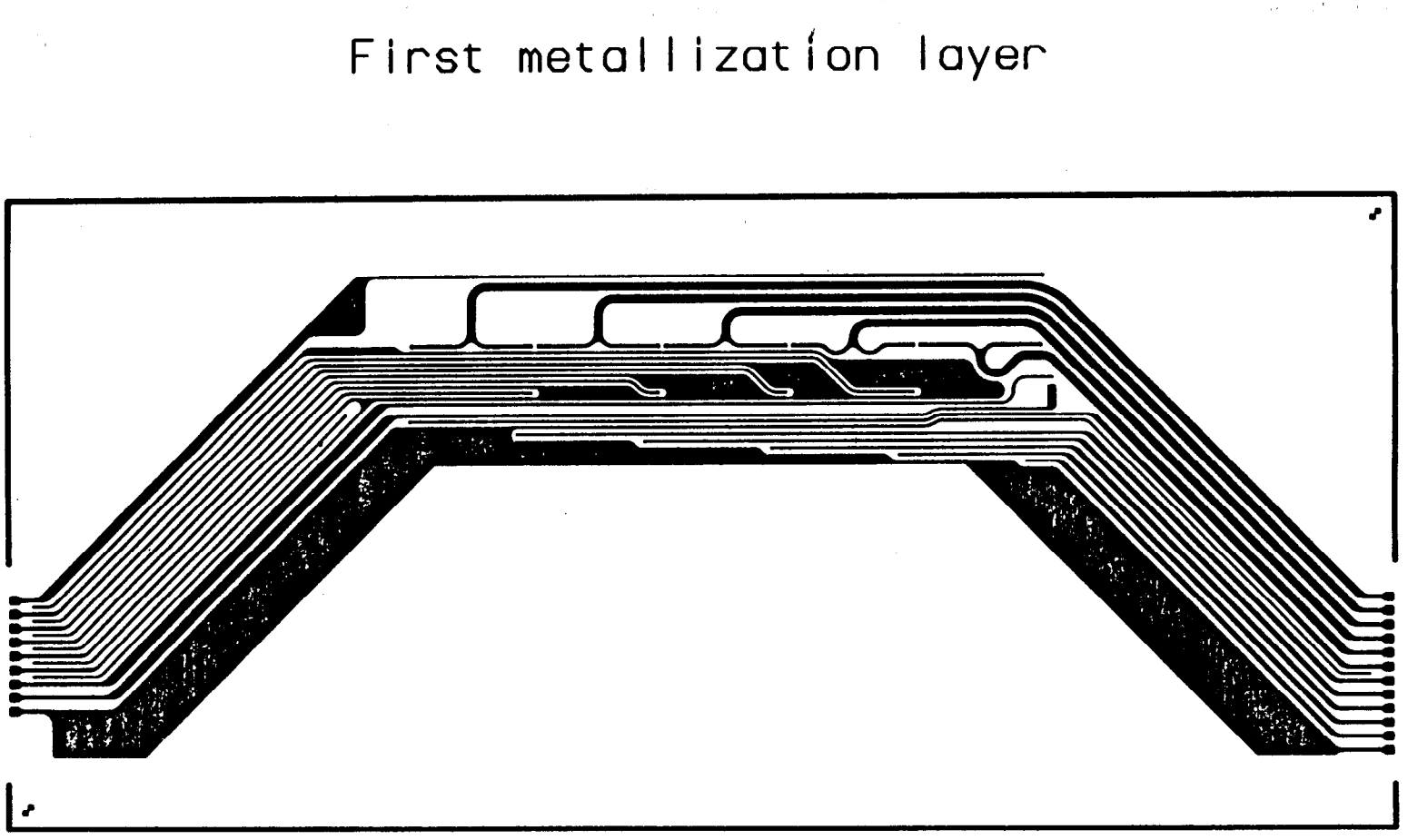

Figure 9.2: The first metallization layer for the ceramic substrate designed to support 5 CCDs. Clock signals are introduced by the traces on the right and signals are removed from the traces on the left.

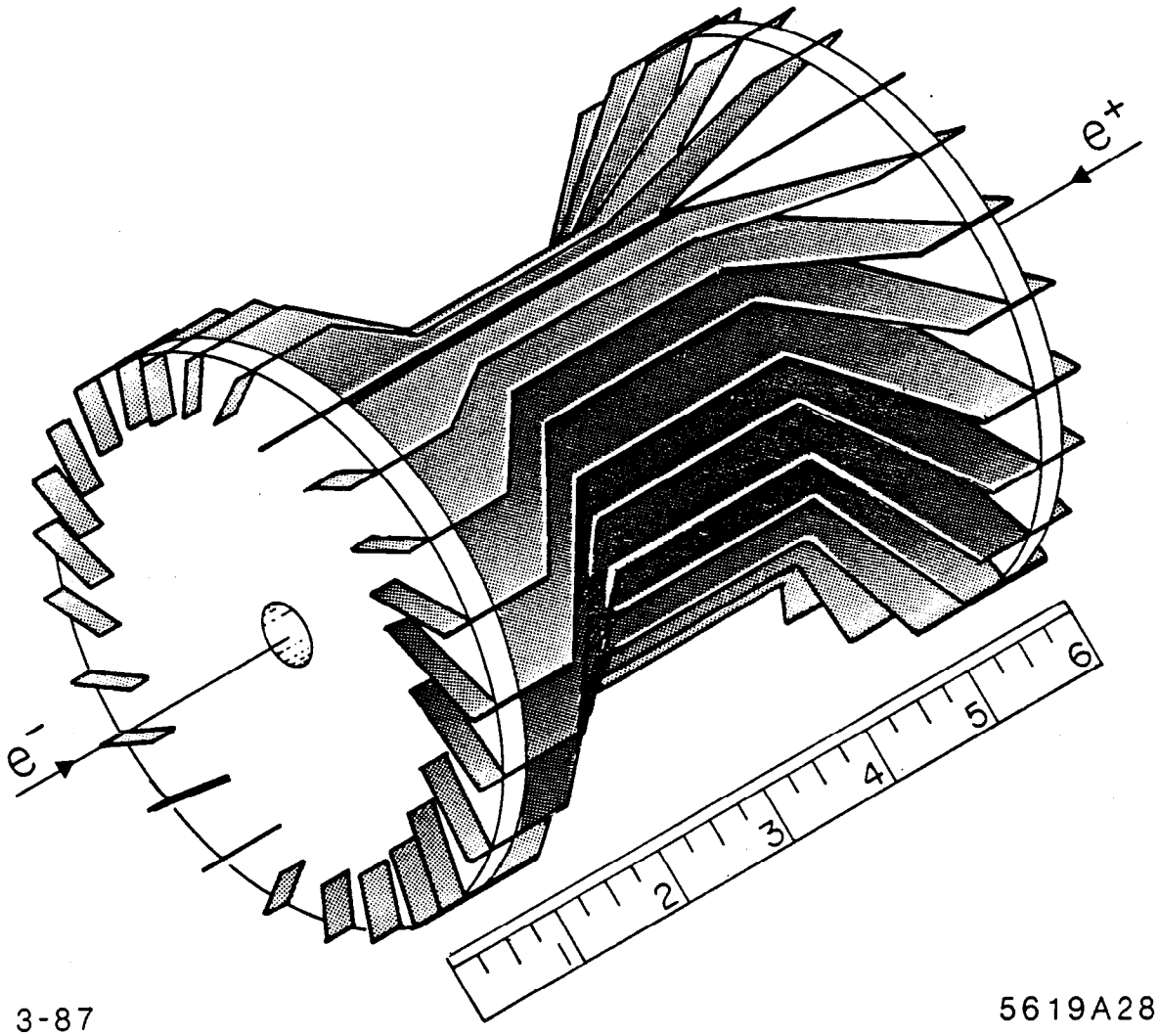

Figure 9.3: Three-dimensional model of the proposed CCD vertex detector structure. Twenty-four ceramic planes support 120 CCDs around the interaction point. The scale is marked in inches.