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OVERVIEW OF THE DATA ACQUISITION ELECTRONICS SYSTEM DESIGN FOR THE SLAC LINEAR COLLIDER DETECTOR (SLD)*

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ABSTRACT

The SLD Detector will contain five major electronics subsystems: Vertex, Drift, Liquid Argon Calorimeter, Cerenkov Ring Imaging, and Warm Iron Calorimeter. To implement the approximately 170,000 channels of electronics, extensive miniaturization and heavy use of multiplexing techniques are required. Design criteria for each subsystem, overall system architecture, and the R & D program are described.

1. INTRODUCTION

The SLAC Linear Collider Detector (SLD) has been approved for construction on a schedule which requires completion by the end of 1988. An R & D program is currently in progress to complete functional prototypes of all critical electronics subassemblies by the middle of 1986. Since the system involves approximately 170,000 electronic channels, and since the radiation environment of the SLAC SLC interaction region will be relatively benign, the opportunity exists to extensively multiplex front-end electronics in order to reduce the cable plant to manageable proportions. This in turn requires extensive use of custom IC and hybrid techniques near the detector elements, which will impose a requirement for extremely high reliability of these circuits.

The overall data collection system will use hardware located very near to the detector magnet; this hardware must contain digitization and memory electronics for each subsystem, intelligent controllers, calibration systems, trigger processors and, at the highest level, data preprocessors. This overall system must collect all raw data on a pulse-by-pulse basis, perform on-line calibration and linearization, and send corrected data to the preprocessors. The beam rate of the machine is a nominal 180 pps, which requires that trigger decisions and data collection be made within times consistent with the 5.6 millisecond beam interaction region.

Fig. 1. Typical Front-End Electronics.

2. BASIC SYSTEM DESIGN PROBLEMS

The photograph of Figure 1 shows the front-end electronics plant for a modern colliding beam experiment with approximately 3800 channels of drift chamber readout, 1600 channels of shower counter, 400 channels of Cerenkov detection, and a fast (scintillator) trigger system, totalling altogether approximately 6000 channels. The SLD detector as currently planned contains approximately 12,000 channels of charge-division drift chamber readout, 40,000 channels of Liquid Argon Calorimetry (LAC) 30,000 channels of Cerenkov Ring Imaging (CRID) readout (very similar requirements to Drift), and close to 90,000 channels of combined strips and pads Warm Iron Calorimeter (WIC) readout, or about 170,000 channels total. In addition, a CCD Vertex detector very close to the beam interaction point will require readout of over 200,000 pixels of data, on each of 240 parallel channels, per event. With conventional readout schemes for Drift, Crid and Calorimetry detection, the resulting cable plant poses extremely difficult packaging problems, and requires a space allocation which could compromise both the physics performance and the maintainability of the system.

Fortunately, SLD has some inherent advantages which potentially simplify the electronics design. One is that it resides in a rather benign radiation environment, so that electronics placed inside the detector should not suffer serious damage. Secondly, it has a very low duty cycle of one beam interaction every 5.6 milliseconds, which provides a relatively long time for forming event triggers, acquiring the raw data and making on-line corrections. These two factors, combined with the potential problems of a massive cable plant, have caused us to consider system designs in which data not only are preamplified close to the detector element, but, going a step further, also are captured in analog storage custom integrated circuits and multiplexed in large groups of channels onto parallel analog data buses which go a short distance to data acquisition modules in crates located on the outside of the magnet iron. With such schemes, the cable plant is reduced by factors of 64 or more, the reduction

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depending upon the amount of data which can be multiplexed in a given time; and the usual multichannel front end data modules become channel-oriented back-end digitizer-memory modules, each channel of which contains logic for selecting, correcting and correlating the event data.

Besides simplifying the cable plant enormously, this approach reduces the size of the data acquisition hardware (number of crates). The disadvantage of this approach is that much more complexity is introduced into the front-end circuits themselves, posing potential problems of reliability, accessibility, testability, and thermal management. To meet these challenges, heavy reliance is being placed upon custom integrated circuits and hybrid packaging techniques. Some specific implementations will be described.

3. SYSTEM DESIGN

The SLD electronics overall system is shown in Fig. 2. The system architecture is a simple tree structure based on the FASTBUS standard data bus, with a major branch (FASTBUS Segment) dedicated to each subsystem. The major subsystems as mentioned earlier are the Vertex, Drift, Cerenkov Ring Imaging, Liquid Argon Calorimeter, and Warm Iron Calorimeter detectors (referred to as Vertex, DC, CRID, LAC, and WIC respectively). The physics parameters of these detectors are described in the SLD Design Report (1), and in other papers in this conference (2-11); the present paper will concentrate on the electronics system specifications and organization as derived from the stated physics requirements of the various detector subsystems. Each Detector subsystem is being designed by a large physics Collaboration involving several institutions. The Electronics effort, being coordinated through SLAC, involves major contributions from several other Institutions such as Rutherford Laboratory, Frascati/Pisa, MIT, and University of Illinois. The Electronics specifications for each subsystem were derived by each subsystem Collaboration group, in some cases working with an associated engineering group.

4. SUBSYSTEM CONCEPTUAL DESIGNS

A. VERTEX DETECTOR

The Vertex Detector, designed to detect tracks within about 10 mm of the beam interaction point, consists of a custom CCD barrel and endcap structure containing 240 CCD's, each comprising about 220,000 pixels or tracking elements of 22μm $\times$ 22μm area. The CCD's are arranged to be read out by parallel paths of high speed analog readout. The detector configuration and electronics channel block diagram are depicted in Fig. 3. A brief functional description of the electronics is as follows (12):

> "The signals first pass through a linear gate which is closed when the CCD's are being clocked in order to protect the sensitive downstream electronics from relatively massive clock feed-through pulses. Without this, there is an inevitable recovery time of some hundreds of nanoseconds. To average and process the signals, the main amplifier and sub-sampler split the signal into four with 5 ns relative delays between each. These signals are combined in the linear fan-in, together with a dc level which provides the control on the sample levels to be taken by the ADC. The flash ADC takes 4 samples at

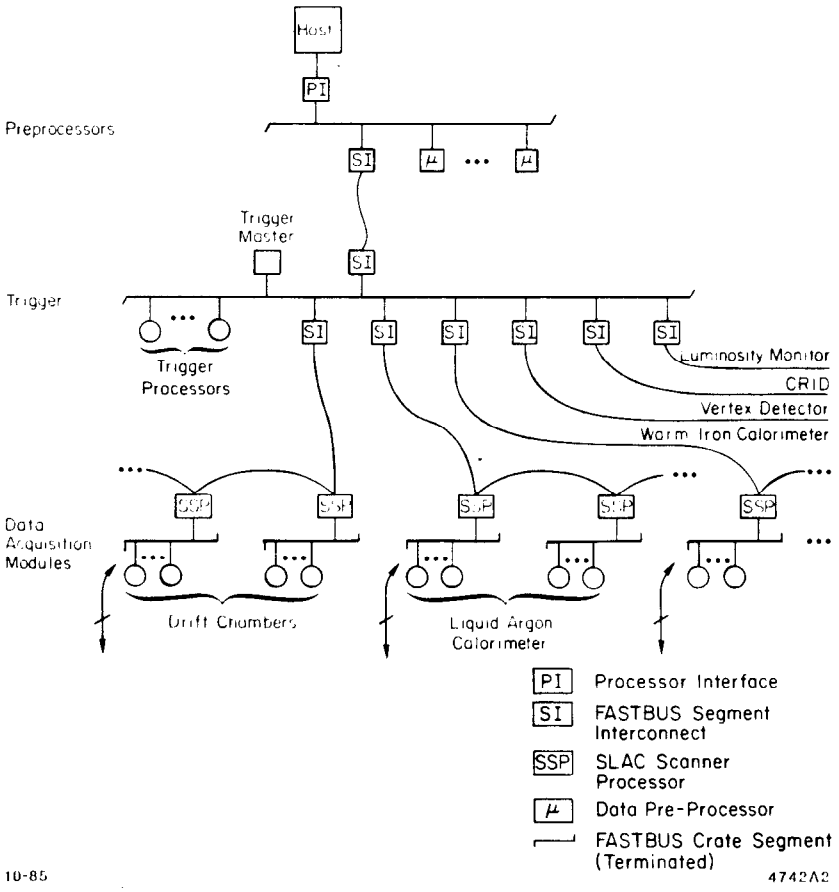
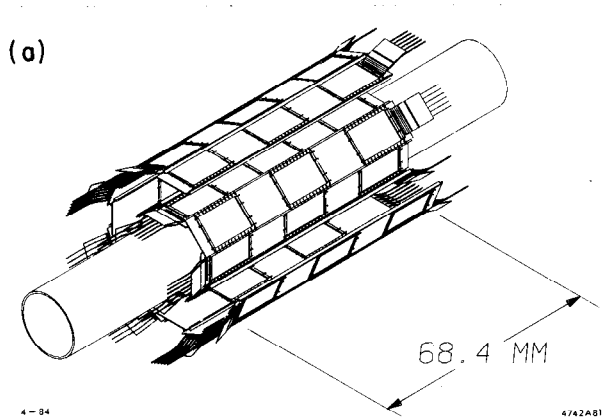


Fig. 2. Overall System.

20-ns intervals (effectively 16 samples at 5-ns intervals due to the effect of the sub-sampler). The correlated sampler sums the 4 samples corresponding to each pixel in turn and subtracts the result from the previous sum. It then feeds out the difference to the Thresholding. Clustering and Memory logic module (TCM module). This will be a pipelined processor working on several rows of data in a fast memory while the next few rows are being read into a second fast memory. This flexible module allows clusters to be defined, the cluster pulse height to be determined, and thresholds (lower and upper) to be imposed on the cluster or on individual pixels. When the pixels which are contained within accepted clusters are recognized, the pixel address (CCD number, parallel register number and serial register number) is associated with the pixel pulse height (6 bytes in total) and sent to the data acquisition memory."

The Vertex detector poses special packaging, thermal management, and clock drive problems. The high currents required by the 10 MHz clock signals dictate striplines of 4 Ω characteristic impedance. Thermal considerations are especially important because each pixel represents a spatial area of only 22μm on a side, and thermal expansion must be tightly controlled.

Aside from the highly specialized CCD detector itself, all circuitry will be packaged in FASTBUS modular hardware. A total of 7 crates is currently planned.



B. Drift Chamber

1. General

The Drift Chamber also consists of a barrel and two end-cap structures, both utilizing the 8-sense-wire cell configuration shown in Fig. 4(a)(1). The plan is to perform charge division readout on each of the sense wires, which requires a total of 11,648 electronics channels. The basic readout scheme is depicted in Fig. 4(b), which shows a sampled data approach; this enables both timing, including multi-hit events, and Z-position, to be derived from the same sampling measurement. A slow drift velocity gas is used such that the overall drift time of 3 μsec results in a spatial resolution of under 100 μm, assuming a time resolution of the pulse leading edge of $\sim$ 8 nsec (one sampling interval). The data from the entire 3 μsec drift period are sampled at about 8 nsec intervals and stored in custom analog chips known as AMU's (10, 13, 14); each channel of drift has a capacity for 512 analog samples (2-256 cell AMU's per channel). After sampling, the event trigger patterns are examined and, if acceptable, the data are digitized and calibrated within the associated data acquisition module.

The AMU has on-chip readout multiplexing so that a number of units can be easily combined on the same analog output bus. Because of the complexity of providing write and clock strobes to the AMU, it was decided to design a 16-chip hybrid with on-board write circuitry (Fig.5); this hybrid can be configured as 8 channels by 512 samples, or 16 channels by 256 samples (10). The unit shown in Fig. 5 serves one 8-sense-wire cell of the drift chamber (or potentially, 16 channels of CRID readout).

The AMU hybrid approach has two main advantages: low cost and high speed, compared with flash ADC's. The hybrid shown, since the write cycle is interleaved, can operate comfortably at 360 MS/s, limited by the speed of the on-board write shift registers. The projected packaged cost is \$ 10/AMU, or \$20 per Drift Channel.

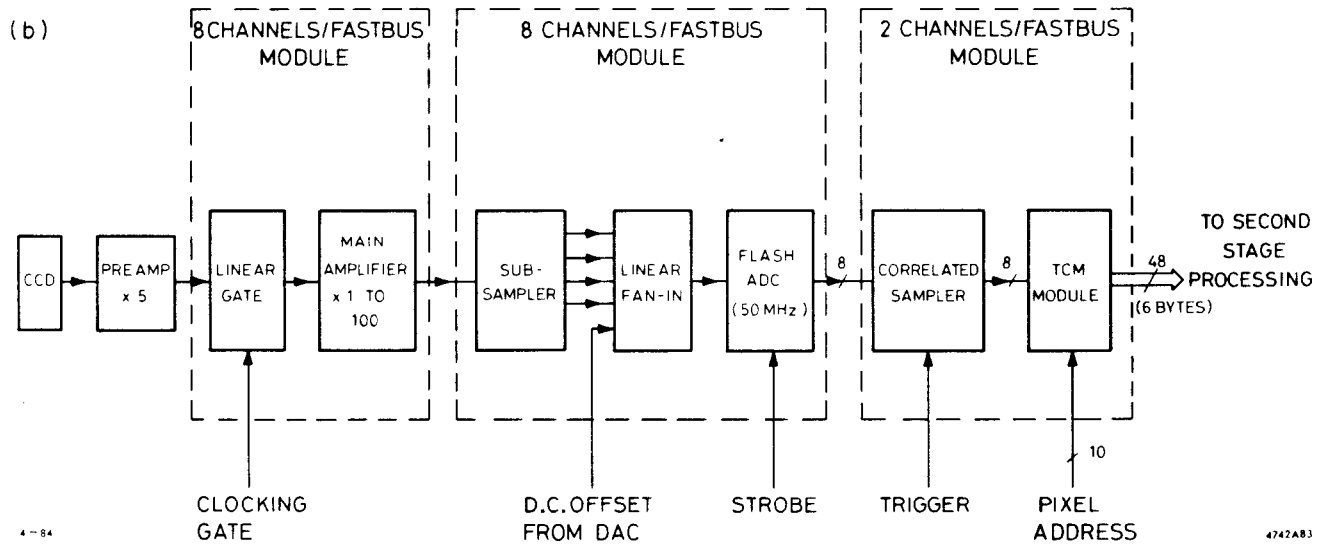


Fig. 3. (a) and (b) Vertex Detector Configuration and Electronics Channel Block Diagram.

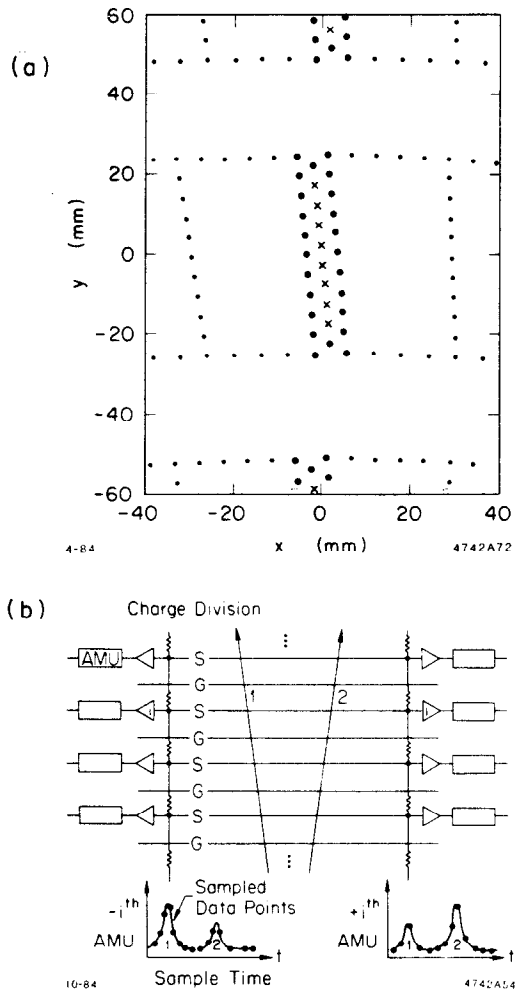


Fig. 4. (a) and (b) Sense Wire Configuration and Basic Readout Scheme.

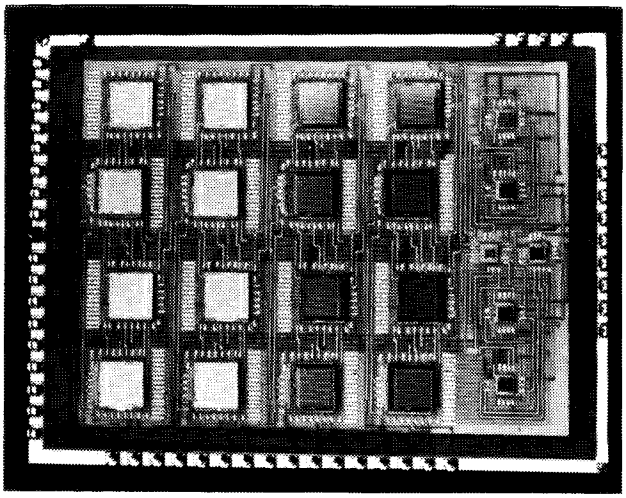


Fig. 5. 16-Chip AMU Hybrid.

2. Packaging and Power Considerations

In order to make use of the multiplexing potential of the AMU, it is necessary to place the devices as close as possible to the preamplifiers, and to minimize package sizes and the number of interconnections. The current plan is to package the preamplifiers, together with calibration and trigger recognition circuitry, in an 8-channel hybrid placed in close proximity to an 8-channel AMU hybrid. All support signals such as power, fast and slow clocks, calibration reference levels, etc. are to be routed on high density multilayer printed circuit boards. Careful shielding of the front ends of the preamplifiers from random noise and clock line pickup will be challenging. The basic channel circuit and proposed front end packaging scheme are shown in Fig. 6 (a) and (b).

The front-end packaging must be very compact, because of the limited volume available. The endplate of the barrel drift chamber is shown schematically in Fig. 7; this illustrates the proposed segmentation of motherboards and subdivision of channel readout by layer, modulo 64 channels (8 major cells $\times$ 8 wires/cell). The output of each group of 64 channels is proposed to be read out over an analog fiber optic link to a digitizing module, the block diagram of which is shown in Fig. 6(a). When the barrel and endcap digitizing requirements are totalled, only 3 FASTBUS crates are needed (2 for the barrel, 1 for both endcaps).

In addition to the above problems of packaging and shielding, thermal problems have to be controlled. The front-end circuit described above dissipates about 1 watt per channel; this can be reduced by a large factor by pulsing the power in synchronism with the beam collisions, and applying power for readout only when the event trigger is positive. This reduces the average duty cycle to about 50 msec per one second, a 20:1 average power reduction.

3. Circuit Considerations

The preamplifier hybrid will contain a fast, low noise preamplifier section, a pattern latch and strobe for calibration, and a discriminator/latch to read out the trigger pattern; it is proposed that the latter be read out also over the analog fiber-optic link.

The AMU hybrid poses complexities of writing, reading, and calibration of nonlinearities and offsets. Many detailed studies of accuracy, dynamic range and calibration indicate that the required accuracy of approximately 8 bits over a range of at least 10 bits, can be met.

Analog transmission by fiber optics is desirable to minimize pickup and ground loop noise problems; however, the active link also has linearity and stability problems which must be mastered. Developments to date indicate that these problems can be controlled; and although the cost of a single link is high, the per-channel cost is easily comparable to that of a single cable per channel in a non-multiplexed scheme. It should also be noted that a conventional analog cable link is a fallback position, in case unsuspected problems with the fiber optic links should arise.

C. Cerenkov Ring Imaging Detector (CRID)

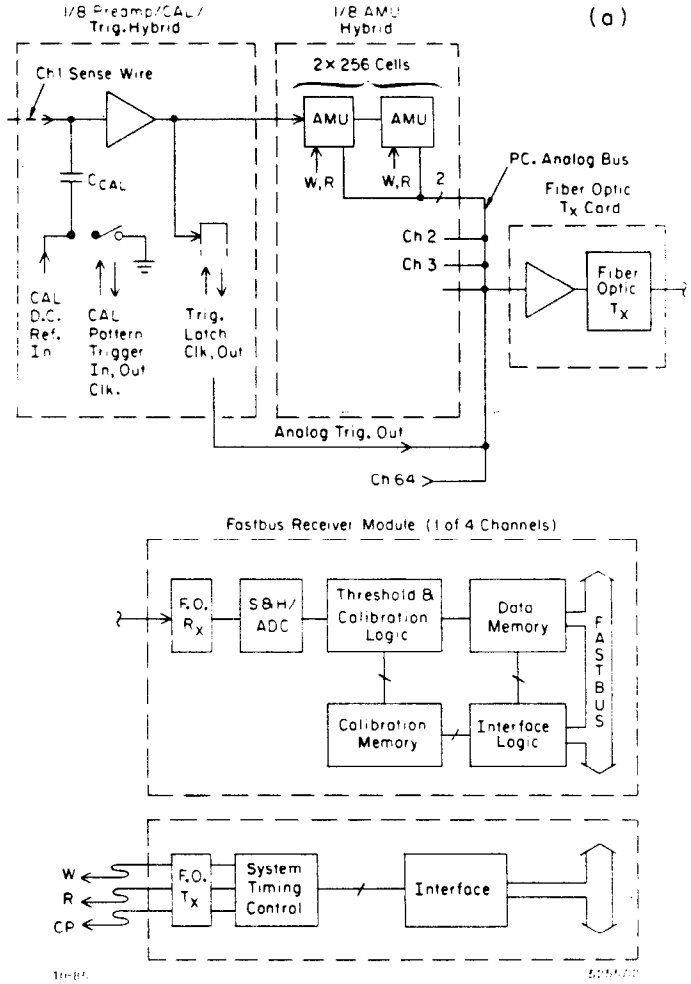
1. General

The planned arrangement for the CRID is similar to that just described for Drift, with the following exceptions:

a) The preamplifiers will be separated from the AMU's by a short distance due to long-term inaccessibility of the CRID front end circuits.

b) Each CRID channel needs only one AMU of 256 samples each; therefore multiplexing will be performed modulo 128 (c.f. 64) channels, and further economies at the FASTBUS module level will be realized.

Note that preamplification and shaping requirements are different from Drift because the pulses are much slower; the AMU



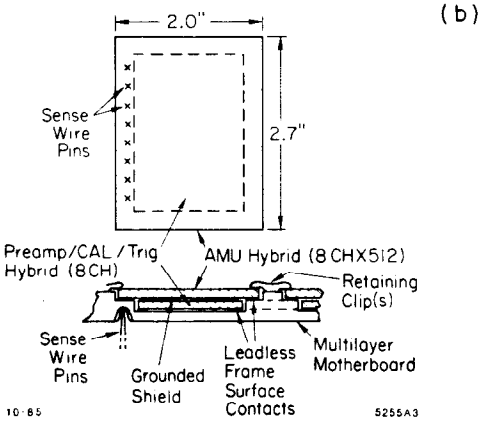


Fig. 6. (a) and (b) Drift Chamber Channel Block Diagram, Proposed Packaging Scheme.

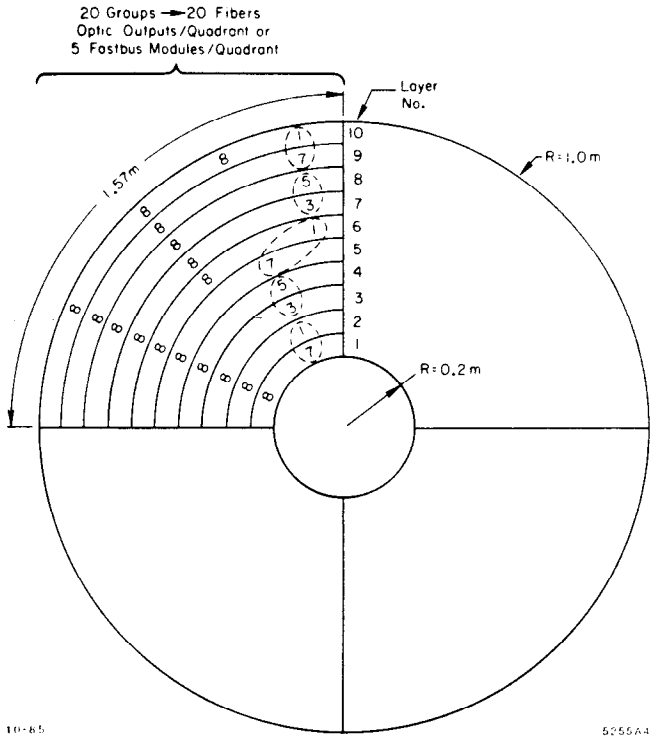


Fig. 7. Drift Chamber Barrel End Plate.

write clock speed will be adjusted accordingly. With these restrictions, the same FASTBUS analog data receiver already described can be used.

Detailed circuit designs for CRID have not yet been undertaken. Extensive experimental work using commercially available preamplifiers and data collection modules is in progress.

D. Liquid Argon Calorimeter (LAC)

1. General

The data handling requirements for the LAC channels are well understood from past experiments: Low noise charge-sensitive preamplifier of about 0.5 $nV/\sqrt{Hz}$ sensitivity, followed by a shaping section, matched to a single-point sampling circuit with 13-bits dynamic range, and including the necessary calibration reference and control circuits. The circuit block diagram is shown in Fig. 8.

The key design feature again is the heavy use of front-end multiplexing, in this case modulo 256 channels, to reduce the cable plant by this factor; the limit of multiplexing is dictated by the maximum time allowable to form the calorimetry total energy trigger. To this end, another custom integrated circuit has been developed (11), called the CDU (Calorimetry Data Unit); this is a 32-input, 4 bucket-per-channel analog storage device similar to the AMU, but with the design optimized for dynamic range as opposed to sampling speed. The purpose of

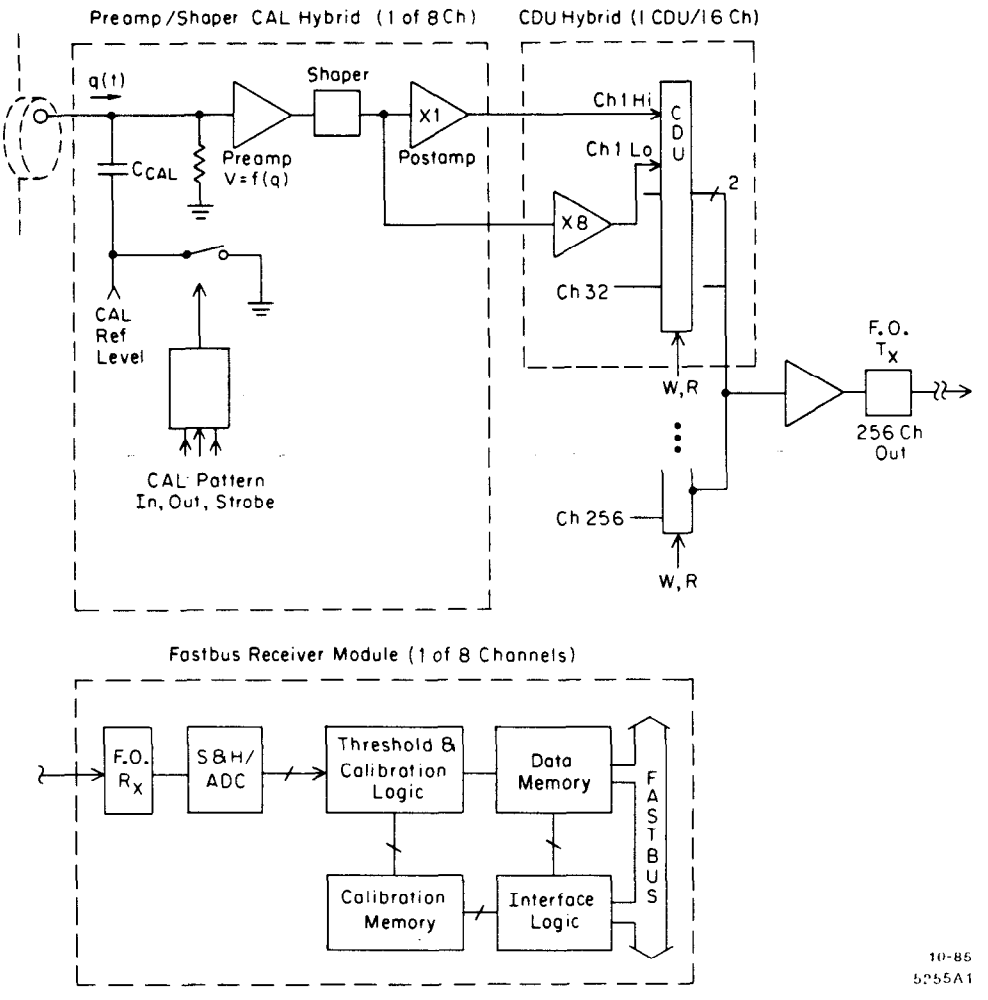


Fig. 8. LAC Circuit Block Diagram.

the extra buckets is to allow the possibility of multiple point sampling, for example to measure shifts in the baseline due to low frequency noise or transients.

2. Circuit and Packaging Considerations

Packaging within the LAC also poses serious problems. Detector elements from the cryogenically cooled and vacuum enclosures are connected via a bulkhead with circular multi-pin high density connectors. Each group of channels must be amplified and sampled locally, then multiplexed via an analog fiber optic (or conventional cable) link.

Figures 9(a) and (b) shows the proposed front end packaging for 32 channels and for an entire bulkhead of 18 × 32 channels. To achieve such high packaging density requires essentially that all circuits be hybridized; and that power, ground, clock signals and analog output bussing and buffering be routed via a multilayer motherboard and/or via the bulkhead connectors themselves. The details of grounding and shielding within such structures will be challenging if the required 13-bit dynamic range is to be achieved, (Note that to achieve the 13-bit range, a hi-lo channel configuration has been assumed; in fact, this may not be necessary, as the prototype CDU chip appears to have very close to a 13 bit range. The dual range scheme would guarantee at least 14-bit dynamic range).

Multiplexing modulo 256, and assuming an 8-channel FASTBUS receiver module, reduces the cable plant to about 150 cables (optical fibers), which offers a tremendous reduction in space, complexity, and cost. The FASTBUS data acquisition section, assuming 8 receiver channels and digital conversion and memory sections per module, can be handled in a single crate (compared with the original estimate of 32 crates in the non-multiplexed mode).

3. Calibration Considerations

The calibration circuit requirements as regards accuracy and range are similar to that of the Drift system, operating in the charge-division mode. Again, it is planned to include a pattern latch and gate in the front end hybrids so, in fact, any desired calibration patterns can be generated; the range is controlled in the usual way by a precise digital-to-analog converter (DAC) generated voltage applied to all calibration capacitors simultaneously.

It is planned to laser-trim the hybrids in order to match all calibration circuits, at a given temperature, to an external reference capacitor (standard charge). Amplifier gains will be similarly matched. Once the circuits are in place, changes can be tracked over time by monitoring a history of responses for each channel for both calibration and data inputs.

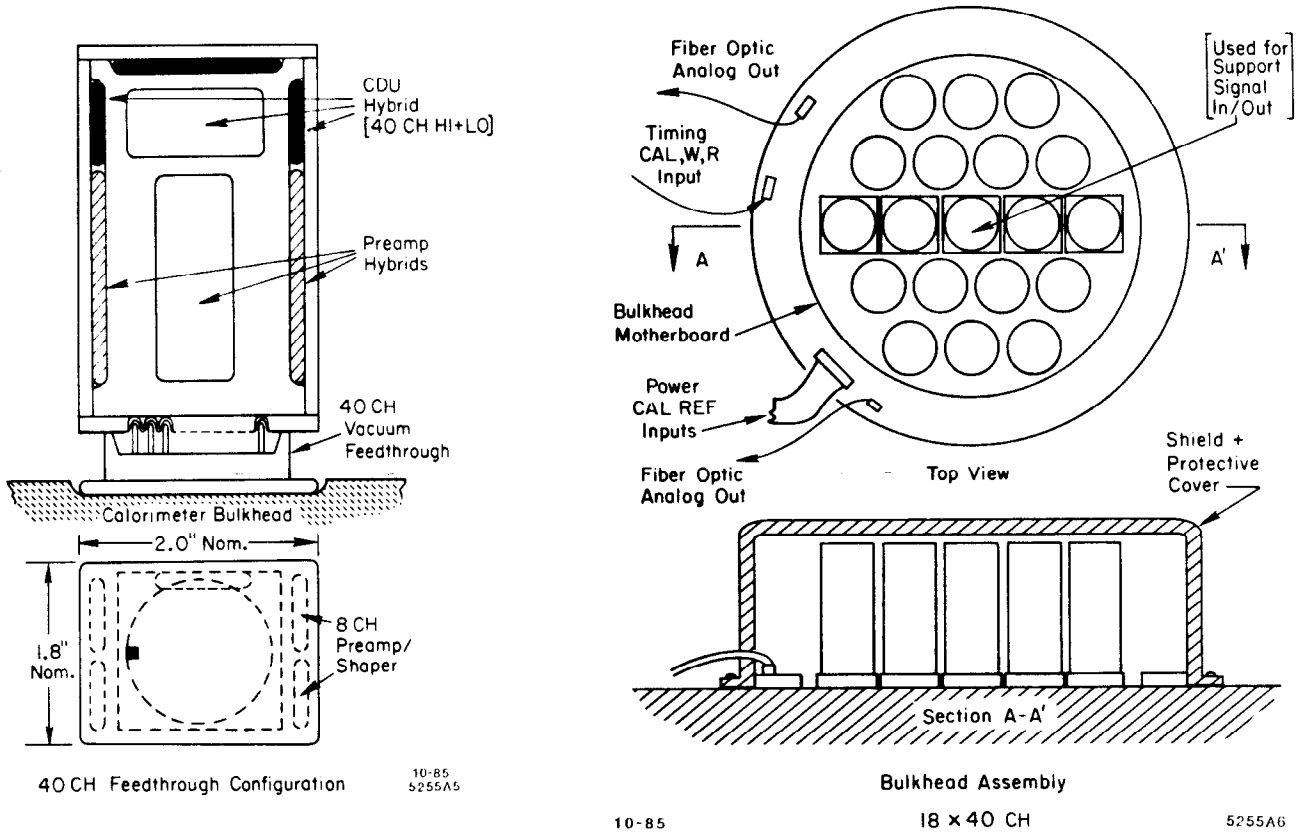


Fig. 9. (a) and (b) LAC Proposed Front End Packaging; Bulkhead Assembly.

4. Power Dissipation

Front-end power, as in the case of Drift, will be pulsed to reduce dissipation. The pulse duty cycle will be similar to Drift, which projects about a 20:1 reduction from dc conditions.

E. Warm Iron Calorimeter (WIC)

1. General

The WIC is a very large structure with relatively easy spatial access for electronics, although the construction of the detector elements themselves is quite complex. The WIC has two parts, pads and strips. Signals from both are large and easy to detect. Pads are connected together in a projective tower geometry (as in the LAC) and summed into a charge-sensitive (integrating) preamplifier; from this point forward, it is planned to utilize exactly the same multiplexing strategy (including the CDU) as for the LAC. The 4,421 pads channels can be processed in about 3 of the 8-channel FASTBUS receiver modules.

The strips readout is a conventional discriminator-shift register latch which will use an Italian custom integrated circuit (15). Since there are 88,000 strips to be read, these will be coupled in large serial strips, e.g. modulo 1024 or possibly greater, and sent to multichannel receiver modules, just a few of which will suffice for the entire system, since the total memory requirements are relatively trivial compared with the other detector subsystems.

5. SPECIAL SYSTEM PROBLEMS AND FEATURES

A. AMU Channel Calibration

The typical AMU channel carries an enormous amount of data. The current plan is to calibrate the AMU using 8 constants for each cell of each AMU. This requires selective data filtering, and fast on-line correction, in order to keep the correction processing time from impacting the overall event trigger dead time. Secondly, it is necessary to calibrate preamplifier nonlinearities via the front-end calibration circuits, and fold these two calibrations to arrive at the final channel correction constants. All of this will obviously require processor intelligence within each data receiver module, in order to maintain the data collection speed of the overall system.

B. Scanner-Processor (SSP)

Each crate will contain an SSP (16) which is a FASTBUS 32 bit 2901-based controller containing a Segment Interconnect (SI) capability; the SSP will assist with routine global calibrations, and will collect and format data (all SSP's operating as parallel processors) prior to transmitting its data block to the track-finding pre-processors and/or the host.

It appears at this time that the SSP will also be able to serve as the Trigger Processor.

C. Trigger Generation

Primary triggers require pattern data from the Drift Chamber, and Energy sums from the LAC and WIC pads; therefore these data must be acquired in under 1-2 milliseconds. It is planned to shift trigger patterns from the Drift system via the analog channel, modulo 64, which will take a nominal 64 μsec. The LAC energy sum will be derived modulo 256 in each receiver module, thence transmitted via FASTBUS to the Trigger Processor. If the energy sum data has to be corrected "on the fly", then correction algorithms will have to be executed within each LAC receiver module, as for the Drift system.

D. PRE-PROCESSORS

The pre-processing section is presumed to be a set of powerful FASTBUS processors based on the Micro VAX II chip set. This is expected to be a commercially-available product. Approximately 20 such processors, or the equivalent, are needed to perform the on-line track reconstruction, or software trigger, for the system.

6. PROGRESS TO DATE

Current work is emphasizing finalization of detector element prototypes, completion of circuit, hybrid and custom VLSI designs, and system front-end packaging prototypes. Front end amplification, shaping and protection circuits are still being finalized. Once finalized, demonstration hybrids will be built, and production of this design or an equivalent tendered for Commercial bid.

The first quantity order of 22,000 AMU chips has been recently completed. The prototype CDU chips have been successfully tested. CAMAC AMU test modules have been built, and have been tested on the drift chamber in the Test Beam Facility.

CRID charge division is being tested with standard available circuits; no special CRID circuits have yet been built. Prototype work on the WIC pads front end is in progress at MIT.

A fiber optics analog link, using a linearity compensation scheme, has been successfully demonstrated, with excellent linearity and dynamic range. Further fiber optic studies aimed at wideband fast clock transmission are underway.

Most of the details of various electronics developments are covered in the other papers cited in the references, many of which are being presented at this Conference.

7. CONCLUSION

The SLD Detector electronics will require a number of new developments to realize the goals set forth in the conceptual design, in particular hybrid and custom chip techniques, and high density hardware mounted very close to the detector elements. Basic feasibility has been demonstrated for most of the hybrid techniques; the project is now moving toward a critical demonstration of subsystem performance, packaging feasibility, and reliability consistent with the difficulties of access to the circuits which are to be locked up inside the detector for long periods of time.

ACKNOWLEDGEMENT

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