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PERFORMANCE REPORT FOR STANFORD/SLAC MULTI-CHANNEL SAMPLE-AND-HOLD DEVICE*

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ABSTRACT

Test results on a newly developed Multi-Channel Sample-And-Hold Calorimeter Data Unit (CDU) are presented. The device is organized as 32 input channels, each consisting of four storage cells to take samples of the 32 analog signals at four separate times. The design goals for the development were wide dynamic range and long hold times. Therefore, each storage cell is laid out in a fully differential way and consists of a sampling stage for the signal and another identical stage for a reference voltage. Results on the performance of the device are described.

1. INTRODUCTION

In High Energy Physics Instrumentation the trend over several decades has been towards the accumulation of more and more complete information about more and more complex physical events. More recently this trend has accelerated to such an extent that even the spectacular improvements in general purpose electronic devices do not suffice anymore, and devices need to be custom developed to satisfy the huge data handling requirements of the field.

This paper describes the third in a series of monolithic devices developed in collaboration between SLAC and the Center for Integrated Systems of Stanford University. The first device, the Microplex Unit[1] incorporates low noise amplifiers in addition to analog storage. The second and third devices are fast analog storage devices. The second micro chip, the Analog Memory Unit[2,3,4], is optimized to achieve good timing resolution, and the Calorimeter Data Unit (CDU) described here is specialized for high volume storage and retrieval of analog information at the greatest possible accuracy (>12 bits) at high signal bandwidth (approx. 30 MHz).

The CDU is implemented using the HMOS-I VLSI[5] process with a minimum feature of 3 μ. The primary line width is 5 μ.

2. OPERATION DESCRIPTION OF THE CDU DEVICE

The CDU sample-and-hold device is a multi-channel array of sample-and-hold cells for analog signal memory applications. This integrated circuit provides 32 parallel inputs for analog signals, and the capability of taking samples on these channels at 4 separate times. All of the sample values are retained in MOS capacitors on the chip, and can be read out serially to a analog-to-digital converter (ADC). Special care has been taken in the IC design to minimize error from the sampling process and following stages, and to provide a maximum signal-to-noise capability.

Figure 1 shows the diagram of a single storage cell for an analog sample. The main inputs to the storage cell are the analog signal input and the write clock ϕ_w. While the write clock is high, the signal input is connected through Q1 to the storage capacitor C1, and the reference input through Q8 to the storage capacitor C2. The nodal time constant at the capacitors is approximately 5 ns. With the falling edge of ϕ_w, Q1 and Q8 are turned off and the most recent values of the signals are held on the capacitors. Since both the signal and reference inputs are sampled at the same time, offsets due to gate overlap capacitance, charge pumping, and input common mode noise are cancelled. The signal and reference samples receive identical amplification and gating in the remainder of the device, therefore only one path will be described.

The signal voltage stored on C1 is buffered by voltage follower Q3 to isolate it from charge sharing effects, which the following signal multiplexer stages could cause. A constant sink current for biasing Q3 is provided by Q4 to keep Q3 always at the same operation point. This bias voltage is generated by Q15 and Q16, which have a geometry and layout identical to Q3 and Q4. Changes in the fabrication process which affect the transistor conduction characteristics will have a compensating effect on the bias generator, so that the proper bias current for the source followers is automatically generated. The output of Q3 is connected to a second source follower Q5, which provides the actual signal current read out of the chip when this cell is addressed. Transmission gate Q6 connects the cell to the row bus, which is routed to the output by Q7.

The chip can be read out in a voltage or a current mode. Current output is obtained by loading the outputs with a virtual ground at the signal and reference output terminals, taking the difference of the two output currents, and passing the result through a load resistor. Voltage output is obtained by connecting the signal and reference outputs to a negative supply through a resistor to produce a source current of about 1 mA, and measuring the output voltage difference directly. In this case, the transistors Q5 and Q12 function as voltage followers. Current output gives a faster transient response when each new cell is selected for readout, and seems to give better transfer curve linearity.

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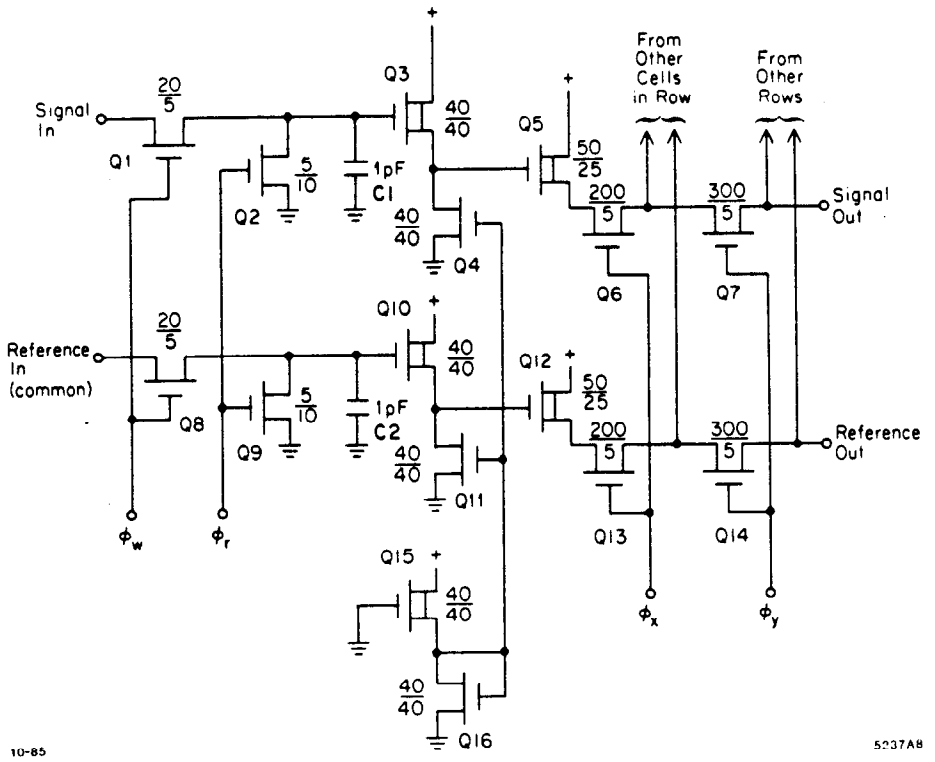

Fig. 1. One storage cell. Transistor size W/L (microns); depletion transistors are marked with a bar.

The column clock ϕ_x and the row clock ϕ_y for addressing the cells are derived from shift registers. Each row consists of 8 cells (two channels with four cells each), so that readout is organized in an array of 16 × 8 cells. This permits the placing of 16 signal input connections on each side of the physical chip axis for easier packaging.

Each sampling cell is fully differential to obtain first order compensation of voltage offsets, resistive drops, sampling transients, and selection losses. The chip is designed to be as large as possible within reasonable fabrication constraints and giving due consideration to the process defect rates. This allows the MOS transistors serving as amplifiers or voltage followers to be made large for suppression of their 1/f noise, despite the fact that devices are nowadays pushed to ever smaller dimensions. The sizes are chosen to permit attainment of a RMS noise level of 1 part in 4096 or smaller, so that a 12 bit resolution could be obtained on a single shot measurement. Also, the series pass transistors used for the output multiplexer are rather large to minimize their total resistance, thereby reducing the error component caused by their nonlinearity with signal level and current. Figure 2 illustrates the physical layout of the cell.

Figure 3 shows the arrangement of four sampling cells for one input channel. The signal inputs are connected together as well as the reference inputs, the reset inputs, and the outputs. Note that in this drawing, the ϕ_x driven transmission gates of Fig. 1 are part of the cell, while the ϕ_y gates are common to a group of 8 cells. Each sampling cell uses a different one of the ϕ_{1w} through ϕ_{4w} clocks. When one of these control pulses is high, it enables the input voltage to be stored on the corresponding capacitor in each channel.

A general block diagram of the chip appears in Fig. 4, showing the major subsections. The 32 parallel analog inputs enter

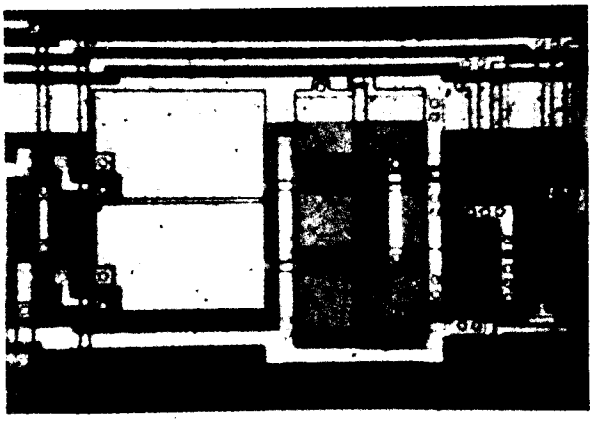

Fig. 2. Storage cell layout.

the 32 by 4 array of sample-and-hold cells at the left. Four sample control pulses, labelled ϕ_{1w} through ϕ_{4w} enter this block at the top left. The stored information is read out as an amplitude modulated serial pulse train. This is done with a set of shift registers, configured to produce two dimensional scanning of the matrix of storage capacitors. The shift registers are internally connected so that only a single set of 128 non-overlapping clock pulses (ϕ_{1R}, ϕ_{2R}) is needed to read out the device.

A sample readout sequence is initiated by simultaneously raising both ϕ_{1R} and ϕ_{2R} high. This causes all of the shift register stages to be initialized to a state with their outputs low, or inactive. When the Start input is low during ϕ_{1R}, a logic 1 is shifted into the first stage of both shift registers, permitting the voltage level in the first time bin of channel 0 to be read out. Subsequent pairs of clock pulses ϕ_{1R}, ϕ_{2R} sequence the

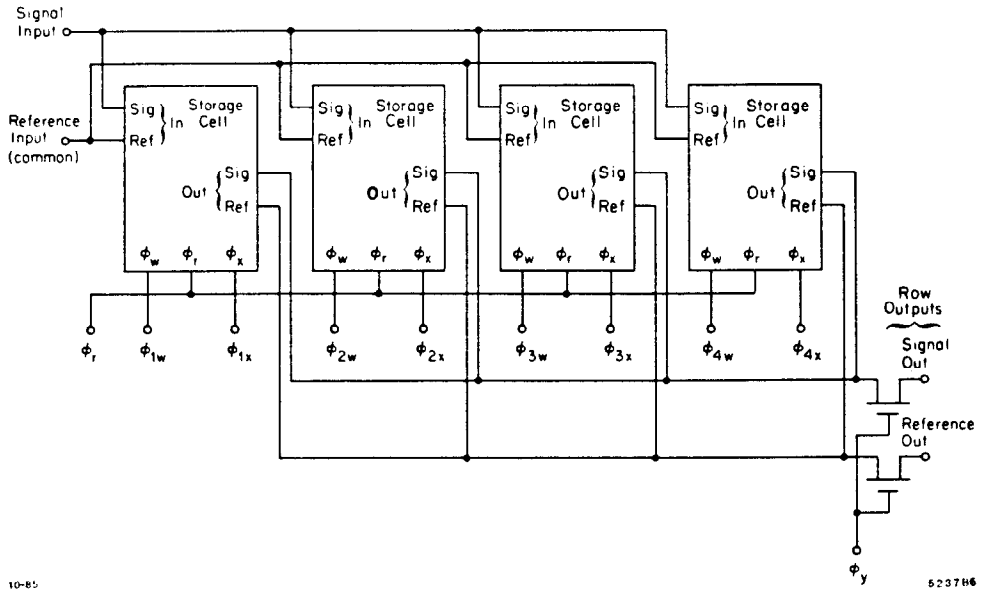

Fig. 3. Organization of 4 storage cells forming a signal channel.

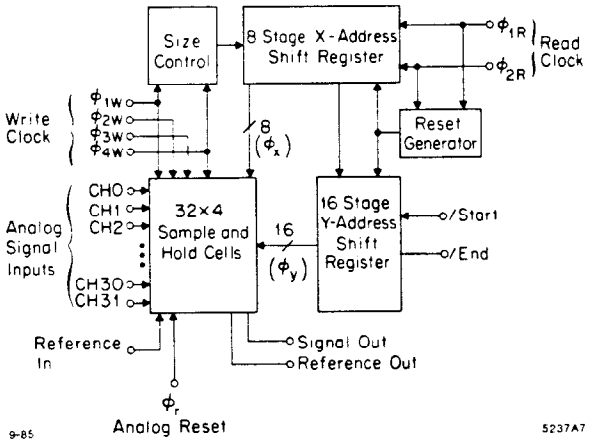

Fig. 4. Functional block diagram of the analog storage chip.

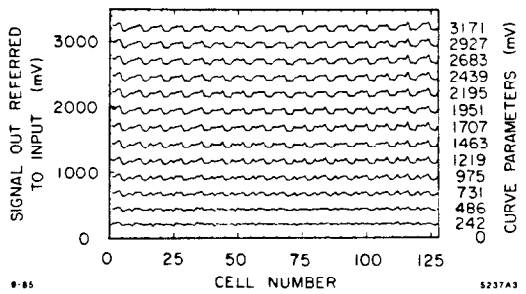

Fig. 5. Cell response to various DC levels at the input (Raw Data).

readout multiplexer through the bins of this channel, and then to channel 1 in turn.

The CDU device provides a choice of writing and reading either four or two analog words per channel. An internal circuit detects the presence or lack of the write pulse ϕ_{4w}, and configures the internal readout shift registers for reading out 4 or 2 time bins per channel, respectively. In the latter case only 64 pairs of clock pulses are needed. The readout process is thus sped up by a factor of two by ignoring the channel bins without data.

When the last cell of the device is addressed, an END signal is generated, which can be used as a START signal for a subsequent CDU chip. The analog outputs of the CDU are in a high impedance state when none of the cells are being addressed by the readout shift registers. Therefore, several chips can be cascaded for serial readout by simply connecting their clock inputs and analog outputs in parallel, and routing the END signal of each chip to the START signal of the following unit. The analog data will be read out as a continuous sequence of analog levels. The primary limitation of this parallel operation is the capacitive loading effects of all the chip outputs, which slow down the output node transient response.

The output signal is usually converted by an ADC. This conversion process can proceed at a moderate pace of approximately 1 MHz, limited primarily by the ADC speed characteristics and transient settling time requirements for the desired accuracy level.

A single master reset pulse to the auxiliary input ϕ_r will cause all record of the sample set to be erased.

3. REPORT ON TESTS AND MEASUREMENTS

Figure 5 shows the response of all 128 cells of one device to various DC levels (curve parameters) at the input. These results are obtained with a sampling gate width of 100 ns. The analog information is read out channel by channel at a rate of 300 kHz. Variations in cell response of approximately five percent are apparent. There is also a regular pattern in the cell response which repeats every eight cells, the origin of which is under investigation. If one considers a group of cells which differ in address by increments of eight, variations in response of less than one percent of full scale are found. The measurements presented here are performed with a substrate voltage of -3 V for the chip. A substrate bias is necessary since measurements reveal a significant drop of the output signal (3% after 2 ms) for small input signals with the substrate

grounded. The CDU device is read out here in a current mode yielding a range of 0.6 to 1.2 mA. The observed rise time of the output signal at the current-to-voltage operational amplifier is 200 ns. A 100 ns rise time of the output signal is obtained by connecting the output of the chip via a 10 kΩ resistor to −6 V. However, with a larger number of CDU devices on a common analog bus the current read out gives shorter risetime over the voltage mode and is thus preferred.

Results after applying a cell by cell pedestal subtraction show only a slight (1%) decrease of the variances in cell to cell response, since the pedestal induced by the sampling gate (W/L = 20/5) is small and most of it is compensated by the reference stage. Upon further analysis a non-uniformity in gain among the cells at the 2% level is found. However, the variances in gain in an eight cell interval are less than 0.1 percent.

The data shown in Fig. 6 are fitted cell by cell to two parameters: offset and gain. Only 12 of the 14 curves are used in the fit. The two-parameter fit yields residuals of 30 to 40 mV. Thus, the transfer curves have a considerable curvature as illustrated in Fig. 7, which is caused by the last voltage-to-current converting FET Q5 (Fig. 1). (Each curve in the figure is shifted with respect to the previous one by 50 mV). It is clear that for a better than 1% accuracy over the 3 V input signal range a S-shaped curvature correction is required. Since a good uniformity of the curves in an eight cell interval

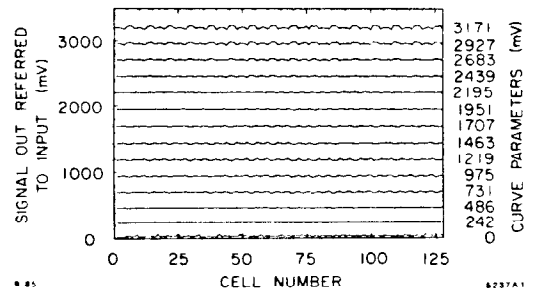

Fig. 6. Same data corrected cell by cell for offset and gain variations.

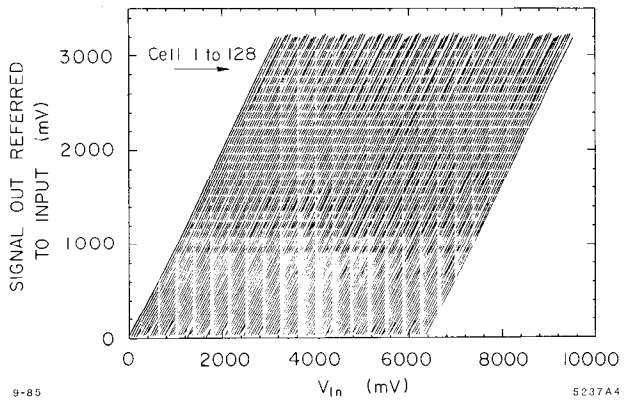

Fig. 7. Transfer characteristics of all 128 cells. (Horizontal scale valid for first curve only. Each subsequent curve shifted to the right by 50 mV.)

is observed, only eight sets of values are needed for correction. Each set is determined by averaging the deviations for a given input voltage obtained by applying a linear fit to each transfer curve in an eight cell interval. The nominal calibration values are modified by these eight sets of correction values. Using the modified values, linear fits are performed for each cell. Table I shows the RMS values (mV) as a function of supply voltage (5 V and 6 V) and input voltage range. Both RMS values before and after the curvature correction are listed. The two parameter fit for an input voltage range of 2.5 V yields RMS values of approximately 10 mV or 0.4% of full range (VDD=5V). The eight set curvature correction improves the ratio to 0.07%, and the accuracy will presumably further increase by applying a cell by cell curvature correction. The RMS values for a supply voltage of 6 V are determined to be 40 mV and 5 mV without and with curvature correction, respectively. (Input voltage range 0 to 3.3 V). The maximum applied input voltage in these measurements is 3.3 V, which is not the upper limit in the case of a 6 V supply voltage for the chip.

Table I. RMS values of residuals in mV with and w/o curvature correction (c.c.) as a function of supply and input voltage.

VDD (V)	Input Range(V)	Residuals w/o c.c. (mV)	Residuals with c.c. (mV)
6	0-2.7	41.7	5.3
6	0-2.9	42.8	5.4
6	0-3.3	43.1	5.5
5	0-2.0	9.3	1.2
5	0-2.2	9.6	1.4
5	0-2.4	9.8	1.6
5	0-2.6	12.9	1.8
5	0-2.9	26.5	2.0
5	0-3.1	51.1	2.1

A supply voltage of 5 V yields a reduced input signal range, but also results in a smaller curvature of output response and smaller cell-to-cell variations compared to 6 V.

The fluctuations of response for repeated samples at the same input level are less than 1 part in 4000 of full scale for both applied supply voltages. Rough crosstalk measurements yield a ratio of 3 to 1000 of full scale, the properties of which will be further investigated.

The power consumption of the analog and digital parts of the device are 30 mW and 70 mW, respectively.

The input capacitance of one channel with one sampling gate conducting is determined to be 6 pF. For each of the four sampling gate inputs a capacitance of 0.6 pF is obtained.

Figure 8 shows the output signal of one cell as a function of signal delay. The RC following time constant of the signal cell at the storage capacitor with one sampling gate conducting is in the range of 5 to 15 ns. Theoretically, the time constant is about 5 ns (Rg≈5 kΩ, C≈1 pF).

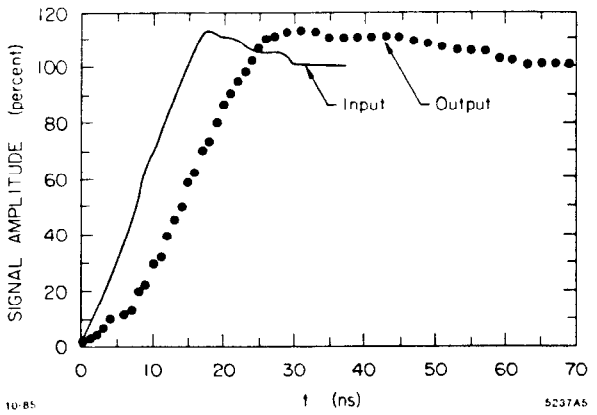

Fig. 8. Output as a function of signal delay.

4. CONCLUSIONS

The Sample-and-Hold device described in this paper shows excellent performance for high speed, high accuracy analog data storage. The dynamic range is better than 4000 : 1. Rough crosstalk measurements yield a ratio of 3 to 1000 of full scale. The signal input bandwith is approximately 30 MHz. A two-parameter fit (pedestal and gain) of the output response yields a 0.4% accuracy over the 2.5 V input range (VDD=5V). A curvature correction with eight sets of values for the 128 channels improves the accuracy to 0.07%. An increase in the supply voltage to 6 V increases the linear input range to more than 3.3 V, but also causes larger deviations from linearity, resulting in a 0.15% uncertainty in reconstructed amplitude after the eight set curvature correction.

The low cost of the integrated circuit and the high density of the signal channels makes the CDU particularly useful in high energy physics detectors, where a very large number signals have to be recorded simultaneously.

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REFERENCES

1. J.T. Walker, S. Parker, B. Hyams, and S.L. Shapiro, "Development of High Density Readout for Silicon Strip Detectors," Nucl. Instrum. Methods in Physics Research, Sec. A, Vol. 226, No. 1, September 1984, p. 200-203.
2. J.T. Walker, S.I. Chae, S. Shapiro, and R.S. Larsen, "Microstore – Stanford Analog Memory Unit," IEEE Trans. Nucl. Sci. NS-32, 616 (1985).
3. D.R. Freytag and J.T. Walker, "Performance Report for Stanford/SLAC Microstore Analog Memory Unit," IEEE Trans. Nucl. Sci. NS-32, 622 (1985).
4. D.R. Freytag, G.M. Haller, H. Kang, and J. Wang, "Waveform Sampler CAMAC Module," presented at IEEE Nuclear Science Symposium, 1985.
5. HMOS-I VLSI is understood to be that version of the N-MOS technology which employs 700 Å thick gate oxide (compared to 1000 Å for normal N-MOS), and 3 μ minimum channel length.