WAVEFORM SAMPLER CAMAC MODULE*

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ABSTRACT

A Waveform Sampler Module (WSM) for the measurement of signal shapes coming from the multi-hit drift chambers of the SLAC SLD detector is described. The module uses a high speed, high resolution analog storage device (AMU) developed in collaboration between SLAC and Stanford University. The AMU devices together with high speed TTL clocking circuitry are packaged in a hybrid which is also suitable for mounting on the detector. The module is in CAMAC format and provides eight signal channels, each recording signal amplitude versus time in 512 cells at a sampling rate of up to 360 MHz. Data are digitized by a 12-bit ADC with a 1 μs conversion time and stored in an on-board memory accessible through CAMAC.

1. INTRODUCTION

The central drift chamber of the SLD detector at SLAC[1] will produce multiple and partially overlapping signals in the regions of the detector which are hit by jets of particles. To disentangle the individual contributions to the signal stream, a complete record of the signal shape with good amplitude and time resolution is required. Similarly, the drift chambers of the Cerenkov Ring Imaging Detector (CRID) require a recording of the signal shapes. Existing devices, i.e. Flash Encoders or CCDs do not reach the required performance levels in versions which are economically acceptable for the planned large system of 20,000 or more channels. For these reasons a custom chip has been designed in collaboration between SLAC and Stanford University, which has a performance suitable for the purpose and uses a technology allowing low cost, high volume production. The device, named Analog Memory Unit (AMU) and described elsewhere[2,3] consists of a matrix of 256 analog storage cells which are sequentially addressed during reading or writing.

This paper describes a CAMAC module that has been constructed to test the performance of the AMU in beam tests using prototype drift chamber modules of the SLD detector. An important detail of the system being tested is the packaging of the AMU. Sixteen AMU chips and six fast TTL devices providing clocking signals are combined in a hybrid. Present plans call for mounting of the hybrid on the detector and the current tests of the system will explore in detail the feasibility of this approach.

2. AMU HYBRID

Packaging of the AMU and connecting it electrically is not a trivial task since each AMU has 47 pads. However, many of the connections are bussed across many devices and others are daisy chained. For that reason a hybrid package for a group of AMUs was implemented from the start[3] to keep the number of external connections at a manageable level.

The hybrid (HAMU II) used in this instrument contains 16 AMU chips with a total of 4096 analog storage cells, four fast TTL shift registers, one OR chip, and a dual JK flip-flop. The block diagram of Fig. 1 shows the subdivision of the hybrid into two groups of AMUs (A0..A7, B0..B7) with the input to each AMU externally accessible. The hybrid can thus be operated in a 16 × 256 or 8 × 512 cell mode. Each group has 16 fast write clock signals (F0A..F15A, F0B..F15B), which are generated by four fast shift registers 54F164. The shift registers are controlled by four external clocks (CP1..CP4), and two JK flip-flops (54F109). The slow write clock signals for each group of AMUs (ϕ_{1SA}, ϕ_{2SA}, and ϕ_{1SB}, ϕ_{2SB}) are derived from the appropriate fast clocks via the four gates of a 74LS32 chip. For the read cycle, each group of eight memory chips is controlled by a serial data-in signal /SDA (/SDB), one set of non-interleaving read clocks CK1A, CK2A (CK1B, CK2B), and the enable read signal ENA (ENB), respectively. The carry signals are named /ENDA and /ENDB. The outputs OUT and /OUT of the two groups are connected on the hybrid.

The following pins are connected to all 16 memory chips: +5DIG (supply of the AMU read shift register), +5ANA (all other supply voltages for the AMU), GND, VSUB (substrate voltage), /INP (the inverting input of the differential buffer amplifier of each cell, including the reference cell), /MR (reset for the write logic), /INHR1, /INHR2 (inhibit recycle signals for write and read), ANRES, ANINH (reset and inhibit signals for the analog part), /LD2 (load signal for the read address).

The master reset /MR also clears the JK flip-flops and the shift registers 54F164. VCC provides power to the TTL write clock logic.

The two groups of AMUs can be operated in interleaving or non-interleaving modes. The order of the input pins A0,B0,A1...B7 defines the order of data on read out in both cases.

The reference cell of the AMU chip in position A7 is connected to pins labelled REFIN (input), CKREF (clock), and OUTREF, /OUTREF (outputs).

Figure 2 shows the commercially manufactured prototype of the 48 pin hybrid. The dimensions of the hybrid are 2" × 2.6".
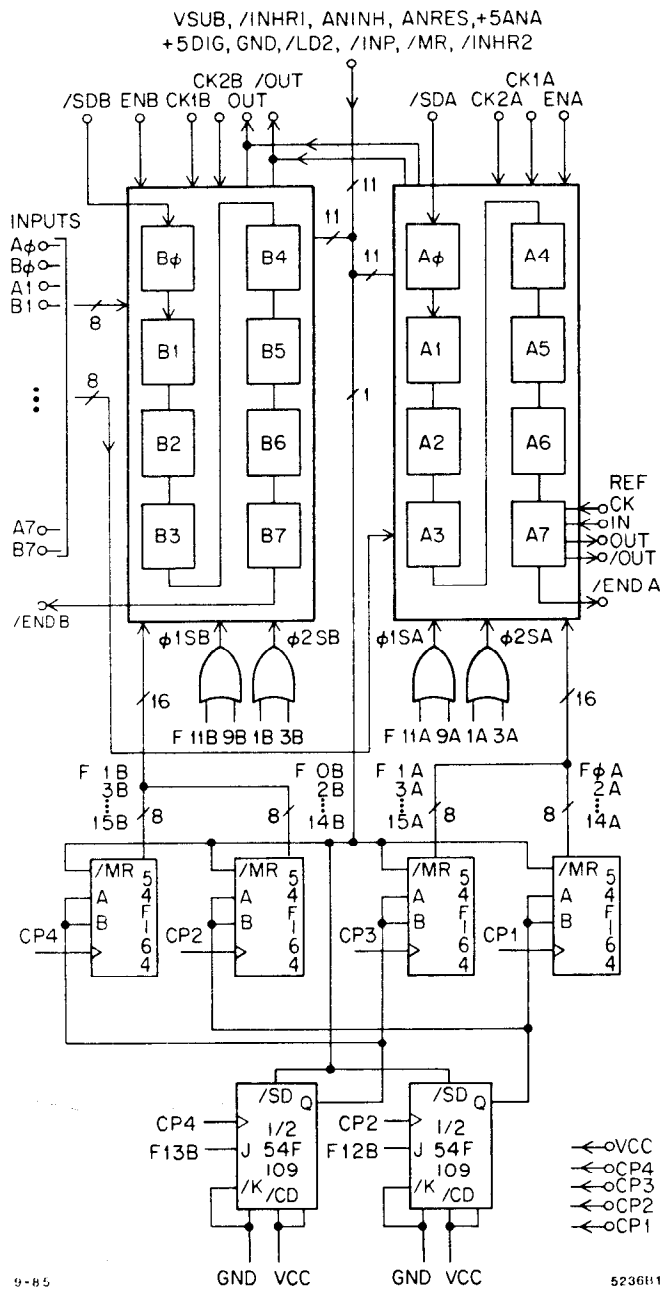
Fig. 1. Block diagram of the hybrid HAMU II. A0...B7 are AMUs. The remaining devices are the 8-bit shift register 54F164, the J-K flip-flop 54F109 and the quad or-gate 74LS32.

The maximum frequency at which data can be written into the eight signal channels of the HAMU II is 360 MHz. This limit is determined by the four 54F164 shift registers (rated at 90 MHz), which are driven by four interleaving clocks. The AMU device imposes essentially the same limit for the sampling rate since writing proceeds in interleaved mode into two AMUs, and each has a frequency limit of 200 MHz. The fast strobe signals generated by the shift registers are overlapping, which allows for satisfactory settling times of the signal on the AMU storage capacitor. The trailing edge of each strobe pulse determines the sampling time. The (90-10%)-fall time of the TTL strobe signal is in fact longer than the sampling interval considered here. However, the significant time interval is the transition from switch open to switch closed or about a 1 V
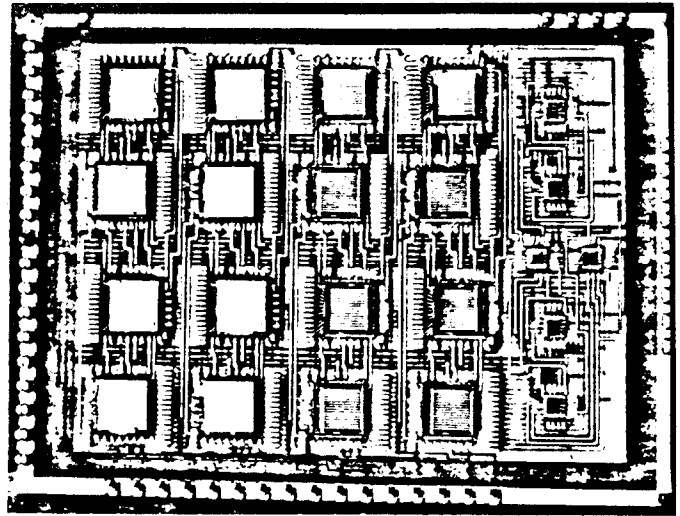

Fig. 2. Photograph of the assembled HAMU II.

change in gate voltage at any given signal level. By pulsing power to the 54F164 to ≈7 V during the write period, the swing of the gate voltage is increased and the fall time decreased to ≈2 ns/V. The effect of the finite fall time on the sampled data can be corrected for. A first test at 300 MHz has been performed and is described below.

The power consumption of the hybrid is five Watts and in order to cut down on the heat load to the detector, a program of power pulsing taking advantage of the low duty factor of the SLC accelerator will be implemented. The write cycle at SLC is only a few μs every few ms during which time VCC (power ≈1 W) and +5ANA (≈2 W) are required. The AMU device may then be powered down and it will retain the analog information. For reading of the analog information +5DIG power (≈2 W) must be applied to the hybrid in addition to +5ANA, but not VCC. The power duty factor is thus dominated by the duty factor of the read cycle (≈10 %) and can be further reduced by subdividing the system into small sequential blocks for purposes of reading.

3. DESCRIPTION OF THE WAVEFORM SAMPLER MODULE (WSM)

The Waveform Sampler Module processes eight analog signals under the control of three signals provided by a central WSM Fast Clock Generator (Fig. 3). The three signals are (1) Master Reset, (2) a train of clock pulses (140 MHz for the drift chamber tests), which causes the acquisition of the data samples, and (3) a convert signal, which initiates digitization of the analog data.

Each analog input signal is buffered through a unity gain, low output impedance amplifier consisting of two complementary pairs of transistors in Darlington configuration. This is needed in order to drive the high input capacitance (≈200 pF) of the HAMU II.

An acquisition cycle for analog data is started by the master reset (MR) signal which powers up VCC and +5ANA and initializes the logic (Fig. 4). After a time interval (<1 μs) the WSM receives a train of clock pulses, which are divided into four sets of interleaving clock pulses (CP1, CP2, CP3, CP4) driving the hybrid. Writing into the hybrid proceeds in interleaved mode into the two AMUs assigned to each signal channel. After completion of the analog write cycle power to the
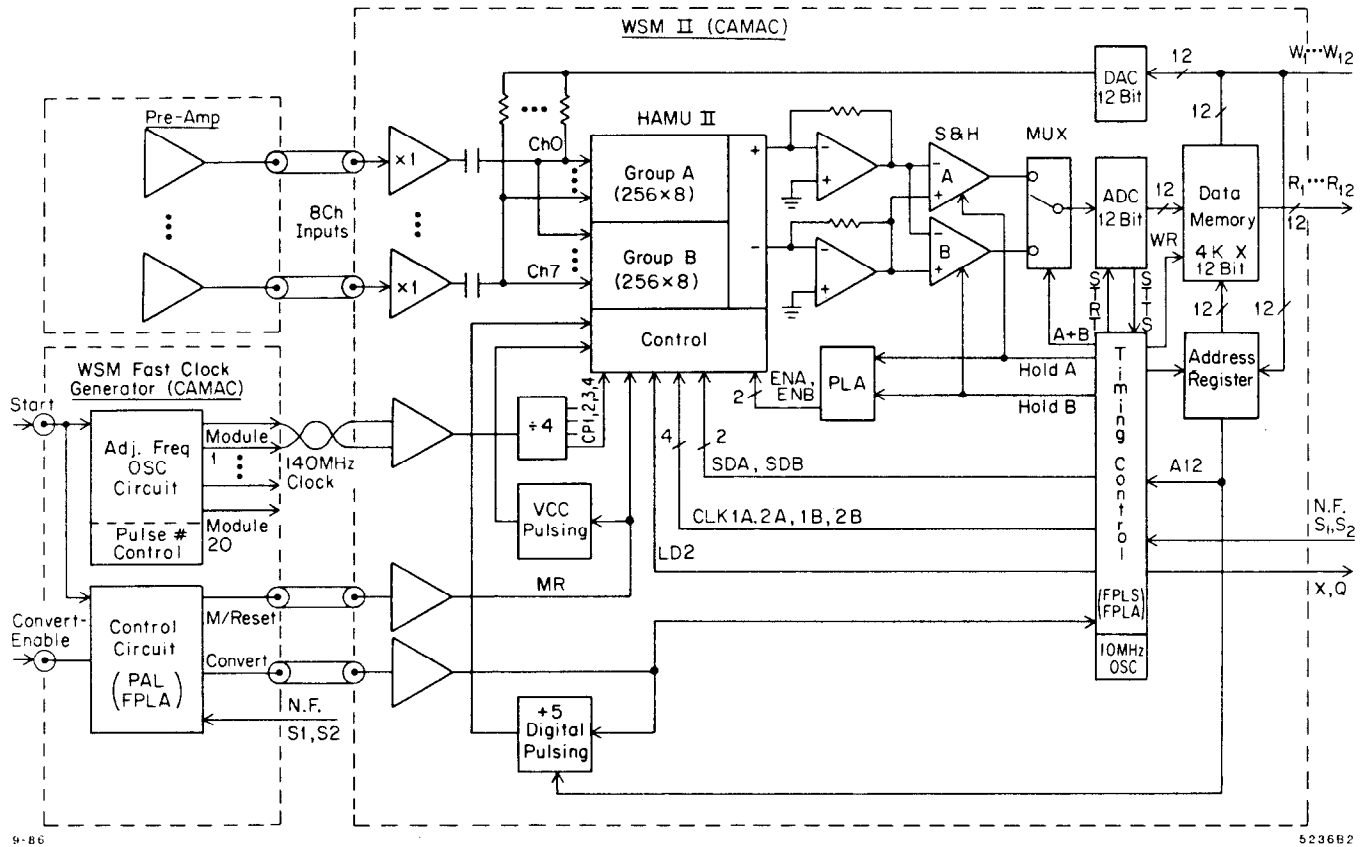
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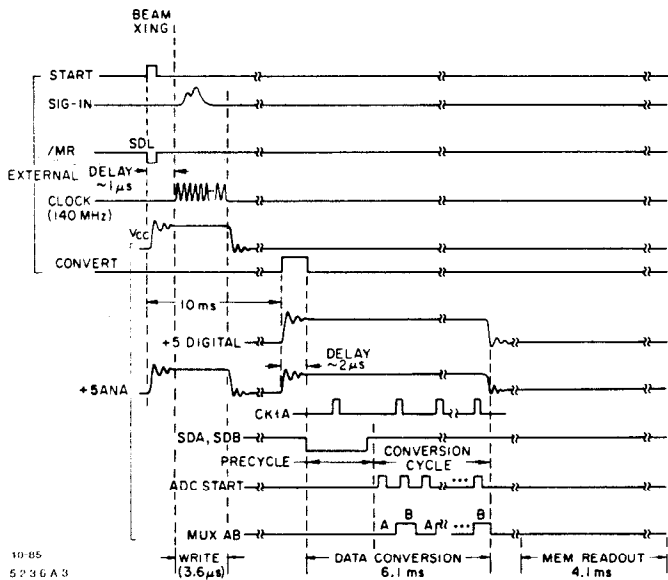Fig. 3. Block diagram of the CAMAC module WSM II.

Fig. 4. Timing diagram of external and internal signals in WSM II.

hybrid is dropped. The time constant for retention of charge on the sampling capacitors is of the order of 1 s.

The convert signal to the WSM brings up +5ANA and +5DIG power and initializes the read-out registers. The duration of the convert signal determines the settling time for power and the back edge starts the digitization cycle. Read out is interleaved between the two AMUs (A and B) serving

one signal channel. Two sample-and-hold (S/H) circuits are provided so that, as soon as data are held in A for digitization, data can be routed to S/H B (and vice versa) to maximize settling time. The analog data are digitized in a 12-bit ADC with 1 μs conversion time and stored in a 12-bit by 4-K-word memory, which is accessible through CAMAC. No corrections to the data (e.g. pedestal subtraction or zero suppression) are performed in this version of the instrument. The conversion cycle for the 4096 cells of HAMU II takes 6.35 ms.

After completion of the conversion cycle the memory address register is reset to zero and the digital data are available for a CAMAC block read. The address register can also be preloaded using the CAMAC code F17. Testing of the digital memory is possible with the help of the CAMAC write command F16.

A 12-bit DAC with a register under CAMAC control is used for calibration purposes and for biasing of the AMU devices.

4. PERFORMANCE OF THE WAVEFORM SAMPLER MODULE

Many of the tests and measurements described elsewhere[3] for an individual AMU device have been repeated for the WSM and the results will be summarized here. Since the version of the waveform sampler described in this paper (WSM II) was completed very recently, only preliminary measurements at 300 MHz sampling rate, presented below, have been performed using the new model. All other measurements refer to WSM I, which uses two of HAMU I[3], each containing eight AMUs. The six TTL devices included in HAMU II are located on the CAMAC board in the WSM I version. Results obtained with

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WSM I for drift chamber signals will be presented in a separate contribution to this Conference[6].

Calibration Measurements

Using the on-board DAC, the sampler response to various DC-levels was digitized repeatedly and the results analyzed. The RMS errors determined at each signal level and averaged over all 4096 cells are listed in the following table:

Table of RMS Values as a Function of Signal Voltage

SIG(mV)	1000	1600	1650	1730	1850	2100	2600	3000
RMS(mV)	0.5	0.6	0.6	0.6	0.6	0.6	0.8	1.2

The same data were used to determine pedestal and gain parameters for each cell. The curvature was parametrized by averaging, at each calibration level, the deviations of cell response from the linear approximation and saving the values in tabular form. A linear interpolation between the eight table values yielded adjustments for curvature of 10 mV or less, which were applied uniformly to all cells. Using these calibration data the uniformity of reconstruction of arbitrary DC signal levels was investigated. The RMS deviations from the nominal values, averaged over 4096 cells were measured to be 5 mV, as was obtained previously for single AMU devices[3]. It appears that the 5 mV limit is caused by small variations in curvature among the cells. An independent analysis[4] indicated that by parametrizing the curvature cell by cell through interpolation of an eight-valued table the residuals could be reduced to less than 2 mV. Such an approach would use large memory banks, but savings may be possible since the deviations show a repetitive pattern every 32 cells and it may be sufficient to define 32 correction tables instead of 4096 for each HAMU II.

Thermal drifts at the 10 mV level were observed over several days under normal laboratory conditions, that is without taking precautions to stabilize temperature. These drifts are believed to originate in the voltage-to-current converting output buffers. The differential construction of the on-chip output buffers insures temperature compensation if the signal level equals the bias at the inverting input (/INP). For signals different from the level at /INP the temperature coefficient was determined as 3.3 mV per °C per V at the input[5].

Sampling of a 20 MHz Sine Wave

A 20 MHz sine wave was applied to one input of the WSM I. At a 130 MHz sampling rate this resulted in the acquisition of 6.5 samples per period of the sine wave for a total of 80 periods. The digitized data were corrected cell by cell using pedestal and gain parameters, and globally for all cells for curvature as described above. The data points were fitted to a sine wave with four free parameters: amplitude, offset, frequency, and phase.

During the analysis it was discovered that the phase and frequency of the signal (and/or the sampling clock) were not sufficiently stable over the 80 periods of the sine wave which are sampled for each trigger. For that reason a fit was performed for the first 100 data points only (16 cycles of the sine wave). The next block of 300 data points was used to determine

32 additional constants describing the deviations from nominal of the 32 fast strobes, which are driven by independent shift register bits. The latter correction was on the average 0.3 ns (RMS) and is expected to be a constant for the module.

A small correction was applied to compensate for the slewing of sampling points due to the finite fall time of the gate pulse ($\approx$2 ns/V). The errors used for all fits were 5 mV for the amplitude and 150 ps for timing uncertainties, yielding unity χ^2 per point. This choice of weights produced uniform errors over the flat and the steep parts of the waveform, where the amplitude or timing errors dominate, respectively.

The fitted amplitude for the first 100 samples was 650 mV peak to peak, compared to 680 mV at the input. This yielded a time constant of the AMU sampling stage of 2.5 ns, about twice the expected value. However, the error in this determinations is quite large. The fitted mean of the signal was 1994 mV, off by 6 mV from the preset value of 2000 mV.

The new model WSM II was tested at high sampling rates. The input signal was again a 20 MHz sine wave while the sampling rate was increased to 300 MHz. The HAMU II was operated with pulsed power, which included a 1 ms period with power down to 1 V between the write and read cycles. The sampled points and the best fit sine wave are shown in Fig. 5. The points show a scatter of 20 mV in amplitude and 0.5 ns in time (RMS), but this is not believed to be the limiting performance of the device.
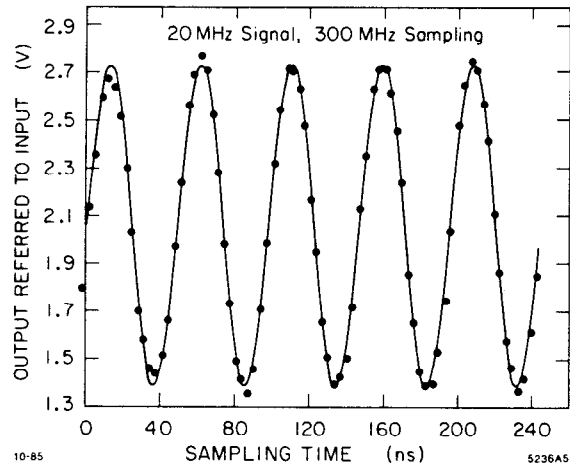

Fig. 5. A 20 MHz signal sampled at a 300 MHz rate. The dots are the measurements and the line is the best fit sine wave.

5. CONCLUSIONS

We are at present able to reconstruct a signal of 700 mV amplitude to 5 mV accuracy or 7.5% of its value ($\approx$7 bit accuracy, or about 9 bit if referred to the full scale range of 2 V). The timing error for each sample is 150 psec. With a more elaborate cell by cell curvature correction the amplitude uncertainty is expected to decrease to less than 2 mV.

The short term stability of a reading (as determined in calibration) is better than 1 mV corresponding to a dynamic range of more than 11 bits. Temperature variations affect the response of the device significantly, and methods to correct

for them using the reference cell are under investigation. It is desirable to design the write and read cycles in such a way as to keep the heat generated in the AMU chips constant and at a low level by pulsing power off while not writing or reading.

The performance levels listed above apply presently only to sampling rates of up to 130 MHz and to the HAMU I-package. Work is under way to test HAMU II more extensively and to determine the performance as a function of sampling frequency. A first test with 300 MHz sampling rate using WSM II has been performed and 360 MHz should be possible.

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