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THE 3081/E EMULATOR, A PROCESSOR FOR USE IN ON – LINE AND OFF – LINE ARRAYS *

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This paper presents a status report on the 3081/E covering the processor hardware, interfacing capability, and accompanying software. Details of production figures and preliminary performance results are given. Plans for the use of arrays of 3081/Es for parallel event processing in both on – line and off – line systems are outlined.

Introduction

The 3081/E, a processor designed by a CERN and SLAC collaboration (1), emulates an IBM System 370 series computer. It is a reduced instruction set machine with the following hardware features.

- Modular architecture – separated execution units with distributed microcode.
- Large memory – up to 7 Mbytes of separated program and data memory configurable in 1/2 Mbyte units.
- FORTRAN 77 – fully supported, with the exception of I/O instructions, including double precision 64 bit floating point thus giving results identical bit for bit to an IBM CPU.
- Conservative design of execution units – maximum chip propagation delay times used in calculating critical timing paths.
- Flexible high speed interface – easily adapted to different external bus specifications. The 3081/E has 64 bit internal data paths capable of a 64 MByte/sec transfer rate.
- High performance – results indicate agreement with the design estimate of > 1 unit IBM 370/168. The upper limit depends on how efficiently the program pipelines in the 3081/E.
- Attractive price – performance – large incremental processing power at low incremental cost.
- Hardware simplicity – pipelining complexity is handled by a software package that performs code optimisation whilst translating IBM object code to 3081/E microcode.

The resulting processor represents a powerful tool well suited to event data processing in both the on – line and off – line environments.

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Hardware Status

Although still undergoing rigorous acceptance tests, prototype versions of the 3081/E run High Energy Physics code at both CERN (BINGO and INGER, the UA1 and R807 track reconstruction programs) and SLAC (MVFIT a multivertex kinematic event fitting program). Bulk production of the processor has started both at CERN (9 units), and SLAC (5 units). The status of the individual hardware elements can be summarised as follows.

- Memory – 8 layer printed circuit production version with 1/2 Mbyte plus byte parity based on 16K bit 55 nsec static RAMs.
- Execution units – prototype and initial CERN production batch in wire–wrap. Construction of Multiwire units is well advanced at SLAC with two of the 5 execution units already tested.
- Interface – a dual port wire–wrap board separated logically into a common general part which drives the internal 3081/E busses, and a specific part which communicates with an external bus. It is only the latter which need be changed if an interface to a different system is required. This feature has already been demonstrated by the successful construction of interfaces to CAMAC, VME, IBM PC, and an IBM channel. The channel connection is made via a Device Attachment Control Unit (DACU) and CAMAC at CERN, and DACU and IBM PC at SLAC, with data transfer rates in excess of 100 Kbytes/s.

This flexible interfacing capability means that the processor has already been hosted by a range of computer systems including NORD, IBM PC, IBM mainframe, Apollo, Motorola 68000, and VAX.

Software Status

The hardware development of the 3081/E has been accompanied by corresponding software development at all stages. The initial design of the execution units was validated by FORTRAN simulations representing the logic at the gate level. Test bench communication with the 3081/E is handled by powerful controller /debugger software –

- SINEX running at CERN on NORD, IBM mainframe, VAX, Motorola 68000, and on an Apollo at SACLAY,
- SNOOPY at SLAC running on an IBM PC and mainframe.

Features of these packages include facilities for testing individual boards in stand alone mode, load and verify of programs, edit memory, set program counter, start process, single step program execution, and examination of registers. They also allow flexible test definition by means of driver and procedure files.

Offline data processing systems comprising a host computer and one or more attached 3081/E processors achieve high efficiency by splitting user programs into two parts. One, which is I/O intensive, runs on the host, and the other, which should be CPU intensive, runs on the 3081/E(s). To facilitate this split, a simple set of routines has been developed.

- SYEDWN(ID,IUNIT,OPTN,IRET) downloads the program into the 3081/E,
- SYEPUT(ID,COMIN,DATIN,OPTN,IRET) writes data into processor memory and optionally initiates execution,
- SYEGET(ID,COMOUT,DATOUT,OPTN,IRET) waits for the processor to finish before reading data back to the host.

To run a program in the 3081/E, the CPU–intensive part of the user's program is first translated. The host program calls SYEDWN to read the translated microcode from logical unit IUNIT and transfer it

into the 3081/E program memory. After the input data is read from tape or disk, SYEPUT is called to transfer data from the host variable DATIN to the processor memory starting with the first word in the common block specified by COMIN, a character string with it's name. Usually, the host variable DATIN is the first word of the same named common block. Similarly, SYEGET transfers results from the processor back to the host.

Translator Status

Converting IBM object code to 3081/E microcode is performed by a translator program which, when operating in pipelined mode, takes account of specifically designed hardware features to perform code optimization. The steps involved in this process are :

- Identification of the START, END , PROLOG, and EPILOG of each program unit
- Analysis of the branch structure, and for each block of linear code

  - Allocation of a double index register if needed
  - Combination of IBM instructions to super instructions
  - Allocation of spare floating point registers
  - Preferential re−ordering of IBM instructions
  - Conversion to microcode
  - Instruction pipelining
  - Allocation of another double index register if required and re−translation

The translator has been successfully tested on Mbyte sized programs, eg. BINGO, and preliminary results show a shrinkage factor of 60 % between unpipelined and pipelined code.

Current Activities

The design and prototype testing phases being finished, 3081/E project activity is now concentrated in four main areas, translator optimization, processor production, off−line farm evaluation, and on−line integration.

A considerable number of requests for machines have been received both in Europe and the USA.

At CERN the off−line farm evaluation takes the form of a pilot project in which up to five 3081/Es will be attached to an IBM 4361 via an in−house designed channel to VME interface rated at 3 Mbytes/s. When operational, the complete system will have at least the power of an IBM 3081K. A similar project underway at SLAC will see a number of 3081/Es attached to the central IBM via the channel/DACU interface.

An initial on−line activity at CERN is the commitment to replace the six 168/Es used at UA1 for trigger/filter purposes (2) by 3081/Es fully integrated into a new VME based data acquisition system (3). An exciting additional feature of this exercise is the intention to configure the system in a way that will also allow it to be used for off−line data processing. Such a scheme, allied with the potential installation of optical disks on the VME bus, would result in considerable computing power being available in the experimental counting room. At SLAC the 3081/E will be used in a FASTBUS data acquisition environment at the Mark II detector for data reduction purposes.

In addition, two external groups have become interested in using the 3081/E as a basic element in their own projects, the development of a VAX emulator and an array processor (APE), both of which are presented at this conference (4,5).

Summary

The 3081/E can be considered to be a working processor. It has achieved its main design aims of speed, reproducibility, and interfacing flexibility, and is available with a full range of software support tools. Ten units have been built and more are in preparation to meet the needs of numerous clients. Work has started on developing off−line data processing farms, and on integrating the 3081/E into on−line environments. Both of these applications demonstrate its value in the role of attached processor for parallel event processing.

References

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