FASTBUS FOR THE PARTICLE ACCELERATOR LABORATORIES*

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Introduction

The FASTBUS modular high speed data acquisition and control system for high energy physics and other applications was described by Costrell and Dawson at the 1983 Particle Accelerator Conference [1]. Both the specification and the implementation of this interlaboratory development have progressed considerably since that time. Because of its many attractive features, FASTBUS is currently in use in several major nuclear and high energy physics laboratories and is also finding application in other areas.

The initial impetus for the development of FASTBUS came from the high energy physics community, since demands placed upon data acquisition systems by experiments in high energy physics were clearly beyond the capability of existing systems. The experiments being planned involved data rates much higher than had previously been encountered and total events were increasing because of improved accelerator technology. These were accompanied by order-of-magnitude increases in the size and complexity of the associated detectors and particularly in the number of detector outputs that had to be expeditiously viewed and processed by the electronics. To meet this need for an extremely fast and versatile system, an interlaboratory effort was launched, resulting in the FASTBUS system.

Description

FASTBUS, as shown in figure 1, consists of multiple bus Segments which operate independently and concurrently, but which can automatically and transparently link together for intersegment communication. A bus Segment may be implemented either as a Cable Segment to which devices may be connected or as a crate backplane which can accommodate up to 26 devices. The multiplexed data and address fields are 32 bits wide. FASTBUS can operate asynchronously using a handshake protocol to accommodate different speed devices without prior knowledge of their speed capabilities. It can also operate synchronously without handshake for transfer of blocks of data at maximum speed. System speed is limited solely by propagation and logic delays. Some FASTBUS systems currently in operation have data transfer rates of 160 megabytes per second.

Specification

The FASTBUS specification has been issued as a U.S. Department of Energy Report [2, 3] and has been adopted by the ESONE committee of European Laboratories. It has also been approved as a Standard of the Institute of Electrical and Electronics Engineers (IEEE) and of the American National Standards Institute (ANSI) [4]. Additionally the document is currently being processed as an international standard of the International Electrotechnical Commission (IEC). French and Chinese translations have been made.

Since the details of operation of FASTBUS have been previously presented and full specifications published, they are not repeated here. However it should be noted that, as with any developing system, minor modifications and clarifications have been found to be
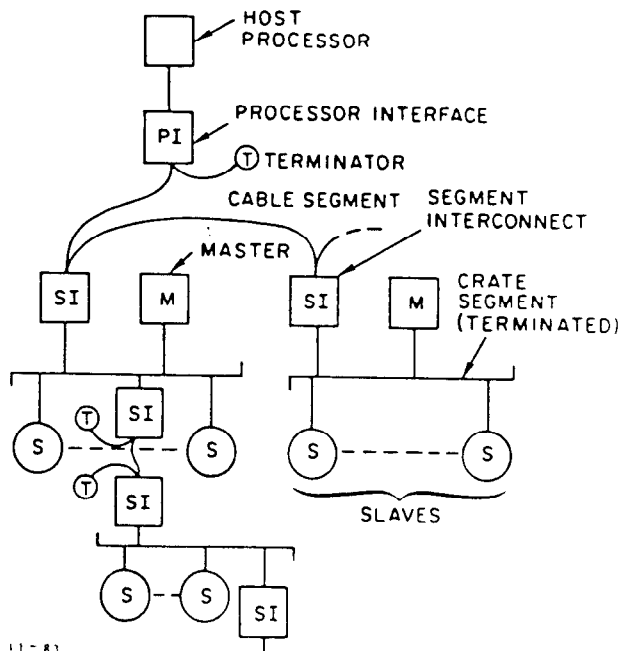

Figure 1. Example of FASTBUS System Topology

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desirable and full information regarding them is available in the April 1985 Supplement [3] to the FASTBUS specification. The clarifications and modifications will be integrated directly into the ANSI/IEEE FASTBUS standard [4] (which is why the publication of ANSI/IEEE 960 has been delayed somewhat) and into the corresponding ESONE document [5]. Of course, we will take steps to assure that ANSI/IEEE Standard 960 and the corresponding international publication of the IEC are technically identical.

Laboratories Implementing FASTBUS

A comprehensive review of FASTBUS applications and developments in laboratories and universities in the U.S.A. and abroad has been presented by Walz [6]. Institutions included are:

Brookhaven National Laboratory

Cornell University Medical College

Fermi National Accelerator Laboratory

University of Illinois

University of Wisconsin

Lawrence Berkeley Laboratory

Los Alamos National Laboratory

Stanford Linear Accelerator Center

TRIUMF, University of British Columbia

KEK, National Laboratory for High Energy Physics, Japan

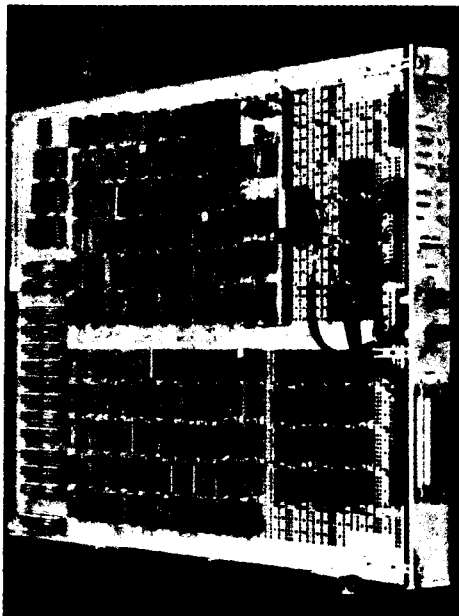IHEP, Institute of High Energy Physics, Beijing, Beijing, China

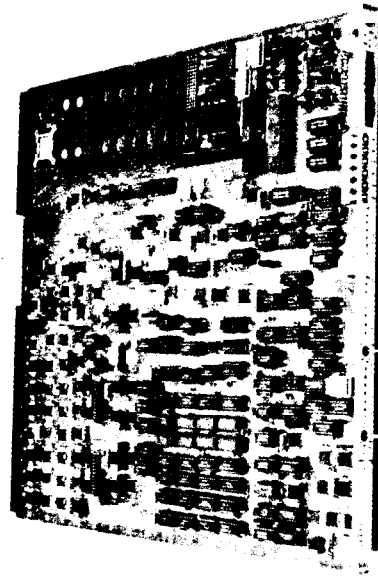Figure 2.   FASTBUS Sequencer Module (CERN)

Figure 3.   FASTBUS SNOOP Diagnostic Module (SLAC)

Ponting of CERN has reported on European Progress on FASTBUS [7]. In addition to CERN, European institutions actively participating in the development and use of FASTBUS include:

HEPHY, Vienna, Austria

University of Edinburgh, Rutherford and Appleton Laboratories, UK

LAPP Annecy, College de France, Ecole Polytechnique, LPTHE Orsay

CEN Saclay, CRN Strasbourg, France

Universities of Freiburg and Seigen, West Germany

NIKHEF Amsterdam, Holland

INFN Pisa, INFN Rome, Italy

CND Valencia, Spain

AFI Stockholm, GWI Uppsala, Sweden

SIN, Switzerland

Examples of FASTBUS Implementations

Three of the initial collaborations established to exploit the LEP Collider facility at CERN intend prodigious use of FASTBUS in their experiments, while the fourth will install the system in those areas where its unique features make FASTBUS indispensable. As an example of the magnitude of these experiments the readout system for the Time Projection Chamber on one of them will require almost 150 crates of FASTBUS electronics, all fully powered and cooled. Figure 2 shows the FASTBUS Sequencer Module developed at CERN.

At the Fermi National Accelerator Laboratory (FNAL) part of the Collider Detector Facility data acquisition system consisting of 12 FASTBUS crates is presently being installed for operation by August 1985.

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At the Stanford Linear Accelerator Center (SLAC) the Mark II/SLC Detector Upgrade project is installing 6 FASTBUS crates for operation by July 1985. Final prototypes of the SNOOP Diagnostic Module for FASTBUS are being tested and associated software is being developed at SLAC and FNAL (Figure 3).

A large FASTBUS system to be used with the TOPAZ detector for studies of electron-positron collisions at TRISTAN in KEK will be described in an article being prepared by Hirokazu Ikeda. Since this system uses CAMAC together with FASTBUS, a CAMAC Crate Controller with a FASTBUS Cable Segment, as shown in Figure 4, has been developed at KEK.

Other Work in Progress

Progress on FASTBUS software has been reported by Gustavson [8]. Rimmer has summarized FASTBUS software developments in Europe [9]. The draft document on software routines for FASTBUS has been extensively reviewed and a firm version is expected to be available in late 1985.

Work is in progress at TRIUMF on the design of address interface (ADI) and protocol (PCL) chips to simplify circuit design and save circuit board real-estate. Some of this has been reported on by Skegg and Daviel [10].

FASTBUS Products

FASTBUS products commercially available or under development are summarized in the article by Walz [6].
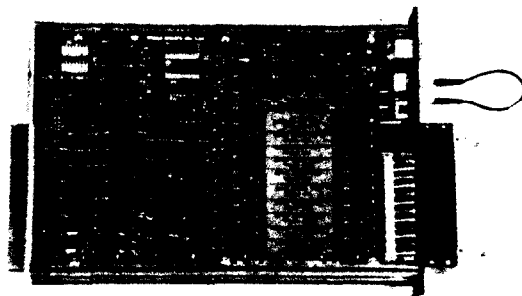

Figure 4. CAMAC Crate Controller with FASTBUS Cable Segment (KEK)

References

1. L. Costrell and W.K. Dawson, IEEE Trans. Nucl. Sci., NS-30, No. 4 August 1983, p 2147-2151.

2. FASTBUS Modular High Speed Data Acquisition and Control System for High Energy Physics and Other Applications, U.S. Dept. of Energy Report DOE/ER-0189, December 1983.

3. April 1985 Supplement to DOE/ER-0189, December 1983 (See Ref. 2, above).

4. FASTBUS Modular High Speed Data Acquisition and Control System, ANSI/IEEE Std. 960 (to be published).

5. ESONE Committee of European Laboratories FASTBUS document to be published to replace ESONE/FB/01, May 1983.

6. H.V. Walz, FASTBUS Review 1984, IEEE Trans. Nucl. Sci., NS-32, No. 1, February 1985, p 253-257.

7. P.J. Ponting, European Progress on FASTBUS, IEEE Trans. Nucl. Sci., NS-32, No. 1, February 1985, p 258-261.

8. D.B. Gustavson, FASTBUS Software Progress, IEEE Trans. Nucl. Sci., NS-32, No. 1, February 1985, p 269-270.

9. E.M. Rimmer, FASTBUS Software in Europe, IEEE Trans. Nucl. Sci., NS-32, No. 1, February 1985, p 271-273.

10. R. Skegg and A. Daviel, A General Purpose FASTBUS Interface Chipset, IEEE Trans. Nucl. Sci., NS-32, No. 1, February 1985, p 305-308.