SLAC – PUB – 3651
April 1985
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Timing System Control Software in the SLC*

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ABSTRACT

A new timing system[1] that allows precision (~1–2 ns) control of the trigger times of klystrons, beam position monitors, and other devices on a pulse-to-pulse basis at up to 360 Hz is in operation in the first third of the SLAC linear accelerator. The control software is divided between a central host VAX and local Intel 8086–based microprocessor clusters. Facilities exist to set up and adjust the timing of devices or groups of devices independently for beam pulses having different destinations and purposes, which are run in an interlaced fashion during normal machine operation. Upgrading of the system is currently underway, using a new version of the Programmable Delay Unit CAMAC module to allow pipelining of timing information for three machine pulses. An overview of the current state of the system is presented in this paper, with an emphasis on software control.

1. SYSTEM ARCHITECTURE

The interlaced operation of beams with different paths, repetition rates, energies, and functions is based on a 16–bit code called PPYY. This code is used by the timing software and hardware to select the times at which devices should be triggered on an upcoming machine pulse. The high order eight bits, called PP or the "beam code", are used to select the time delays for klystrons, kicker magnets and other devices which are needed to produce a specific type of beam. The low order eight bits, called YY, are used to synchronize additional devices; for example, when a user wishes to gate and readout beam position monitors[2].

The general architecture of the timing system is shown in Fig. 1. The reference signal for timing, a 476 MHz CW signal with a phase-locked 2.1 ns "fiducial pulse" superimposed at a rate of 360 Hz, appears on the main drive line. Communication of PPYY occurs on a dedicated subchannel of the CATV communications cable, the same cable which is used for communication between control programs residing in the VAX and the local microclusters. Each microcluster consists of an Intel 86/30 single board computer (SBC) housed in a Multibus crate containing, among other things, a Pattern Receiver Interrupt Module (PRIM) and a Multibus CAMAC Driver (MBCD). The same timing software runs in each of the sector microprocessors, with the particular configuration of triggered devices being specified in the appropriate section of the SLC database. In addition to the sector microclusters there is a special microcluster responsible for broadcasting the PPYY code on the communications cable. At present this Master Pattern Generator (MPG) microcluster receives PP beam codes from the previous linac control system. In the future, it will generate beam codes according to operator-determined rates and priorities. The MPG also processes operator requests to associate a YY code with an upcoming PP beam code.

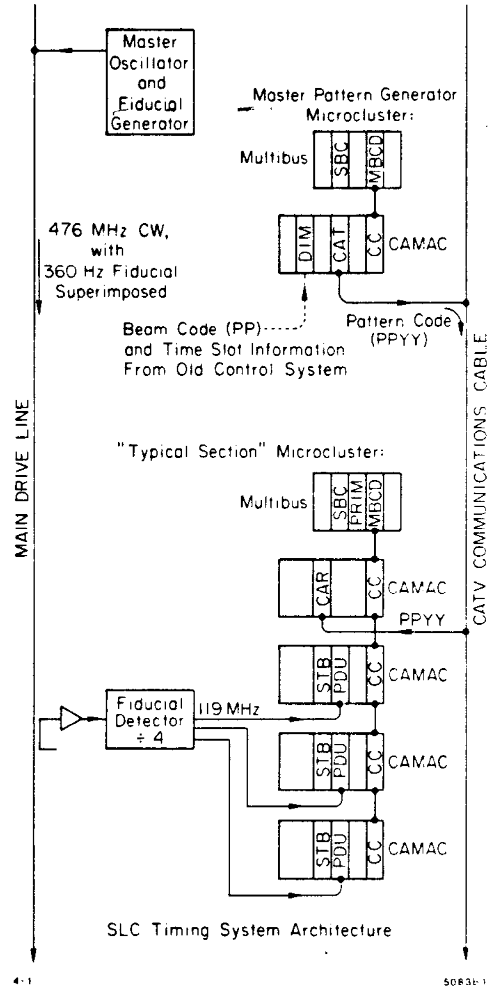

Master Oscillator and Fiducial Generator
Master Pattern Generator Microcluster:
Multibus
SBC
MBCD
476 MHz CW, with 360 Hz Fiducial Superimposed
DIM
CAT
CC
CAMAC
Beam Code (PP) and Time Slot Information From Old Control System
Pattern Code (PPYY)
MAIN DRIVE LINE
CATV COMMUNICATIONS CABLE
"Typical Section" Microcluster:
Multibus
SBC
PRIM
MBCD
CAR
CC
CAMAC
PPYY
STB
PDU
CC
CAMAC
Fiducial Detector ÷ 4
119 MHz
STB
PDU
CC
CAMAC
STB
PDU
CC
CAMAC
SLC Timing System Architecture

Fig. 1. The timing system architecture. CAR = Cable Access Receiver; CAT = Cable Access Transmitter; CC = SLC Serial Crate Controller; DIM = Digital Input Module; MBCD = Multibus CAMAC Driver; PDU = Programmable Delay Unit; PRIM = Pattern Receiver Interrupt Module; SBC = Single Board Computer (Intel iSBC 86/30); STB = Simple Timing Buffer.

The PPYY code is broadcast on the cable through a Cable Access Transmitter module and received by a Cable Access Receiver module in each of the sector microclusters. Receipt of PPYY by the Cable Access Receiver module causes the Pattern Receiver Interrupt Module to produce a Multibus interrupt that invokes an interrupt handler in the microprocessor timing software (see below).

Two new CAMAC modules, the Programmable Delay Unit (PDU) and the Simple Timing Buffer (STB) are currently being installed and tested in the SLC timing system, replacing earlier versions of these modules that have been used in the

* Work supported by the Department of Energy, contract DE–AC03–76SF00515.

Poster paper presented at the 1985 Particle Accelerator Conference,
Vancouver, B.C., Canada, May 13–16, 1985

first ten sectors of the linac during the past two years. The PDU[3] has 16 channels, each of which can produce a trigger at a different time with respect to the fiducial. The PDU is clocked by a signal from the fiducial detector, which produces a 119 MHz pulse train (476 Mhz Main Drive Line signal divided by 4) with a missing pulse at fiducial time. Thus the PDU counts "ticks" of approximately 8.4 ns (1/119 MHz) starting from the fiducial. The output pulses from the sixteen channels of the PDU are distributed on the upper backplane of the CAMAC crate. These signals may also be brought out through the front panel of the STB.

2. PROGRAMMING MODES OF THE PDU

Each PDU channel can be programmed in one of four different modes. The timing system software uses information in the database to determine in which mode a channel is to be used. Internal to the PDU is an array, the pattern timing table, which can contain up to 256 19-bit delay values for each of the 16 channels. How (and whether) all these values are used for a given channel depends on which of the four programming modes is used for that channel:

1. PP mode: the delay time with respect to the fiducial depends on the beam code PP. Delay values for different PP's are stored and updated in an array in the VAX (see next section); the appropriate parts of this array are sent to the microprocessor, which loads them into the pattern timing table of the PDU via CAMAC.

2. YY mode: The delay time with respect to the fiducial depends on the value of YY. A particular YY value can be made to produce specified delay(s) from specified channel(s) by programming the appropriate locations in the PDU pattern timing table.

3. Base-rate mode: Only the first 36 locations in the part of the pattern timing table for a given channel are used, as a modulo-36 counter. The pattern of delays in these channels is repeated ten times each second (see Fig. 2).

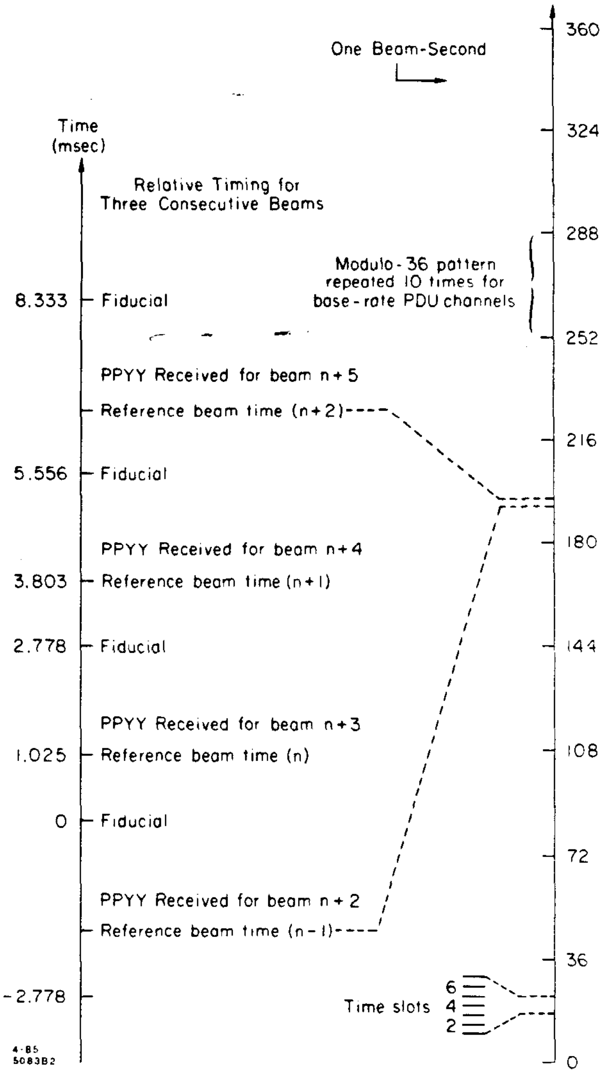
4. Reuse mode: The same delay is produced on every pulse, regardless of the value of the PPYY code.

3. SOFTWARE DATA STRUCTURES

The most important data structure used by the timing control software in the VAX is the T-MATRIX, which is in shared memory, accessible to the SLC Control Programs (SCPs) and to other programs running in the VAX. The rows of the T-MATRIX correspond to the beam codes and the columns to triggered devices. In other words, a row of the T-MATRIX contains the time delay with respect to the fiducial, in units of PDU ticks, for each of the devices in the system that are to be triggered according to the value of the PP part of the PPYY code.

The time delay with respect to the fiducial of the pulse produced for a triggered device by its associated PDU channel is the sum of several components:

TDELAY = TREF + PDUT + TNOMINAL + OFFSET



One Beam-Second
Time (msec)
Relative Timing for Three Consecutive Beams
Modulo-36 pattern repeated 10 times for base-rate PDU channels
8.333
Fiducial
PPYY Received for beam n+5
Reference beam time (n+2)
5.556
Fiducial
PPYY Received for beam n+4
3.803
Reference beam time (n+1)
2.778
Fiducial
PPYY Received for beam n+3
1.025
Reference beam time (n)
0
Fiducial
PPYY Received for beam n+2
Reference beam time (n-1)
-2.778
Time slots
6
4
2
4-85
5083B2
360
324
288
252
216
180
144
108
72
36
0

Fig. 2. Relative timing diagram.

Two of these components are independent of the beam code and are kept in the database. The first component, TREF, is associated with the PDU, while the second component, PDUT, is associated with the triggered device. TREF is the time delay needed to produce a PDU pulse that is simultaneous with the passage of a reference beam, as seen on an oscilloscope. The PDU pulse is brought to the oscilloscope through an STB, and the signal from the passage of the beam comes through a CAMAC module. The reference beam is produced 1025 μs after the fiducial, as measured by a standardized procedure at the injector. Thus TREF is essentially the time of passage of the beam with respect to the fiducial, when all propagation delays are taken into account. PDUT is a "standard" delay with respect to the passage of the beam for the triggered device with which it is associated. TNOMINAL is a term associated with a specific beam code, that takes account of the fact that the beam may be shifted with respect to the reference beam time. TNOMINAL can in fact be different for different sectors of the machine on the same beam code. Any additional corrections needed for the triggered device on a particular beam are represented by the OFFSET term.

The T-MATRIX is automatically set up by a program called TGEN, using information in the database. TGEN searches the database for devices that are to be triggered according to the PP beam code, allocates space for each of them in the T-MATRIX, and sets up arrays of pointers into the T-MATRIX. TGEN is run immediately after a new database is generated or after changes have been made in the database that will affect the structure (as opposed to just the values) in the T-MATRIX. After TGEN has been run, saved sets of delay values for triggered devices can be restored to the appropriate locations in the T-MATRIX.

4. CONTROL FUNCTIONS AND USER INTERFACE

The PP-mode channel delay times can be set up using an interactive facility called Beam Design Language (BDL). As the name suggests, it is used to design a configuration of triggered devices for a specific beam. Users of BDL may activate triggers to the "standard" delay value TREF+PDUT, on the desired PP beam codes, and they may add on an arbitrary OFFSET. They may also deactivate a trigger on a given PP by setting the corresponding delay value to a special value that causes the PDU to produce no output pulse. BDL also includes commands to copy sets of timing values from one PP to another, and adjust TNOMINAL for a specific beam PP. All of these actions occur by first changing delay value(s) in the T-MATRIX and then sending a message to the micro(s) to update the data in the pattern timing table of the appropriate PDU(s).

The SLC Control Program running in the VAX allows users to control the delay times that are output by PP-mode PDU channels in a straightforward manner. Users may activate and deactivate triggers from touch panel buttons and may adjust a delay or set of delays from a knob. Like BDL, the SCP operates on values in the T-MATRIX and then sends messages to the micros to update the data inside the PDUs.

The YY-mode channels delay times are put into the PDU's pattern timing table on request from the BPM or other software, in advance of the receipt of the desired YY(s).

The reuse channel delay times can only be changed by editing the database and then rebooting the micro; these times are not intended to be changed casually. Programming of the baserate mode PDU channels is still under development.

5. TIMING SYSTEM SOFTWARE IN THE MICROPROCESSORS

Timing system software support in an individual sector microprocessor is provided by one of a set of jobs running in the multitasking environment provided by the Intel iRMX operating system. The timing job consists of a background task, a pattern interrupt task, and a pattern error interrupt task. When the machine is run in pipelined mode, the pattern interrupt task will be responsible for reading the 16-bit code PPYY for the "next plus two" beam from the pattern register on the PRIM board and then broadcasting the three pipelined PPYY codes to the CAMAC crates.

The most important functions of the timing job's background task are to initialize the PDUs and to update timing delay values in PDU memory upon request from SCPs or other programs running in the VAX.

Errors occurring in the communication of PPYY are detected using the cyclic redundancy checksum encoded as part of the SDLC network protocol. If such an error is detected by the CAR, a special pattern error interrupt is generated instead of the normal pattern interrupt.

All of the timing job routines are written in Fortran 77, except for the pattern interrupt handler which is written in 8086 assembly language.

ACKNOWLEDGEMENTS

The original design of the timing system architecture is due to M. Breidenbach and R. Melen. M. Breidenbach also designed and implemented the first version of Beam Design Language. Many other people have contributed to the hardware developed for the timing system, particularly E. Linstadt, L. Paffrath, R. Koontz, and M. Ross. D.Yaffe and A. Hunter wrote early versions of the interrupt handler. We also thank K. Jobe, M. Ross, and J. Bogart for many useful discussions regarding the timing software.

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