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A PROGRAMMABLE DELAY UNIT INCORPORATING A SEMI-CUSTOM INTEGRATED CIRCUIT*

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1. INTRODUCTION

The synchronization of SLC accelerator control and monitoring functions is realized by a CAMAC module, the PDU II (Programmable Delay Unit II, SLAC 253-002), which includes a semi-custom gate array integrated circuit. The PDU II distributes 16 channels of independently programmable delayed pulses to other modules within the same CAMAC crate. The delays are programmable in increments of 8.4 ns. Functional descriptions of both the module and the semi-custom integrated circuit used to generate the output pulses are given.

2. PDU II DESCRIPTION

The module provides 16 independent channels of timing signals delayed relative to the fiducial (or reference time) detected on the 119 MHz pulse train received from the FIDO[1]. The timing signals are differential ECL pulses eight clock cycles long, delayed a programmable number of 8.4 ns increments relative to the fiducial. A buffered differential ECL version of the 119 MHz clock received from the FIDO is also distributed throughout the CAMAC crate on an auxiliary upper backplane.

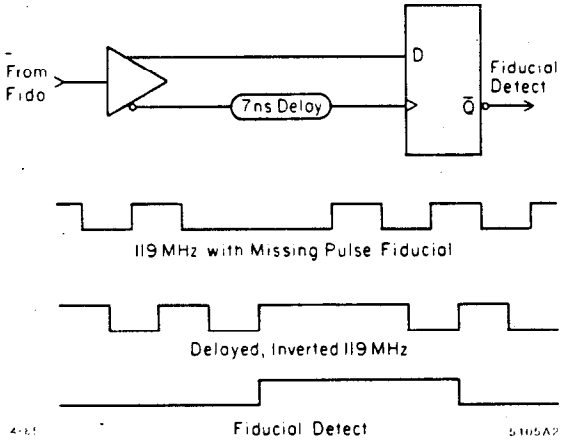

Fig. 1. Digital Fiducial Detection.

Delay values for each of the 16 channels are obtained by looking up the appropriate entry in the Pattern Timing Table whenever a fiducial is detected. See Fig. 2. The Pattern Timing Table holds the Beam Matrix[2], the timing information describing the set of possible time multiplexed linac pulses. Elements in the Pattern Timing Table, a 4K by 20 bit RAM, are the 256 possible delays required for each of the 16 channels. The desired values are selected by using either an 8 bit field of the data stored into one of three Pattern Input Registers (describing the next three cycles of the linac), by using a modulo-36 Time Slot Counter, or by using Pattern Timing Table location 'FF'H (dedicated to reuse/standby operation) as an index pointer into the Pattern Timing Table. This choice is determined for each channel by the mode selected by the value stored in the Mode Select Table. The delay values of interest are transferred from the Pattern Timing Table to two Semi-Custom Integrated Circuits, the Eight Channel Alarm Clock (ECAC). After all 16 channels have been set up, the Pattern Input Registers are overwritten with the standby pointer value of 'FF'H, the Time Slot Counter is incremented, the Pattern Timing Table Pointer is restored to the value it held before the fiducial was detected, and the outputs of the ECACs are enabled. The entire programming cycle, from fiducial detection to the enabling of the outputs, is completed in less than 12 microseconds.

The outputs of the ECAC directly drive the auxiliary upper backplane, distributing the required timing signals. Fiducial detection resets a counter in the ECAC, which is incremented by the 119 MHz clock received from the FIDO. When the time elapsed since the fiducial, as indicated by the counter, is equal to the desired delay value stored in the ECAC for a given channel, an output pulse 8 clock cycles long is generated for that channel.

Additional features were incorporated into the PDU II to simplify the supporting control system software and to aid maintenance. Successive reads or writes from the Pattern Timing Table automatically increment the Pattern Timing Table Pointer. The Pattern Timing Table is initialized to 'FFFFF'H after power-up or a CAMAC reset command. Latched status bits indicate the detection of and the absence of fiducials. The ECACs may be run from an internal 8 MHz clock, and fiducials may be 'generated' by a CAMAC command, allowing standalone operation for diagnostic purposes.

3. ECAC DESCRIPTION

The ECAC, or Eight Channel Alarm Clock, is an ECL semi-custom (gate array) integrated circuit which performs the delayed timing pulse generation for 8 channels in the PDU II, two such chips being used in each module. It is implemented as a design option on the Fairchild FGE 2000 array[3]. Details on the semi-custom design process were presented in a previous paper[4].

A simplified block diagram of the ECAC, showing the pulse generation logic for one of the channels, is shown in Fig. 3. Buffers on the chip distribute the 119MHz waveform received from the FIDO as a CLOCK directly to the upper backplane. A RESET pulse, derived from the detected fiducial, is used to reset the 20 bit pseudo-synchronous counter, and to reset the output flip-flops. TIMEOUT signals, the logical AND of the counters second and third most significant bits, provide the counter overflow information needed for the observation of missing fiducials. Eight 20 bit latches store the desired time of output pulse generation. Individual LATCH lines are provided for each channel, trading off the logic complexity of address decoding for additional package input pins.

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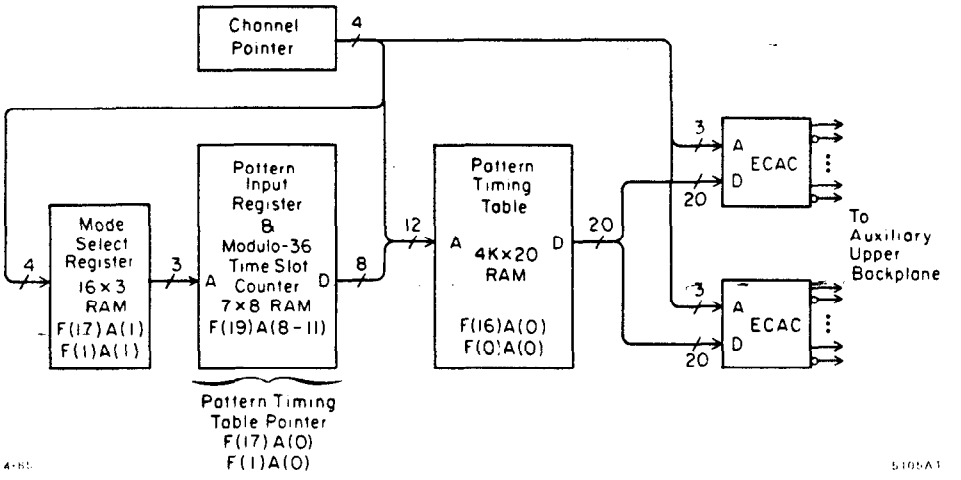

Fig. 2. Data Flow Diagram of the PDU II.

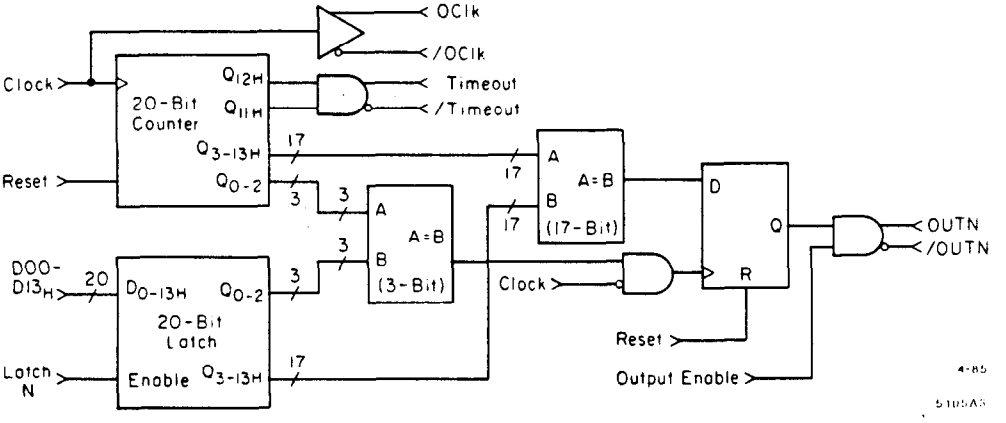

Fig. 3. Simplified Block Diagram of the ECAC.

The data stored in each 20 bit word of memory is simultaneously compared, on a bit by bit basis, to the outputs of the counter in a two stage process. An equal-to comparison of the three least significant bits generates a pulse once every eight clock cycles. This pulse train is used to clock the result of the comparison of the 17 most significant bits. The resulting eight clock cycle wide pulse, gated by a common OUTPUT ENABLE, is used to drive the upper backplane. This logical structure, analogous to a content addressable memory, allows the sharing of the complexity of counter circuitry among all channels, allowing a greater number of channels to be implemented.

A detailed block diagram of the counter is shown in Fig. 4. Settling time and carry look-ahead circuitry were traded off, producing a 20 bit counter out of 4-bit ripple counter sections. Testability of the chip was provided for by adding 5 additional inputs to the array, CANDH, which increments the counter while gating off subsequent clock transitions, and TEST1-TEST4, which increment ripple counter modules. These inputs are used to preload the counter after a reset, allowing the verification of device functionality with a compact test program.

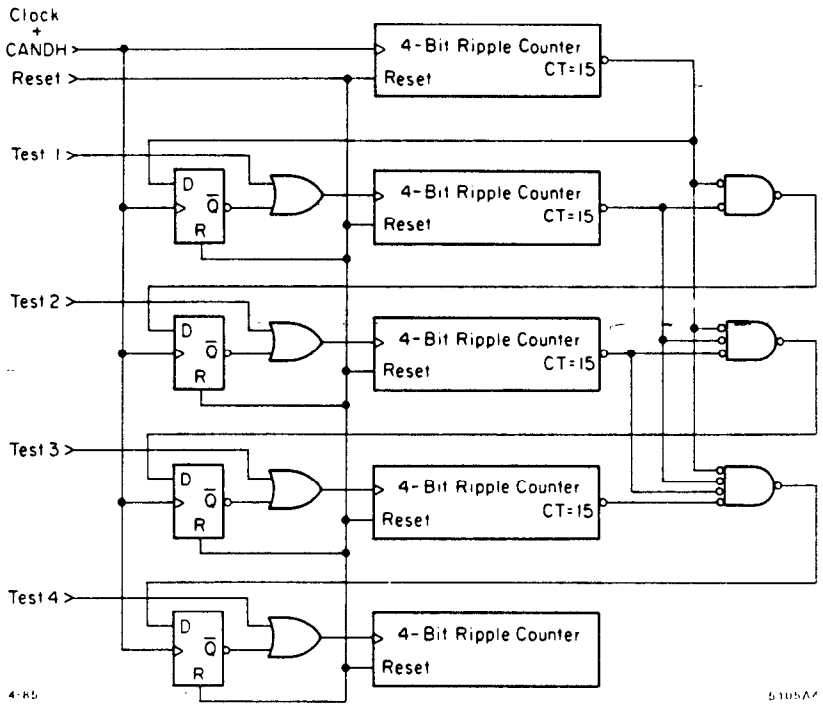

Fig. 4. Detail of the 20 – Bit Counter.

All ECAC inputs and outputs are ECL 10K compatible. No problems have been encountered with any of the prototype or production run parts. Typical current consumption is 1.2 A at -5.2 V, while bench testing revealed that the parts continued to function at voltages as low as -3.8 V. The module takes advantage of this and powers the chips at -4.2 V, lowering the power each ECAC must dissipate to 4.5 W. The total cost of the 400 production parts, including prototype development and non-recurring engineering (NRE) charges, was approximately $275 each.

REFERENCES

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