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A NEW TIMING SYSTEM FOR THE STANFORD LINEAR COLLIDER*

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Abstract

In order to be able to meet the goals of the Stanford Linear Collider, a much more precise timing system had to be implemented. This paper describes the specification and design of this system, and the results obtained from its use on 1/3 of the SLAC linac. The functions of various elements are described, and a programmable delay unit (PDU) is described in detail.

With the advent of the new Stanford Linear Collider (SLC), a new timing system had to be designed to meet much more stringent requirements than the old one.[1] To further complicate the issue, the new timing system has to coexist with the old one, since the new devices requiring the improved timing signals are being brought on line over a period of several years.

Figure 1 shows the SLC system and the overall design and performance of the Stanford Linear Collider Control System is discussed in a separate paper at this conference.[2] The new timing system is a subsystem within the overall control.

The specification of the new system was to provide timing signals with a precision of 2.1 ns, in increments of 8.4 ns with a jitter of less than 1 ns, and furthermore to have a multiplicity of these signals available at many locations.

In the linac, there are two lines which were considered for carrying the timing information, the main drive line (MDL) which carries the 476 MHz RF and the main trigger line (MTL) which carries two pulses on it for the old timing. Figure 2 shows schematically the two lines and the old trigger timing. Basically, the 360 Hz zero crossing, in coincidence with a submultiple of the 476 MHz, initiates two timing pulses, an early one known as t minus 1024, which allows early triggering of slow devices, and another pulse just before beam time to trigger klystrons. The timing signals are picked off at each sector and distributed by the sector trigger generator.

Because the MDL is temperature stabilized, the decision was made to use the MDL for the new timing by superimposing a fiducial on the 476 MHz as shown in Fig. 3 and using the 476 MHz as a frequency source for counting.

The repetition rate of the fiducial is 360 Hz. Figure 4 shows the logical derivation of the fiducial and of the old timing signals. The 360 Hz zero crossing is anded with 8.5 MHz, a submultiple of 476 MHz. 8.5 MHz was chosen because it is the damping ring revolution frequency. The anded signal is first resynchronized with 476 MHz, to produce the fiducial which is then superimposed on the 476 MHz. Also, this anded signal triggers the two timing signals required for the old system on the MTL.

The fiducial generator was designed by R. Koontz and G. Leger, the Master Trigger Generator and precision delays were designed by A. Wilmunder.[3]

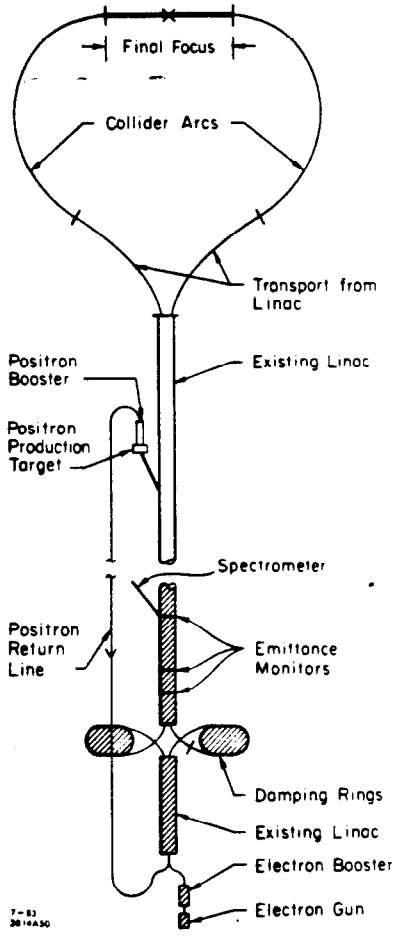

Fig. 1. The SLC System.

In order to be able to use this new fiducial, use was made of the fact that there already existed 30 couplers (1 per sector) on the MDL which pick off the 476 MHz for multiplication to 2856 MHz to the subboosters to drive the klystrons. An additional amplifier was provided at these points to provide a suitable signal for the fiducial detector (FIDO). See Fig. 5.

The FIDO, designed by E. Cisneros, performs several functions. It detects the fiducial by arming a zero crossing detector, and generates an internal signal of fixed length starting at the zero crossing of the fiducial. This signal is used to reset the divide by four counters. At the end of the reset, the counters resume. The outputs of the FIDO are at 119 MHz, with one pulse missing, at the time corresponding to the fiducial. This missing pulse is used by subsequent modules as their timing reference. Figure 6 is a logical block diagram of the FIDO and also shows timing details.

The FIDO provides a total of 6 outputs, 4 connected to one counter, two connected to another. The set of two outputs have

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the property that if an external device supplies a busy or active input, the counter is not reset by the fiducial pulse. The outputs of the FIDO are -32 mA, i.e., -1.6 V into 50 Ω.

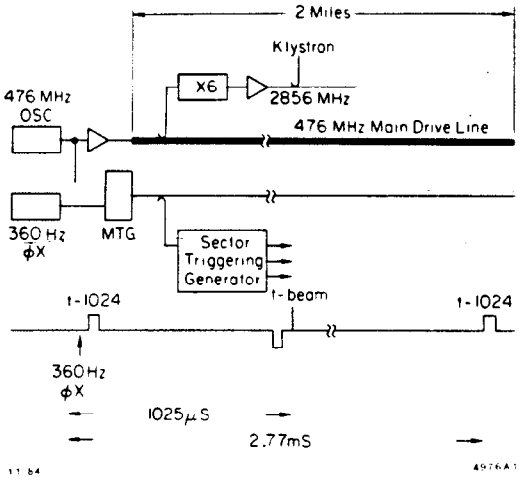

Fig. 2. A schematic diagram of the old timing system.

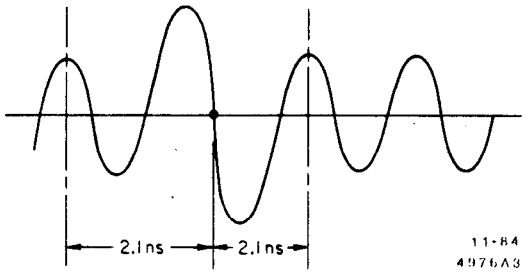

Fig. 3. The Fiducial superimposed on 476 MHz.

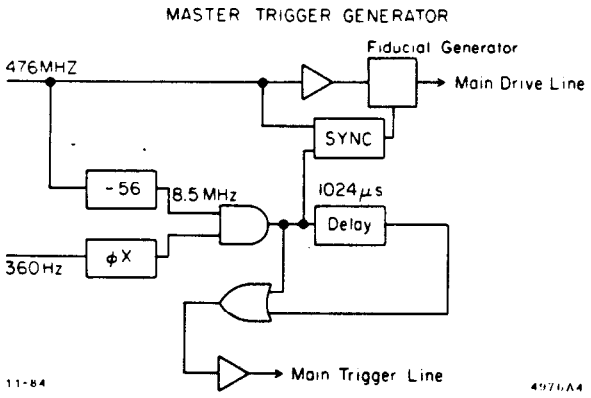

Fig. 4. The Fiducial and Timing generation.

The outputs of the FIDO are currently used by two CAMAC modules, the Programmable Delay Unit (PDU) and the Programmable Synchronization Unit (PSU). The PSU, designed by H. Kang, described in another paper[4] is used primarily at the damping rings where the ability to track individual bunches of electrons or positrons for longer than 2.7 ms is required. The PDU is used at every location where timing signals are required. The PDU specifications are as follows:

Input	:	119 MHz pulse train with missing pulse (from FIDO)
Outputs	:	16 Channel Differential ECL
	:	Pulse at end of programmed delay
	:	T_w = 67.2 ns (fixed)
	:	T_r, T_f = 1.5 ns
	:	Jitter < 1 ns
	:	Z_0 = Outputs drive 100 Ω terminated auxiliary backplane

Operationally, the delay (if programmed) occurs after the receipt of the fiducial. This delay is programmable in increments of 8.4 ns. The precision with respect to the MDL is 2.1 ns. The PDU may be programmed at any time during the interfiducial period. If any channel is programmed, the contents of a register is transferred to a counter just after the receipt of the fiducial. The counter starts counting and when the count is completed an output pulse is generated. A feature was incorporated called the "reuse" bit. This bit enables any particular channel to provide an output with some delay after every fiducial without having to continuously program that channel. Figure 7 is a logical block diagram of the PDU (only one channel is shown).

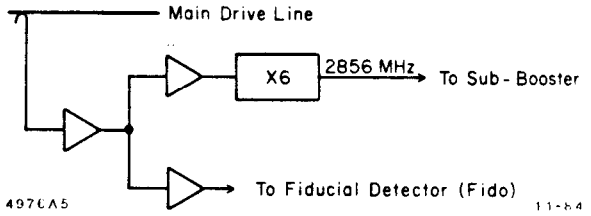

Fig. 5. MDL Pickoff and Drive for FIDO.

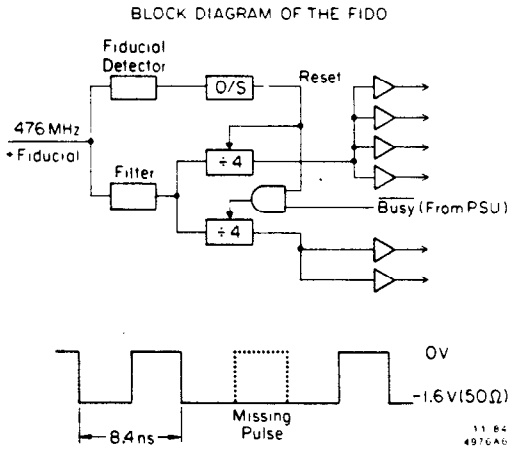

Fig. 6. Block diagram of FIDO and output timing.

The PDU distributes its 16 channels as differential ECL signals together with the 119 MHz on a special backplane within each CAMAC crate. Thus any module connected to this backplane may pick off any timing signal it requires. Examples of such modules are the beam position monitors, parallel I/O processors (for klystron control, and phase measurement).

For timing signals where the 8.4 ns increment is too crude, another module called the Vernier Delay Unit (VDU) was designed by W. Pierce.[5] The VDU provides the ability under pro-

gram control to delay two backplane PDU pulses or two external NIM pulses to be delayed in increments of 100 ps over a range of 10 ns.

Since the PDU only provides pulses of fixed width, a module called the Programmable Width Unit (PWU) was designed by W. Pierce to meet the needs of variable width pulses for some special applications. The PWU was designed to accept under program control either of two groups of 8 backplane signals, and provide from the front panel pulses of $n \times 8.4$ ns width where n ranges from 1 to 2^{20}. This module is currently being prototyped.

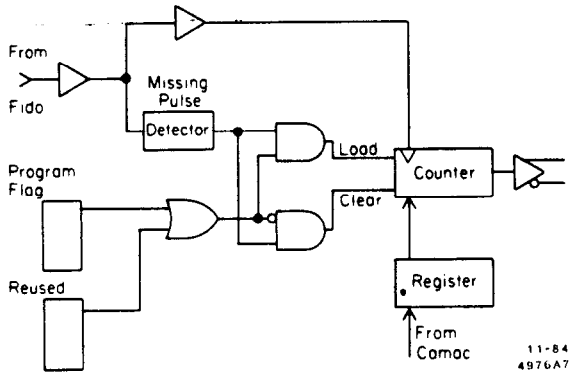

Fig. 7. Logical Diagram of one PDU channel.

Conclusion

The new Timing System was installed in the first ten sectors of the linac and at the injector and electron damping ring. The system has been operational for a year, and has met or exceeded all specifications. The timing jitter observed over a short time period is of the order of a few tens of ps. Work is continuing on the timing system, in particular the synchronization of the linac to PEP and SPEAR under the direction of M. Ross. Also a new and improved version of the PDU is being prototyped.

Acknowledgements

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References

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