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TRANSCEIVER FOR THE FASTBUS CABLE SEGMENT*

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Abstract

A 4 mA differential transceiver circuit which meets the Fastbus Standard is described in this paper. It is planned to hybridize this circuit for use in Fastbus Cable Segment devices.

Introduction

The Fastbus Cable Segment consists of 60 differential line pairs. Circuits which attach to it are differential current drives and differential line receivers whose specifications, taken from the Fastbus text, are shown in Table 1. The specifications for the receiver are written to satisfy the commercially available ECL 10114. But since no commercial integrated circuit meets the specifications of the driver, hybrid units (quad, 4 mA, 20 pin SIP) have been developed at CERN and at Fermilab.

The circuit described in this paper incorporates a 4 mA driver as well as a receiver and it is intended to be hybridized, 4 channels in a 20 pin DIP package.

Table 1

Driver's Specifications

- Differential current driver
- Wired OR capability (up to 32 devices)
- I ("1") $= 4 \pm 0.2$ mA
- I ("0") $\leq 40\,\mu$A
- $\Delta\ (I_{source} - I_{sink}) \leq 40\mu$A
- Common mode range $\geq \pm 3.0$ volts

Receiver's Specifications

- Differential line receiver
- $I_{input} \leq 100\,\mu$A
- $\Delta\ I_{inputs} \leq 10\,\mu$A
- Common mode range = +0.1 to −2.0 volts
- Terminating voltage = −0.9 volt

- Cable segment's characteristic impedance = 100 to 150 ohms
- FASTBUS power supplies' range:
  V_{CC} = +4.8 to +5.5
  V_{EE} = −4.8 to −5.7

The Basic Circuit

Figure 1 shows the basic block diagram of the transceiver.

The driver section is composed of a current source, a current sink and a current switch controlled by the driver input. In the quiescent state the current I from the source flows directly into the sink without affecting the equilibrium of the cable's differential line. When a logical "1" signal is applied to the input of the driver the direct source — sink connection is broken and the driver sources the current I into the "1" line ($L+$) of the differential pair of the cable and sinks an equal current I from the "0" line ($L-$), generating thus a differential voltage across the termination resistor of the differential line.

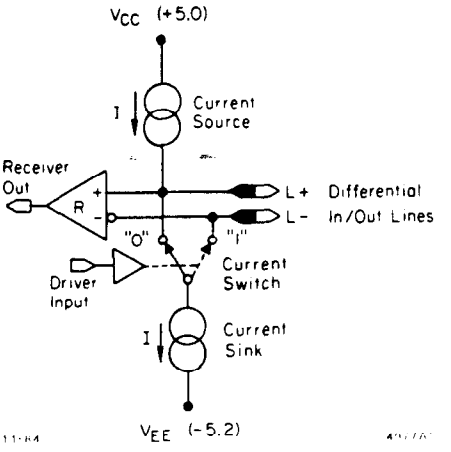

Fig. 1 Transceiver: block diagram.

The receiver senses the differential voltage signal of the lines and generates a standard logical output accordingly.

The basic circuit of the driver is illustrated in Figs. 2 and 3.

The Op-Amp and the external transistor make a simple, high quality current source or sink without the drawbacks of the current mirror approach (Early effect, V_{BE} offsets and their variations with temperature, matched-pair transistors, ...). V_1 is the reference voltage (common to all four channels); its value is fixed by the reference diode V_Z and the resistors R_1 and R_2. The voltage V_1 is set so that V_0 is very close to the supply voltage ($\Delta V \sim 400$ mV) so that a wide range of voltage compliance can be achieved.

For the circuit in Fig. 2 (current sink) we have:

$$V_1 = V_{EE} + V_Z \frac{R_1}{R_1 + R_2} \quad ;$$

$$V_0 = V_1 \quad ;$$

$$I = \frac{V_Z}{R_E} \frac{R_1}{R_1 + R_2}$$

For the current source (Fig. 3):

$$V_1 = V_{CC} - V_Z \frac{R_1}{R_1 + R_2} \quad ;$$

$$V_0 = V_{CC} - V_Z \frac{R_1}{R_1 + R_2} \left(1 - \frac{R_2}{R_1} \frac{R_a}{R_b}\right) \quad ;$$

$$I = \frac{V_Z}{R_E} \frac{R_1}{R_1 + R_2} \left(1 - \frac{R_2}{R_1} \frac{R_a}{R_b}\right)$$

where R_a ($R_a \gg R_E$) and R_b are needed in order to reach the 400 mV drop across R_E. In fact, while the input voltage of most Op-Amps can go as low as the negative supply, it has to remain about 1.5 volts lower than the positive supply to work properly. So V_1 cannot be set higher than $V_{CC} - 1.5$ or +3.5 volts, while V_0 should be set at about +4.6 volts.

For both circuits we can see that I is independent of either power supply and can be fine-tuned by the resistor R_E ($\sim 100\Omega$).

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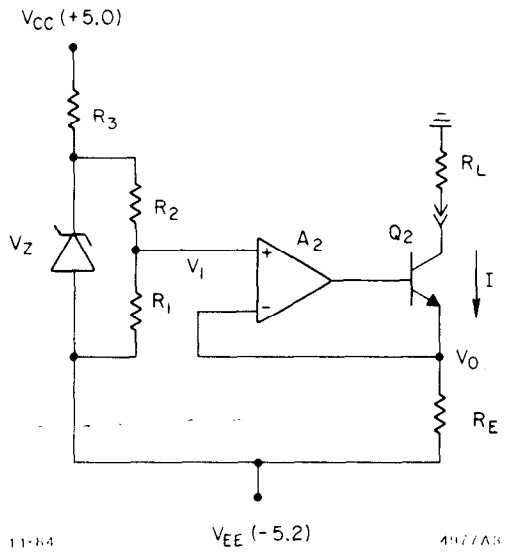

Fig. 2. Current sink circuitry.

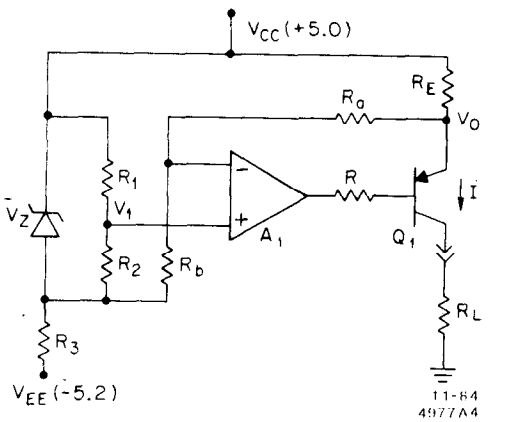

Fig. 3. Current source circuitry.

Of special importance for the stability of the circuit as a function of voltage and temperature, is the reference diode V_Z that sets V_1. A good inexpensive voltage reference has been obtained by using the 2N 3906 PNP transistor connected as a zener: *i.e.* the emitter-base junction biased in the reverse direction. The result can be seen in Photo A. The zener voltage of 6.8 is constant from 20 μA up to 20 mA and quite stable with temperature (25° C – 100° C).

Photos B and C show the I versus V curves of the current sink and source using the Op-Amp LM224 and the transistors 2N 3904 and 2N 3906 respectively.

The Transceiver

By combining current source and sink circuits together with a differential current switch we obtain the 4 mA current driver. Figure 4 shows the complete schematic of one channel of the ECL transceiver with the driver on the left side and the receiver on the right side.

In the driver the 2N 3904 has been replaced by the differential amplifier CA3102. Resistors have been added to obtain a better temperature coefficient. Adding the current switch has made the current sink circuit again dependent on the negative power supply. By lowering the bias voltage of the transistors Q_3 and Q_4 we get a wider common mode (compliance) range, but the circuit becomes more dependent on the supply voltage. By raising it we lose in compliance range. A compromise was reached by having both lower-limit-common mode and negative-supply independence set at −4.0 volts.

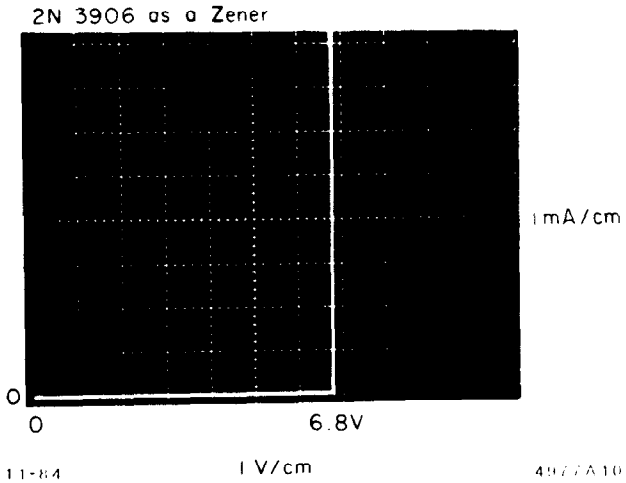

Photo A. 2N 3906 as a Zener.

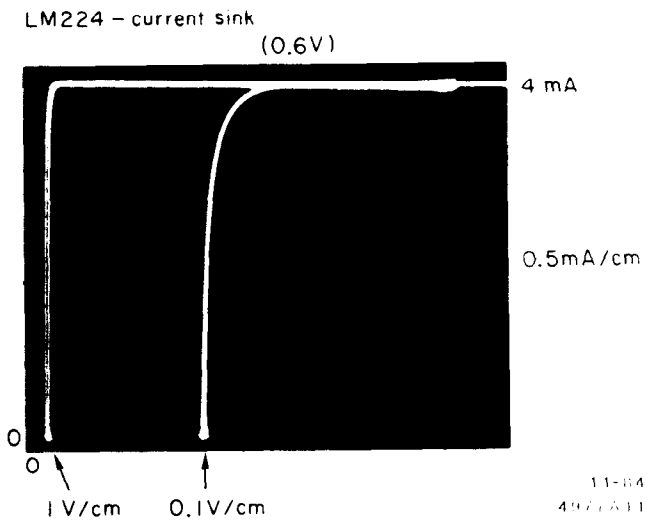

Photo B. LM224 – current sink

The current I is determined by the two resistors R_E. The requirement for I is 4 mA ± 10% (see Table 1); by selecting one R_E resistor with 1% tolerance (10 times better than the requirement) we have only one parameter to vary in order to obtain a very low leakage current. By fine-tuning the other R_E we were able to match source and sink currents and set I ("0") at less than 1 μA at ambient temperature.

The receiver is a modified version of the front end of the 75107 type differential receiver. The transistors are the CA3086, for the zeners the 2N 3906 is used again here and the output is modified to generate ECL positive logic. The current mirror (Q_1', Q_2', Q_3') sets the current source of the long-tail pair at 0.7 mA, so that the input current of the receiver is 7 μA typical, with an input imbalance of 2 μA maximum. Common mode

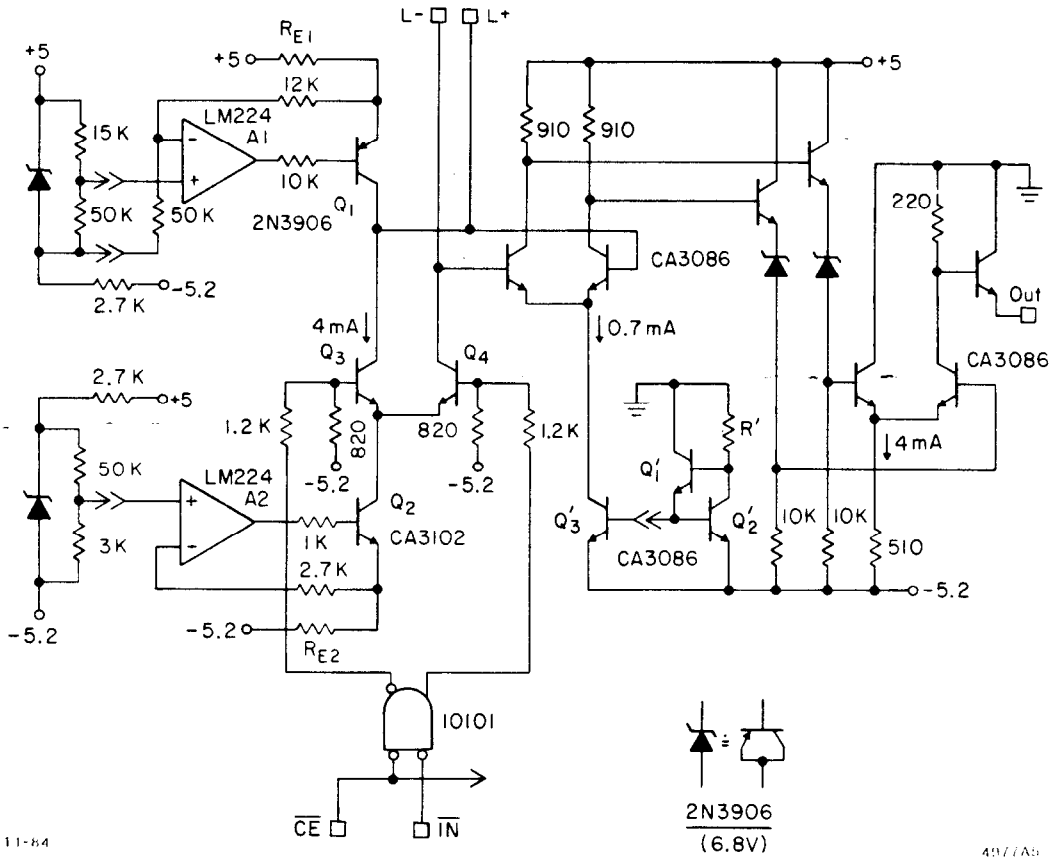

Fig. 4. ECL differential transceiver.

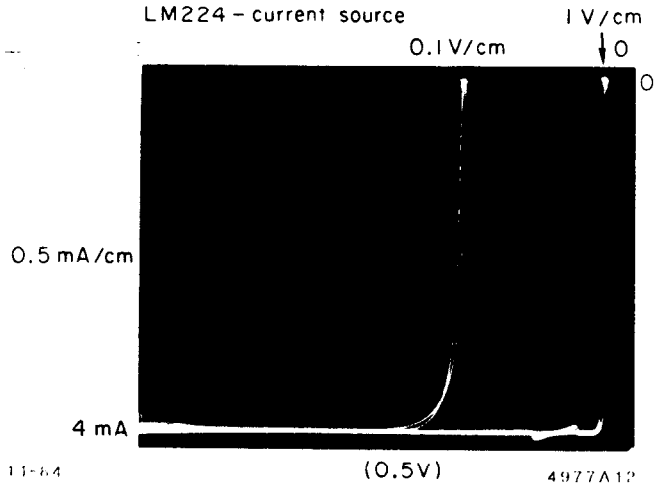

Photo C. LM224 – current source

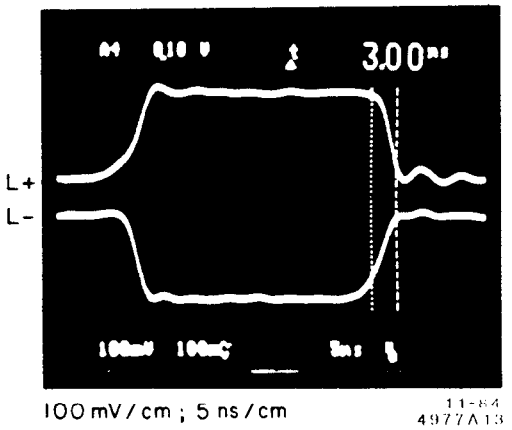

Photo D.

voltage range is ±4.0 volts. This symmetry around zero would also permit the use of 0 voltage (ground) as the terminating voltage (V_{term}) at one end of the cable segment.

Photo D shows the differential signals from the driver across a 50Ω load. Photo E shows an input signal at the driver and the output from the receiver.

Table 2 summarizes the characteristics of this ECL differential transceiver.

Table 2

Driver's Characteristics

- 4 mA Differential driver
- Sink–source current imbalance better than 1 μA
- I("0") better than 1 μA
- Common mode range: +4.25 to −4.00 volt
- Power supply independence:
- Lower limit = +1.8 volt; −4.00 volt
- Upper limit = better than ±10 volt
- Propagation delay = 5 nsec
- Rise and Fall time < 3 nsec

Receiver's Characteristics

- Differential line receiver
- $I_{input} \sim 7\,\mu$A
- Output Rise and Fall time ~ 3 nsec
- Propagation delay time ~ 12 nsec
- Common mode range: ±4.00 volts
- V_{term} = 0 volt

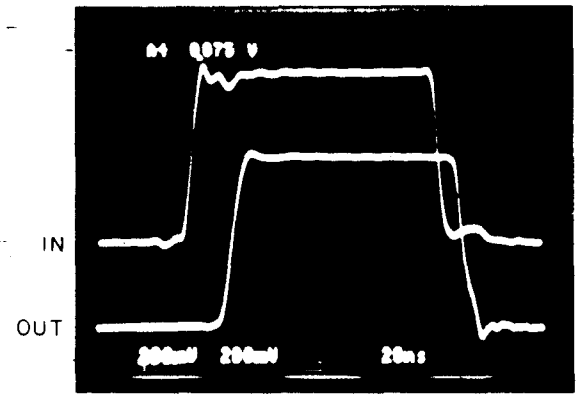

Photo E

Figure 5 is the schematic of the TTL version of the same transceiver. The only differences from the ECL version are the 10124 TTL to ECL translator and the 75107 receiver.

Conclusion

Although a complete temperature test has not been made at this time, partial tests show good stability over a wide temperature range.

The calculated power dissipation of the ECL version (four circuits) is approximately 700 mW, for the TTL version about 1 W.

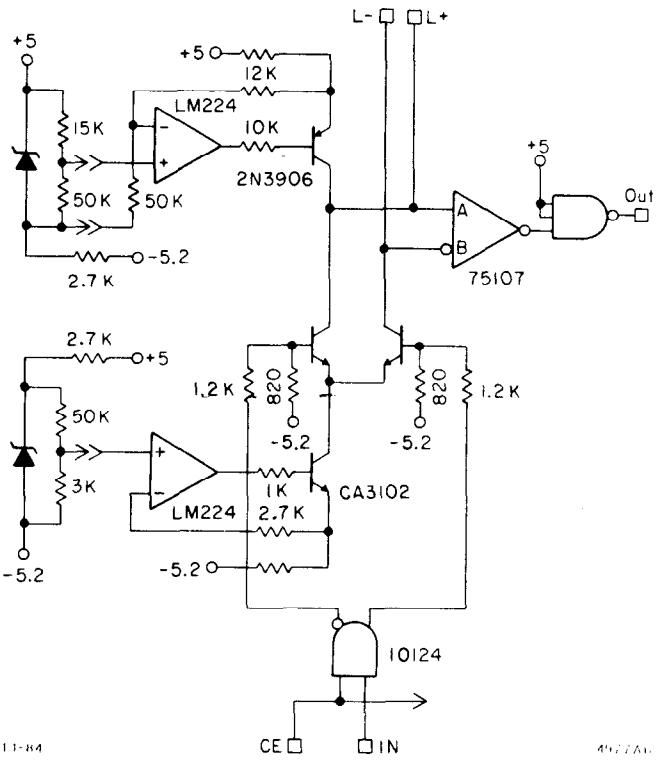

Fig. 5. TTL Differential Transceiver

The plan is to hybridize these two circuits as quad transceivers in dual in line 20-pin packages.

A driver scheme, where a second current switch is added to the current source, has been studied. It has the advantage of zero leakage current in the quiescent state at any temperature and the disadvantage of more components involved. Though not practical for a hybrid version, this configuration which does not require fine-tuning any part, is more suitable for a monolithic or a gate array version of the transceiver.

Acknowledgements

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