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FASTBUS REVIEW 1984*

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Abstract

The first year of work with the FASTBUS Specification DOE/ER-0189 for modular high speed data acquisition and control systems is reviewed. FASTBUS system components such as crates, power supplies, modules, and diagnostic tools available from research laboratories and industry in North America and Japan are summarized. New developments and future plans for applications and products are highlighted.

European progress on FASTBUS and review of software activities are presented in other papers at this Conference.[1,2,3] Relevant background information may be found in the FASTBUS status report presented at the 1983 Nuclear Science Symposium.[4]

The FASTBUS Standard

The FASTBUS Specification, developed by the U.S. NIM Committee in collaboration with representatives from Canada and Europe (ESONE), has been published by the U.S. Department of Energy as report DOE/ER-0189, December 1983, and was distributed in March 1984.[5] In June 1984 FASTBUS was approved as IEEE Standard 960-1984 with public distribution expected during 1985. The specification has also been submitted to the American National Standards Institute (ANSI) and the International Electrical Commission (IEC) for comment and processing.

Report DOE/ER-0189 has been updated by the Addenda and Errata dated September 1984. This included changes in the definition and assignment of geographical addresses to accommodate Segment Extender modules (SE) and some changes to Operation Passing for Segment Interconnects (SIs) in Section 10.

Tutorial short courses on the FASTBUS Specifications have been offered at the Nuclear Science Symposium in October 1983 and at Fermilab in December 1983. FASTBUS news information is available to interested parties from the U.S. NIM Committee.[6]

FASTBUS Hardware Summary

To FASTBUS system architects and implementers the ready availability of system building blocks is a first-order concern. Many FASTBUS developments reported on a year ago at NSS 1983 have yielded hardware items which are available today as commercial products from industry or as design documentation packages from laboratories or universities. In the Appendix an attempt is made to summarise available FASTBUS components in functional categories. All items included are available now or are expected to be ready in one to two months. For completeness in respect to commercially available products, we have included in this listing FASTBUS hardware from a West German manufacturer.

News from Laboratories

FASTBUS applications and research and development efforts at laboratories and universities are summarised.

1. BNL - Brookhaven National Laboratory

   (a) Experiment E780

   This experiment expects to utilise the early FASTBUS prototype system (specification incompatible) from E749 with water-cooled crates and modules.

   (b) MPS II - Multi-Particle Spectrometer

   A new single crate system for 17K channels with LRS1821 SM/I interface to VAX-750 host is being assembled.

   (c) Experiment E787

   Scheduled to run late in 1986, this experiment is considering the use of LRS ADCs and TDCs. They have a LRS 1805 starter kit in use for development work.

2. Cornell University Medical College

   This data acquisition system for imaging coronary arteries has been improved and expanded during the past year.[7]

3. FNAL - Fermi National Accelerator Laboratory

   (a) CDF - Collider Detector Facility

   The data acquisition system for this detector will process 75K signal channels and utilise 50 FASTBUS crates and six cable segments with 50 SI modules. Prototype development for most system components has been completed; some hardware production is in progress. The phased installation schedule extends from November 1984 to October 1986.

   (b) Experiment E636

   One crate of LRS 1879 TDCs and a LRS 1821 SM/I interface planned for January 1985.

   (c) Experiment E653

   Installation of 11 crate system to commence by February 1985. LeCroy hardware to be used includes 1821 SM/I interface, 1879 TDCs, 1885 ADCs, 1891 MEB Memory.

   (d) Experiment E665

   Testing of three crates with LeCroy 1821 SM/I interface, and 1885 ADCs scheduled to start by March 1985.

   (e) Experiment E687

   Testing of four crates with UPI interface, LRS 1885 ADCs, and UI Dual Port Memories expected to start by January 1985

* Work supported by the Department of Energy, contract DE-AC03-76SF00515.

Invited talk presented at the Nuclear Science Symposium, Orlando, Florida, October 31–November 2, 1984.

4. UI - University of Illinois

(a) Rack Cooling System

Development of rack for 3 air cooled crates, power supplies, water heat exchangers for 10 kW, and microprocessor interlock and monitor system. A prototype rack system is being tested. Design is under consideration for SLD at SLAC and CDF at FNAL.

(b) FASTBUS to Ethernet Interface

A simple interface has been developed.[8]

(c) FASTBUS Slave Interface with PALs

Collaboration with CERN to develop a standard slave protocol control utilising PALs and hybrid packaging.[9]

5. University of Wisconsin

Multihit Time-to-Digital Converter packaged as 96-channel FASTBUS module is under development. A prototype has been tested and a multiwire unit is now being built.

6. LANL - Los Alamos National Laboratory

(a) Single-Board 32-Bit Computer for FASTBUS

A general-purpose master module based on NS32032 CPU with 4 MByte memory is being developed. A complete wirewrap prototype will be fabricated and tested early in 1985.[10]

(b) WNR Data Acquisition

For neutron TOF measurements, single crate data acquisition stations with MicroVAX, UPI, and custom modules are being developed.[11] Custom module design is being done by SSI, Los Alamos. Testing of a prototype station is scheduled for March 1985.

7. LBL - Lawrence Berkeley Laboratory

At present two FASTBUS crates with a complement of modules are in use for development work.

(a) In collaboration with FNAL a readout system for CDF is under development. The system will contain LRS 1879 TDCs and SLAC SSPs and will be installed in 1986.

8. SLAC - Stanford Linear Accelerator Center

The Stanford Linear Collider (SLC) presently under construction (Figure 1) provides the motivation for two detector projects, which will utilize FASTBUS: the Mark II/SLC and the SLD Detectors.

(a) General Developments

PC artwork for the *Snoop Diagnostic Module* has been completed including the 68000 processor section. Fabrication of five new prototype modules is in progress.[12] A *hybrid transceiver* for the cable segment interface is being developed.[13] A latched *Bus Display Module* prototype for crate segments has been built. A display option for the cable segment is being planned. A FASTBUS dual cable port *interface for the 9081/E* processor is in development.

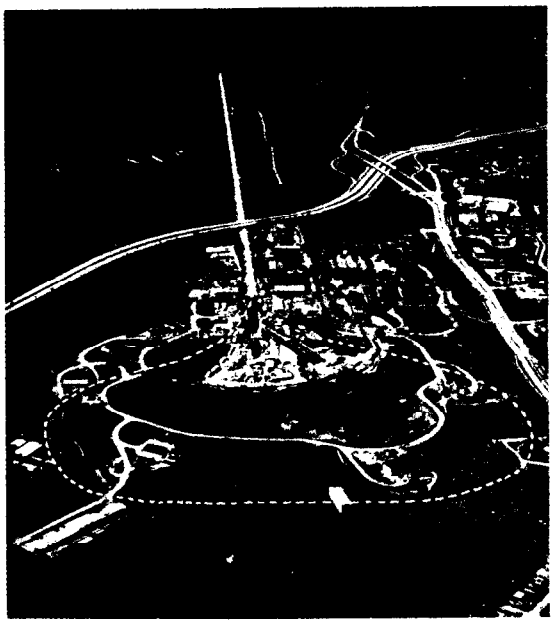

Figure 1. SLAC with Stanford Linear Collider

(f) Mark II/SLC Upgrade Data Acquisition System

Upgrading work for this detector is well underway with test runs using cosmic rays and PEP beams scheduled to start in April 1985. Eventually this system will have 20K signal channels requiring approximately 25 crate segments.

- Drift Chamber Front-End Electronics[14] have been developed with 24 channel postamplifiers packaged on FASTBUS boards and housed in 12 FASTBUS crates mounted on the detector magnet (Figure 2).
- SSP - SLAC Scanner Processor[15] master module has been designed for crate-level readout and processing of TDC and FADC data. Several wirewrap prototypes are in testing.
- Trigger Card for LRS 1879 TDC is a 96 channel programmable trigger logic card which connects to a LRS 1879 TDC via the FASTBUS auxiliary connector (Figure 3). Production quantities of this card have been fabricated and tested.
- FADC Module is under development. A prototype of this 16-channel, 100MHz, 6-bit design is expected by 12/84.

(g) SLD Detector

Construction of this new detector for the SLAC Linear Collider (SLC) is planned from 1985 to 1989. Based on the SLD design report (July 1984), this detector will have 215K signal channels requiring a data acquisition system of 81 crates and 8 cable segments (Figure 4 and Table 1). Extensive use of monolithic VLSI circuits and hybrid packaging is envisaged.

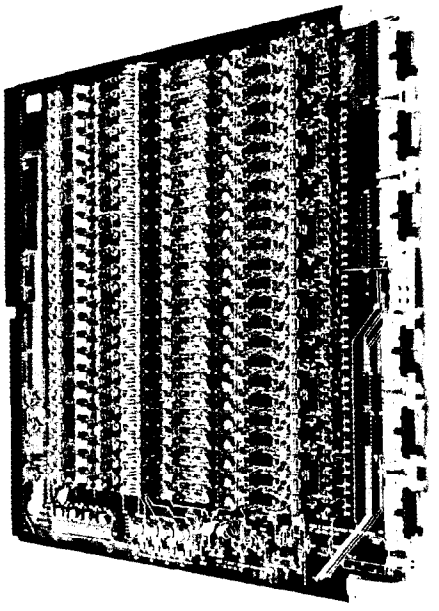

Figure 2. Mark II/SLC Drift Chamber Postamplifier Module

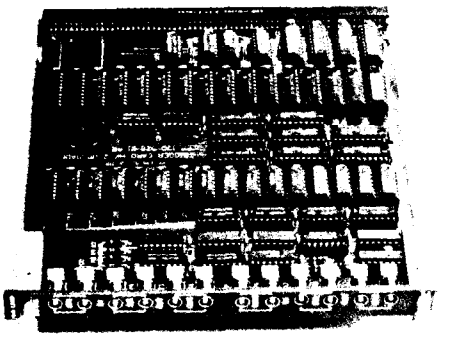

Figure 3 Mark II/SLC Trigger Logic Card

Table 1

System	N Channel	N Boards	N Crates
CCD Vertex	220	165	7
Drift Chambers	14K	212	10
CRID	33K	516	24
LAC	46K	720	32
WIC Pads	10K	154	7
WIC Strips	111K	12	1
Totals	215K	1779	81

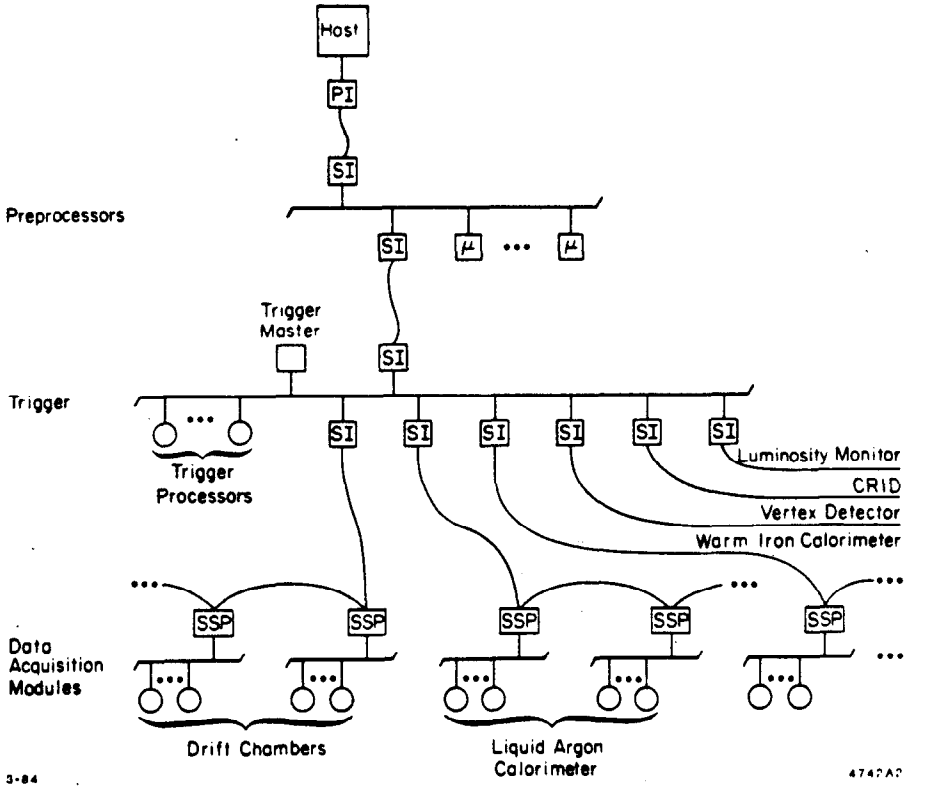

Figure 4. SLD Data Acquisition System

- AMU Analog Memory Unit[16,17]

  A custom VLSI analog memory chip has been developed and tested. An 8-chip hybrid prototype is in testing.

- CDM Analog Memory

  Samples of a VLSI monolithic memory chip to be used for the Calorimetry Data Module are expected by 11/84.

9. TRIUMF Laboratory, Vancouver, Canada

   (a) Technical editing of FASTBUS Standard Routines Specification.

   (b) FASTBUS interface gate array IC set based on LS TTL. Detail design for a 16-bit ADI unit is ready.[18]

10. KEK National Laboratory, Japan

    Three detector facilities for the TRISTAN intersecting storage ring will use FASTBUS data acquisition systems.

    TOPAZ (50 crates), VENUS (25 crates), AMY (22 crates). All three systems will utilise DEC VAX-FPIs, LRS 1821 SM/I interfaces, 1885 ADCs, and 1810 CAT modules. The AMY detector will also use LRS 1878/79 TDCs and 1891 Memories.

    Various prototype components are presently in development:

    - For VENUS: TAC, ADC, Track Finder, Trigger Decision Modules.
    - For TOPAZ: Sector Sequencer and Digitiser Modules.
    - KEK FASTBUS crate and front-insertion ancillary logic.
    - FASTBUS interface to TKO front-end bus.
    - 32-bit I/O Register Modules.

11. IHEP Institute of High Energy Physics, Beijing, China

    IHEP is acquiring a FASTBUS development system for laboratory R&D work. A Chinese translation of the FASTBUS Specification has been completed and is ready for publication.

Future Products From Industry

Plans for future FASTBUS products from industry are summarized.

1. KSC Kinetic Systems Corporation, Lockport, IL

   KSC is planning a passive extender module, a Segment Interconnect Type S1, a low-current power supply package, and a multicrate rack with cooling.

2. LRS LeCroy Research Systems Corporation, Spring Valley, NY

   Planned are development of the 1861/62 ICA and start of production of the 1891 memory module.

3. NYBC Real-Time Computing, Port Washington, NY

   Development of a Micro-VAX master module prototype with software. Prototype to be operational by 2/86.

4. SSI Scientific Systems International, Los Alamos, NM

   Development of Segment Extender (SE) module. Production and sale of module expected from KSC by late 1985.

5. WDS White Data Systems, Union, OR

   Future products are an active extender module, a rack with cooling, a FASTBUS starter kit.

Summary

The first year of FASTBUS as a DOE specification and as an approved IEEE Standard seems to have been a successful one. This is evident from the substantial number of applications being implemented or planned for the next several years. This is also evident from the increase in commercially available FASTBUS building blocks.

The year 1985 will be a crucial year for FASTBUS. It is hoped that several of the larger FASTBUS data acquisition systems such as CDF at FNAL and Mark II/SLC at SLAC will succeed in becoming operational and thereby bring proof of the suitability of FASTBUS as a specification for large systems.

Acknowledgements

The efforts of representatives from all the laboratories, universities, and commercial enterprises to provide the information for this report is warmly acknowledged. A special thank-you goes to R. S. Larsen and E. Barsotti for their encouragement.

References

1. P. J. Ponting, *"European Progress on FASTBUS,"* invited paper 6A8, this Conference.
2. D. B. Gustavson, *"FASTBUS Software Progress,"* invited paper 3B1, this Conference, SLAC–PUB–3511.
3. E. M. Rimmer, *"FASTBUS Software in Europe,"* invited paper 3B2, this Conference.
4. H. V. Wals, *"Review of Recent FASTBUS Developments,"* IEEE Trans. on Nucl. Sci. *NS-31,* No. 1, 205 (1984).
5. DOE/ER-0189, *"FASTBUS Modular High Speed Data Acquisition and Control System for High Energy Physics and Other Applications,"* U.S. NIM Committee, December 1983; available from the National Technical Information Service, U.S. Department of Commerce, Springfield, VA 22161.
6. L. Costrell, Chairman NIM Committee, NBS, Washington D.C. 20234.
7. E. J. Siskind *et al., "New Features of a FASTBUS Based Data Acquisition System for Imaging Coronary Arteries,"* paper 4B13, this Conference.
8. R. W. Dobinson *et al., "A Simple FASTBUS to Ethernet Link,"* paper 4B12, this Conference.
9. L. Pregernig and R. W. Downing, *"Using PALs to Simplify FASTBUS Slave Interfaces,"* paper 5B3, this Conference.
10. R. Kellner *et al., "Single-Board 32-Bit Computer for the FASTBUS,"* paper 4B9, this Conference.
11. R. O. Nelson *et al., "FASTBUS Data Acquisition System for Neutron Time-of-Flight Measurements,"* paper 6A3, this Conference.

12. H. V. Walz and D. B. Gustavson, *"Status of the SLAC Snoop Diagnostic Module for FASTBUS,"* IEEE Trans. on Nucl. Sci. *NS-30,* No. 4, 2276 (1983).

13. B. Bertolucci, *"Transceiver for the FASTBUS Cable Segment,"* paper 5B4, this Conference, SLAC-PUB-3488.

14. D. Hutchinson *et al., "The SLAC Mark II Upgrade Drift Chamber Front-End Electronics,"* paper 3D10, this Conference, SLAC-PUB-3491.

15. A. J. Lankford *et al., "The SLAC Scanner Processor: A FASTBUS Module for Data Collection and Processing,"* paper 6A9, this Conference, SLAC-PUB-3471.

16. J. T. Walker *et al., "Microstore - An IC Analog Memory Unit,"* invited paper 3D1, this Conference, SLAC-PUB-3503.

17. D. Freytag and J. T. Walker, *"Performance Report for the Stanford/SLAC Microstore Analog Memory Unit,"* invited paper 3D2, this Conference, SLAC-PUB-3455.

18. R. Skegg, *"A General Purpose FASTBUS Interface Chip Set,"* paper 4B14, this Conference.

Appendix

FASTBUS HARDWARE SUMMARY NOVEMBER 1984

1. Crates: WDS, KSC F050, STR 101/102
2. Power Supplies: WDS, Low Current-SLAC, STR 101/102
3. Cooling: WDS 8152 Blower, STR 101/102
4. Crate Ancillary Logic:

   KSC F151/152 (SLAC), WDS 8183, STR 162/163, KEK ATC/GAC, KSC F150 Terminator
5. Cable Ancillary Logic & Terminator:

   UI Wirewrap, FNAL PC Proto
6. Segment Interconnect Module SI:

   UI Wirewrap S-1, Maruei Shoji Simplex SI (KEK)
7. Processor Interface PI:

   IORFI (FNAL) : BiRa 9882-2, LRS 1822
   FIORI (CERN) : STR 164
   UPI (FNAL) : KSC
   VAX-FPI (KEK): DEC Japan
   CCP-FPI (KEK): Housin Electronics
   Segment Management and Interface LRS 1821 SM/I
   CFI (CERN) : STR
8. Master Modules, General Purpose:

   SFC with Multibus MPU: SLAC
   68K-FPI (KEK): Maruei Shoji
9. Slave Modules, General Purpose:

   KSC F400 - TRIAC, LRS 1882/85 ADC,
   LRS 1878/79 TDC, LRS 1810 CAT,
   STR 136-137 IO Modules,
   STR 146-147 RAM Modules,
   Transiac FB 2064 DVM,
   UI Dual Port 2 MByte Memory
10. Diagnostic Bus Displays

    FDM (FNAL): BiRa, WDS
    FB Monitor (CERN): STR 160
    FDM Diagnostic & Display (CERN): STR 161
    Bus Display (KEK): Housin Electronics
    Switch & Display (KEK): Housin Electronics
11. Crate Extender Modules

    Passive Extender: SLAC, WDS
    Active Extender:

    KSC F210 (FNAL), LRS 1801, STR 178 (CERN)
12. Development Support

    Memory Modules:

    SLAC PRIMO ECL, FNAL Test Memory, 256 W Memory (KEK) Housin Electronics

    SLAC ECL Sequencer, SLAC Manual Test Box, SLAC Lightbar Display
13. Kluge Boards (Layers)

    KSC F010 (2), KSC F011 (4), WDS (2), WDS (5), STR 144, STR 159, KEK (4)
14. Starter Kits

    LRS 1805: 1822 IORFI, 2891 CAMAC IO, CABLE, Software; CERN Starter Kit from Struck
15. Special ICs and Hybrids

    Cable Quad Hybrid Driver:

    Philips-Elcoma (CERN), FNAL, KEK-NACL

    AD Interface Gate Array, 8-Bit Slice, ECL:

    FMA 601 Maruei Shoji (KEK)

Note: From Europe only commercial products are included. For laboratory developments see Reference 1.

Commercial Enterprises:

BiRa Systems, Inc., Albuquerque, NM, USA

KSC Kinetic Systems Corporation, Lockport, IL, USA

LRS LeCroy Research Systems Corp., Spring Valley, NY, USA

Transiac, Mountain View, CA, USA

WDS White Data Systems, Union, OR, USA

Philips-Elcoma, Zurich, Switzerland

STR Struck, Tangstedt/Hamburg, West Germany

DEC Japan Digital Equipment Corporation, Japan

Housin Electronics, Japan

Maruei Shoji Corporation, Ltd., Japan

NACL Nippon Avionics Corporation, Ltd., Japan