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CAD/CAM AND NEW DESIGN TECHNOLOGIES IN HIGH ENERGY PHYSICS ELECTRONICS APPLICATIONS*

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Abstract

In the past few years, several significant new technologies related to electronics design, fabrication and testing, appear to have reached a level of maturity which makes them ripe for exploitation by high energy physics laboratories. This paper will review recent developments and trends, and will draw particularly from some examples at Stanford Linear Accelerator Center. Cost benefits as well as difficulties of implementing new technologies into relatively small laboratories will be examined.

1. Introduction

The advancement of the basic science of experimental high energy physics over the past two decades has been greatly aided by spectacular advancements in the state-of-the-art of electronics. These advancements are most evident in the development of increasingly sophisticated and powerful electronic particle detectors encompassing a variety of classical techniques- -calorimetry, time-of-flight, Cerenkov radiation, and multiwire tracking chambers. Whereas twenty years ago almost all high energy physics experiments involved fixed targets and limited solid angle coverage of the experimental region by perhaps a few hundred channels of scintillation hodoscope and/or photographic spark chamber or bubble chamber apparatus, the newest detectors under construction today achieve close to 100% solid angle coverage of a colliding beam interaction region by detection and data acquisition systems comprising more than 100,000 electronic channels.

As the Institute of Electrical and Electronics Engineers, principal sponsors of this Symposium, enters its 101st year of existence, it is appropriate to focus on the contribution of electronics technologies to the field of high energy physics, and to look to future developments which promise to be at least as exciting and productive as those of the past two decades. In this brief summary, we describe some developments which are particular to SLAC, but which are intended to be illustrative of developments in the field as a whole.

2. The Past Two Decades

The past 20 (or perhaps 25) years of electronics perhaps can be summarized graphically by the use of a photograph (Fig. 1). The device on the left is probably not recognizable by some of our younger engineers. This vacuum tube device could be configured either as a high gain operational amplifier, or as a dual flip-flop. It required a few hundred volts and a few 10's of milliamps, plus heater currents, which made the entire assembly rather warm to the touch (20-30 watts consumption). The analog and digital computers of the late 1950's used these devices as basic building blocks. At that time, most particle physics "counting" experiments used a special tube known as a Decatron which had a visual readout; later counters employed tubes with illuminated decade numbers (NIXIE's). However, data were recorded and entered into calculations manually.

A decade later (late 1960's), many advances were evident, as illustrated by the second device in Fig. 1. This single channel 8-bit ADC with a fast gated input was a major advance, but was used sparingly because of its cost ($ 800). A companion TDC was also available. In addition to high speed discrete transistor and small scale integrated circuit technology which made this complex circuit possible in such a small package, note also that a packaging standard (Nuclear Instrument Module, or NIM) had been adopted to promote interchangeability of modular instruments among vendors and various laboratories, a development which greatly aided the sharing of resources among High Energy and other Laboratories.

As a rough comparison, it would have taken about 20 of the vacuum tube units to build the equivalent of this circuit, at roughly a X5 greater cost, and X10 greater space and power requirements.

Less than a decade later (mid 70's), techniques had evolved as shown in the next device. Two versions of this device served to perform the ADC and TDC functions of the previous NIM modules. (Not shown is the double width ADC module which served to process data from these front end modules; this added a small fractional cost and space overhead.) The major advances represented by this device were that the spatial density was improved by two orders of magnitude over the NIM module (128:1); per-channel cost was reduced by a factor of 20-30; and a new modular standard with a built-in computer data bus, CAMAC, had been firmly established.

The modules shown are capable of processing only one event, or "hit", at a time; although multi-hit versions of these modules were made, density was reduced and per channel cost was proportionately higher.

In recent years, more emphasis has been placed on the ability to record events over the entire live time (drift time) of the detector apparatus, leading to the development of electronics with multiple-hit capabilities. This has led to the use of new integrated circuit techniques such as CCD's (as used in time-projection chambers), SOS shift registers (as used in the newest commercial TDC systems), etc. In essence, such measurements require much higher numbers of memory cells, (analog or digital) per channel, and place a much higher burden on the memory storage and pre-processing sections of the data acquisiton system.

The fourth device shown in Fig. 1 represents a very recent development, approximately 25 years from the initial vacuum tube device discussed. The device is barely visible since it is an unpackaged 5mm x 5mm VLSI chip. Fig 2 shows a 4" x 1" hybrid test package containing 8 of these devices. Each chip contains 256 analog memory cells together with write and read address logic and multiplexing. By way of comparison, each chip

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is functionally equivalent to 8 of the 32 channel CAMAC modules shown in Fig. 1, such that the entire hybrid is functionally equivalent to 64 such modules, or 3 full CAMAC crates. The unpackaged chip costs less than $ 5.00, and the packaged version will cost under $ 10.00 per chip.

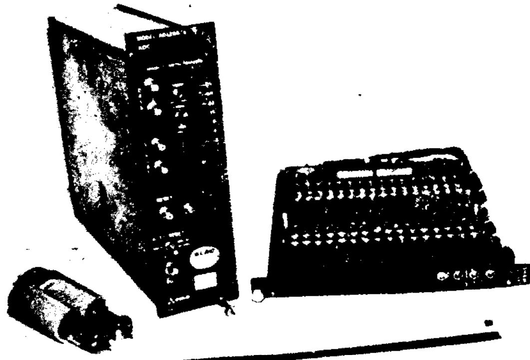

Fig. 1. 2 decades of electronics development.

Fig. 2. Hybrid package with 8 VLSI chips.

A rough comparison of size, power consumption and cost, assuming packaging in a functional module, normalized to the first device shown, is as follows:

Year	Device	Per Ch* Volume	Per Ch* Pwr Cons.	Per Ch* Cost
<1960	Philbrick K2	1	1	1
1966	EGG TDC/ADC	1/10	1/10	1/5
1974	CAMAC TAC/SHAM	1/1000	1/1000	1/100
1984	AMU Chip**	1/20,000	1/20,000	1/20,000

* Per channel (or per function) cost assumes one ADC channel equivalent.

**Assuming 64 Ch/FB module or 25 Ch/CAMAC equivalent.

In addition to improved per channel volume, power and cost profiles, it should be noted that the newer technologies offer improved performance in both dynamic range and speed.

3. Current Technologies and Trends

There are several inter-related developments which have contributed tc the development of improved systems in high energy physics; these are listed, in no particular order, as follows:

I. Design Capabilities:
  (a) Circuit design using SSI, MSI, LSI and VLSI technologies.
  (b) Multilayer circuit board design.
  (c) Hybrid integrated circuit design.
  (d) Programmable logic (firmware) design.
  (e) Gate array or standard cell custom IC design
  (f) Full custom IC design-NMOS, CMOS, Bipolar, SOS, GaAs, etc.

II. Design Tools:
  (a) CAD Schematic Drafting and Printed Circuit Design Systems.
  (b) CAD Hybrid Circuit Design
  (c) CAD Integrated Circuit Design Systems
  (d) Circuit and logic software simulation (SPICE, TEGAS, etc.)
  (e) Firmware Logic design software/hardware
  (f) NC automated tool path generation.
  (g) CAD cable harness and cable plant design

III. Manufacturing Tools:
  (a) Multilayer board lamination press
  (b) NC precision high speed drill
  (c) Thick film and thin film hybrid processing/packaging (automated placement, bonding, component laser trim, and testing).
  (d) Gate array custom metallization process
  (e) Custom silicon wafer fabrication.

IV. Testing Tools:
  (a) Commercial Programmable testers (eg. μ P's, GPIB hardware and software)
  (b) Custom modular test hardware and software (eg. μ P and CAMAC or FASTBUS standard interfaces)
  (c) Automatic Test Equipment (ATE) for production testing or maintenance
  (d) System diagnostics techniques (eg. diagnostic LAN's)
  (e) Self-diagnostics at chip and board levels

V. Packaging and Interconnect Tools:
  (a) Custom IC and hybrid packaging
  (b) Leadless frame and surface mount technologies
  (c) Multilayer board techniques w/many layers
  (d) Custom front end (eg. preamp) packaging
  (e) Modular packaging standards (eg. FASTBUS)
  (f) Mass termination techniques
  (g) Fiber optics signal transmission

Developments in integrated circuit technology for commercial and government/military applications over the past 1-2 decades have stimulated this impressive arsenal of technology. A relatively few years ago, many of these techniques were inaccessible or prohibitively expensive to the relatively small High Energy Physics community. However, two factors have combined to put most if not all of these techniques within reach. One is that increased automation and simplification of customized semiconductor, hybrid and multilayer board technologies has greatly reduced the cost of custom fabrication. Secondly, the larger sizes of physics detectors have driven up the quantities of electronics required by roughly an order of magnitude. The combination of more manufacturers catering to small customers for specialized chip, hybrid and related needs, and increased demand by the physics community, appears to have enabled the community to cross a new threshold of economic feasibility.

Table I
Prototype Design Cycle Involving
Custom Chip, Hybrid and Multilayer PC Board

Conceptual Design (User)	Conceptual Data Acq. Module Design (User)
Detailed Spec. (User)	Detailed Module Spec. (User)
Detailed Chip Design (Contract)	Detailed Module Design (User)
Circuit Stimulation (User or Contract)	Multilayer PC Design (User)
Fabricate Masks (Contract)	Films/Drill Tape (Vendor/User)
Wafer Fab and Test (Contract)	Fab/Load Prototype Multilayer (User)
Dice and Pkg Test Units (User)	Design Test Hardware/Software (User)
Design Hybrid Package (User)	Test Prototype Module(s) (User)
Fab/Test Hybrids (Vendor)	

Table II
Production Cycle Involving
Custom Chip, Hybrid and Multilayer PC Design

CHIP	HYBRID	BOARD
Bid Pkg Prototype Wafers	Bid Pkg Prototype Hybrids	
Award	Award	
Convert Mask Format (Vendor)	Design Hybrid Circuit (User Pref.)	
Production Quality Masks (Vendor)	Fabricate Prototype Substrates (Vendor)	
Fabricate Prototype Wafers (Vendor)		
Wafer Test (User)		
	Assemble Hybrids (Vendor)	
		Prototype Multilayer Boards (User)
		Test/Rework (User)
Production Quantity Wafers (Vendor)	Production Hybrid Quantities (Vendor)	
Specify/Test Proc. (Vendor)		
	Assemble Quantity Hybrids (Vendor)	
		Production Board Fab. (Vendor)
		Production Board Test (Vendor or User)

4. Example Design Project

A few of the current trends and techniques will be illustrated by use of one example design involving a custom chip, hybrid package, and finished multilayer board module. The techniques currently in place at SLAC would follow the flow chart of Table I for the prototype design, and Table II for the production phase.

The basic philosophy is to use outside vendor or contract support for the chip and hybrid prototype and production phases and for the multilayer board production phase. However, the in-house capabilities have been structured to support design of multilayers and rapid fabrication of initial boards for test. The tools required are a centralized CAD system, multilayer lamination press, board fabrication capability to production standards, and automated drill. The CAD system has also recently been used to design multilayer hybrid circuits. These tools are illustrated in Figs. 3,4 and 5. Having an in-house prototype board capability is important to minimize extra queue time at commercial vendors during development and rework phases.

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Fig. 3. CAE/CAD/CAM system

Note that participation of the user in all design phases (chip, hybrid and board) gives the optimum ability to achieve favorable vendor pricing and delivery via the bid process. Also, since large sums are involved, particularly in chip manufacturing, government procurement procedures are much smoother if bids can be tendered to multiple vendors.

In board manufacturing, it is sometimes possible to contract for board testing, particularly if a vendor wishes to provide the product in future as part of a standard catalog product line. However, our recent experience has been somewhat unsatisfactory, primarily due to some vendor's inability or unwillingness to invest in the appropriate test gear and training. This problem increases with the complexity of the design.

Some of the processes involved in this example will now be described.

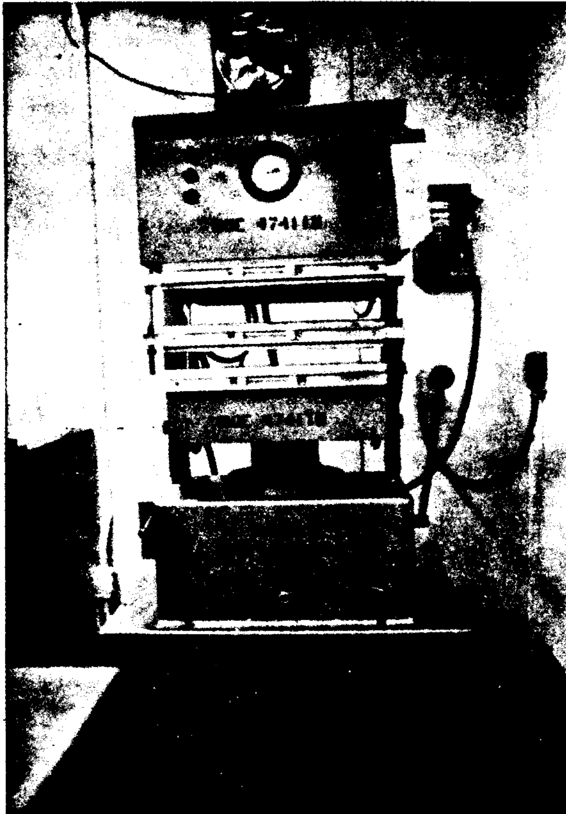

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Fig. 4. Multilayer PC lamination press.

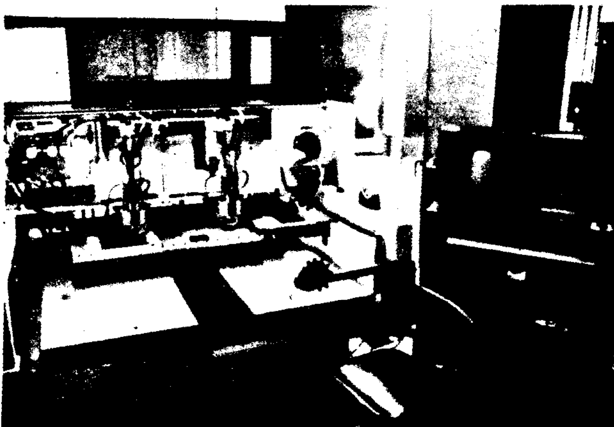

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Fig. 5. PC board NC Drill

5. Custom Chip Design

Many vendors now offer full custom chip design services. For high energy physics users, unless a design has utility in a much wider market, vendor costs could be discouraging (eg, \$ 100*K* for the design ~~and~~ fabrication of a few prototypes). However, the marketplace is rapidly becoming more competitive, and design costs should reduce as techniques and cell libraries become more readily available.

SLAC enjoys the luxury of a contractual relationship with the Stanford Electronics Laboratories, whereby sufficiently novel chip design projects can be undertaken by Senior Research engineers supervising graduate students. These projects form the basis of graduate theses for the students, so SLAC in effect pays for a Research Assistantship and some supervisory and computer time. The design system is shown in Fig. 6; a microphotograph of a typical chip with 3μ minimum feature size is shown in Fig. 7. This particular chip is discussed in detail in two other papers at this Conference (1,2).

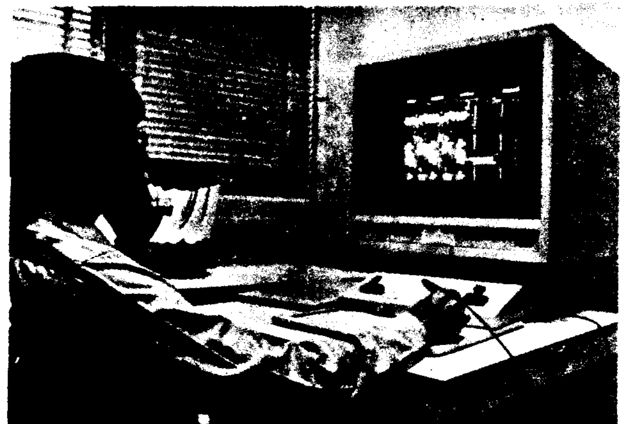

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Fig. 6. VLSI design workstation.

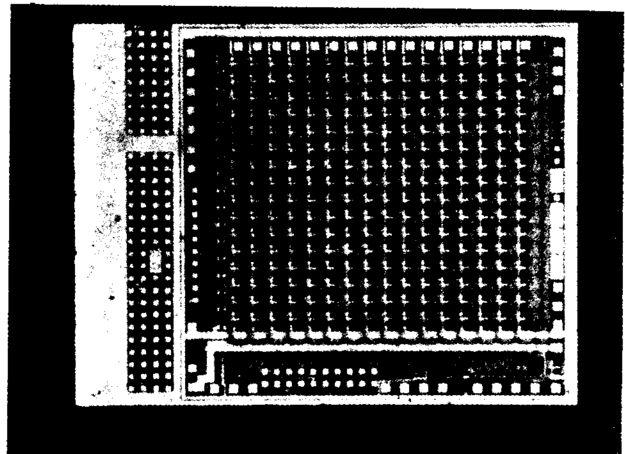

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Fig. 7. VLSI chip detail.

One gap in our current capabilities is that more mundane designs which nevertheless may be of great significance to a particular applications goal, are not of interest to the University as research projects; for such designs, we must either go to a vendor or find another way to perform the design. One future option is to purchase a third party standard cell software package and perform our own designs on our existing CAD system. This is quite feasible, since a single project would justify the cost of the software, and since several of our younger engineers have learned chip design as part of their engineering curricula. There are multiple sources for mask-making, tape conversion and wafer fabrication, such that total costs can be significantly reduced. This is a rather critical issue when one considers that some designs will not be successful, and typically some rework is expected.

6. Custom Chip Production and Testing

Provided quantities are reasonably large (high thousands or 10's of thousands), custom chip fabrication costs at "silicon foundries" are very reasonable. Chip testing will add a small premium; however, for a small non-recurrent engineering charge (NRE), silicon foundries will develop a test program per customer specifications to be run on automated testers which can perform both analog and digital testing. Unusual test requirements will require support from the user in terms of development of special hardware and/or software. Also, masks made at a prototype facility such as Stanford have to be re-made to higher quality at the vendor; this comprises part of the NRE charge.

Once masks are available in the vendor's format and checked by the user, actual silicon fabrication is very rapid, typically 6-8 weeks. One-shot production runs, or continuous runs in the thousands of devices per week, are equally possible. Devices can be sampled or 100% tested by the vendor.

7. Hybrid Circuit Design, Production and Testing

The design of hybrids is equivalent to a multilayer printed circuit design performed to the vendor's design rules and under his supervision. Final designs are approved prior to film fabrication. The advantages of the user retaining the design are that rework is simpler, and multiple bids can be solicited at the production stage, within limitations of the vendor's design capabilities. An example of a finished product was shown in Fig. 2.

Production is greatly facilitated by the automation of placement, bonding, laser trimming of resistors, and chip testing. In most cases, the user will have to assist with any special test fixtures or programs. For hybrid circuits which can be handled by automated means in quantities of 5000 or more, pricing is only slightly higher than the equivalent discrete circuit, while packaging, reliability and maintenance advantages are enormous. An obvious disadvantage is that chips must be thrown away when they fail; thus it is not wise to make the devices excessively large or expensive. In some cases, devices can be structured so as to be repairable, and for an expensive module, this should be kept in mind.

8. Multilayer Board Design, Fabrication and Testing

Multilayer boards are designed on the CAD system shown in the block diagram of Fig. 8. This is a distributed system using a central VAX 780 which supports, in addition to electronics, mechanical, architectural and electrical wiring design; and provides manufacturing support for NC tool path generation, pc drill tapes, and board photoplot outputs. The system does not at this time support circuit simulation software; this is currently performed on SLAC's central IBM facility.

The CAD system was purchased with the option of linking to the central facility. This is now possible through Ethernet, which is in wide use at SLAC, but the CAD system link has not yet been implemented.

The CAD system has three types of workstations: a full-power, dual 19" screen (1 color, 1 monochrome) 1280 x 1020 pixel resolution unit with local processor and memory; a similar device except with a single monochrome or color 19" screen; and a "low cost" device, with local hard and floppy disks, UNIX software, Ethernet link to the VAX, and MSDOS (IBM PC) compatibility. The latter is new and under evaluation as an engineering desk-top workstation. The 15" color screen has 680 x 480 pixel resolution.

This system has been built up over the past 1 1/2 years and is just beginning to reach full efficiency. In the Electronics Department, the system is used for much of the schematic and pc production work, limited mainly by the number of work stations and by our limited ability to support shift operations. Besides the problems of managing a new method of archiving drawings and designs, a major retraining of designers and draftspeople has been necessary.

One of the current goals is to place more (low cost) workstations in the hands of engineers to facilitate circuit simulation and prototype design. Also, if the engineers take over the task of entering initial schematics into the system, and perhaps sections of prototype artwork, some of the traditional documentation bottlenecks will hopefully be minimised.

Design consists of schematic entry, followed by netlist generation, IC placement, automatic routing, and manual editing and cleanup. Once completed, checkplots are generated for the design engineer. One of the failings of our system is that mistakes can be made such that check plots still need to be manually checked for accuracy, a time-consuming job which in future it is hoped will become unnecessary with expected improvements automatic in Design Rule Checking (DRC).

Once checkplots are approved, films are generated by a contract vendor, and typically two multilayer boards are built, with one loaded for test. Testing may be aided by specialized test jigs which are designed in advance. A typical test setup is shown in Fig. 9; this involves a microcomputer tester, special test jigs, and standard modular hardware, display, and test equipment such as oscilloscopes. SLAC has, to date, standardized on an LSI-11 test system utilizing FORTH as a test language; approximately 50 systems are in use around the Laboratory, primarily for use in testing. More recently, a MicroVAX has been implemented as a Multibus/CAMAC/FASTBUS test station; this device may become our future standard, especially for FASTBUS test stations.

The pre-production prototype is completed in every detail prior to bidding for vendor fabrication. Usually, rework of the first units is necessary; if the rework is minor, new films are generated and the job proceeds to production; if major, the boards may have to be rebuilt and re-tested. The circuit itself, test jig, and test software, are thoroughly documented at this time.

9. Automated Testing

At the present time, the foregoing test systems represent the limit of our capabilities–that is to say, computer test stands, augmented by standard test gear such as oscilloscopes and logic analyzers, and by custom test modules designed to test specific devices.

Industry has spurred the development of sophisticated chip and board testers. The most up-to-date board testers use a "bed-of-nails" probe system which can apply analog and digital test signals to selected points, in order to make bare board as well as in-circuit dynamic tests. Board and circuit descriptions can be downloaded from the CAD design files for direct testing; custom test routines are generated from on-line computer terminals.

At the present time, the cost of such machines capable of handling very large boards (eg. FASTBUS) is very high,

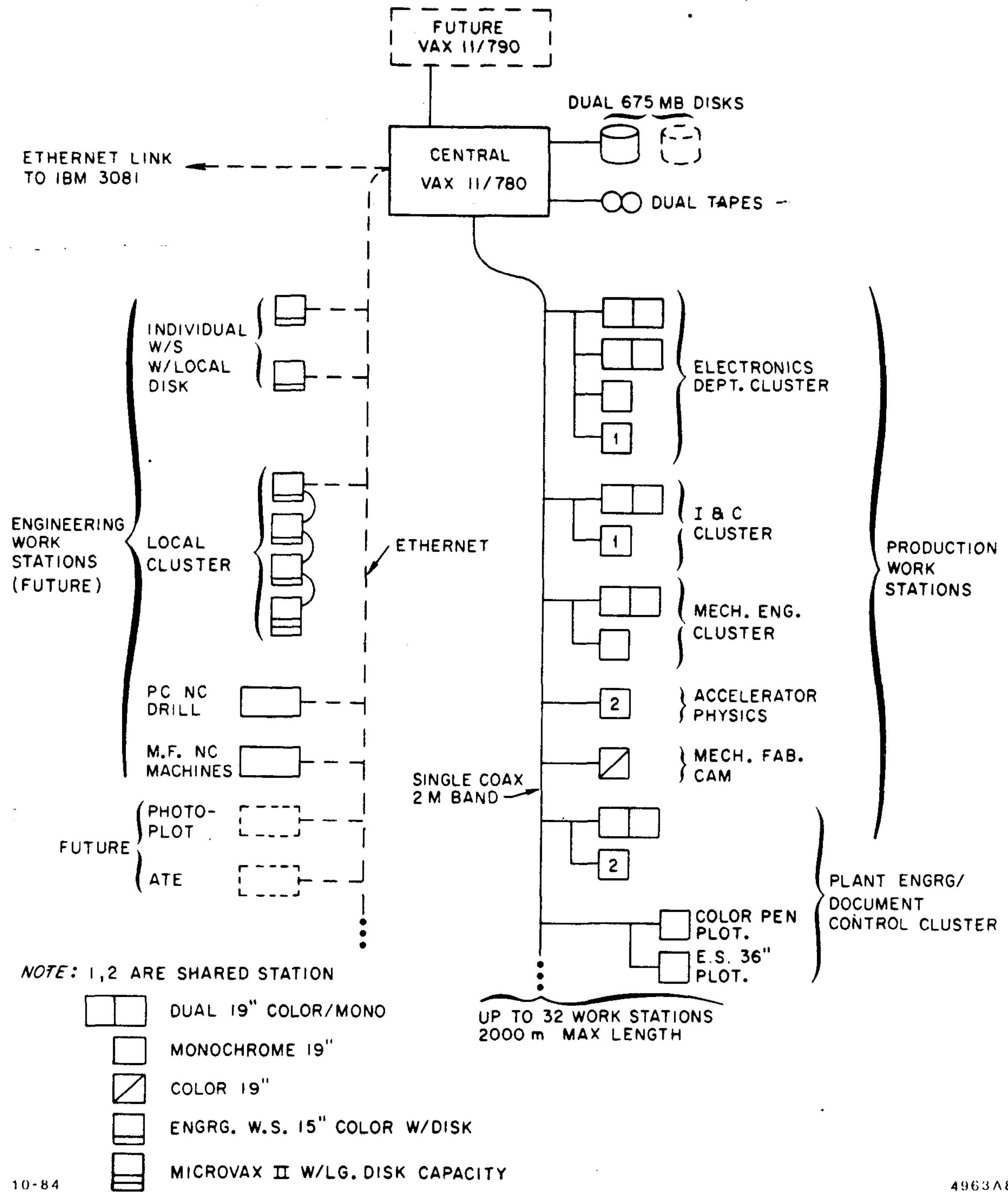

Fig. 8. SLAC CAE/CAD/CAM Architecture.

(~ $ 350K); and the cost of custom jigs, templates and software makes the technique costly for small production runs. However, for large runs, and for boards which can be easily stripped of mounting hardware, the system can also perform both incoming inspection and maintenance testing, which may be especially valuable for ultra-sophisticated modules containing complex processors and control logic. As these test systems develop further, costs can be expected to come within reach of the laboratories.

Fig. 9. Engineering μP test station.

10. Future Trends

The foregoing example gives a hint that for maximum effectiveness, it is desirable to integrate or network as many of these design and manufacturing tools as possible. The flow of work shown in Fig. 10 can theoretically be accomplished on a common system. The potential advantages are that the data pertinent to a given tasks does not have to be re-created or retranslated manually, thus avoiding mistakes and inconsistencies; and that laborious manual checking can be avoided. There is the further long-range ideal that if all the laboratory's design documentation, including textual information, can be documented in a common relational data base, then all logically connected documents can be cross-indexed and, in the ultimate, updated automatically when a revision is made to just one of the related documents. Although vendors currently advertise such capabilities, in reality they are a long way from being realized, and the software overheads in such systems in practice may be prohibitive.

Another important problem in converting to CAD documentation, is that of translating existing drawings into the system. In the ultimate, this is necessary, or true conversion to a CAD data base will never be accomplished. Obviously, some reasonable choices must be made, as it is impractical and unproductive to convert all of the old information. It is much more important to collect as much as possible of the *new* design information in this manner.

There are two basic ways to enter old drawings into the system. The first is the painful method of simply copying the drawing into the new system; this will take far less time than the original, but still will be a boring and costly exercise. A second method is to use a semi-automatic approach, in which the drawing is first scanned by a special camera, and then edited online by an operator to make sure it is translated properly. Such systems can reduce the workload of drawing conversion by about a factor of X5; however, like ATE, the systems are expensive, in the $ 350K range. SLAC is researching this matter, but has made no definite commitments to date.

Two other important tools should be mentioned. One is CAD software and peripheral hardware which can aid the construction of engineering documents, combining text editing with graphics data from the CAD files. The graphics data can be pulled from existing archives, or created on-line by the graphics artist. At present, all such graphics work at SLAC is performed manually; in future, with photographic quality 2D and 3D color graphics available directly from the CAD system, a more direct linkage seems inevitable.

The second tool comprises firmware programming software and hardware, and an engineering document archival system which links this information to the final documentation package. Currently, the system developed by the SLAC Electronics Department develops and archives this information on the central IBM 3081 facility, but establishes linkage to Document Control through special codes in the document material list (ML) which flag Document Control to order this information via computer link to the IBM whenever a user requests a copy of the particular document package to which it pertains. (A paper on some of these firmware capabilities is presented at this symposium; see Ref. 3).

11. Modular Standards

As has already been pointed out, modular standards have played a central role in the successful development of large-scale detector systems. The newest standard, FASTBUS, shown in Fig. 11, has been structured to encompass extremely complex pre-processing, as well as relatively simple front-end modules. In practice, the availability of custom chip technologies may result in more circuitry migrating into front-end circuits, closer to the detector elements, while the data conversion, memory and preprocessing elements remain housed in the traditional modules.

12. Human Factors

We have described the emerging capabilities for electronics design, production, testing and documentation, some of which are just recently coming within economic reach of the high energy physics communities. These tools are necessary because the remarkable advances in electronics have brought with them considerable increases in complexity, including very high density complex circuitry, precision fabrication requirements, and the necessity for some level of automated testing. Increasingly, reliance is being made upon software and firmware to replace custom hardware, both in circuit design and in testing. Thus

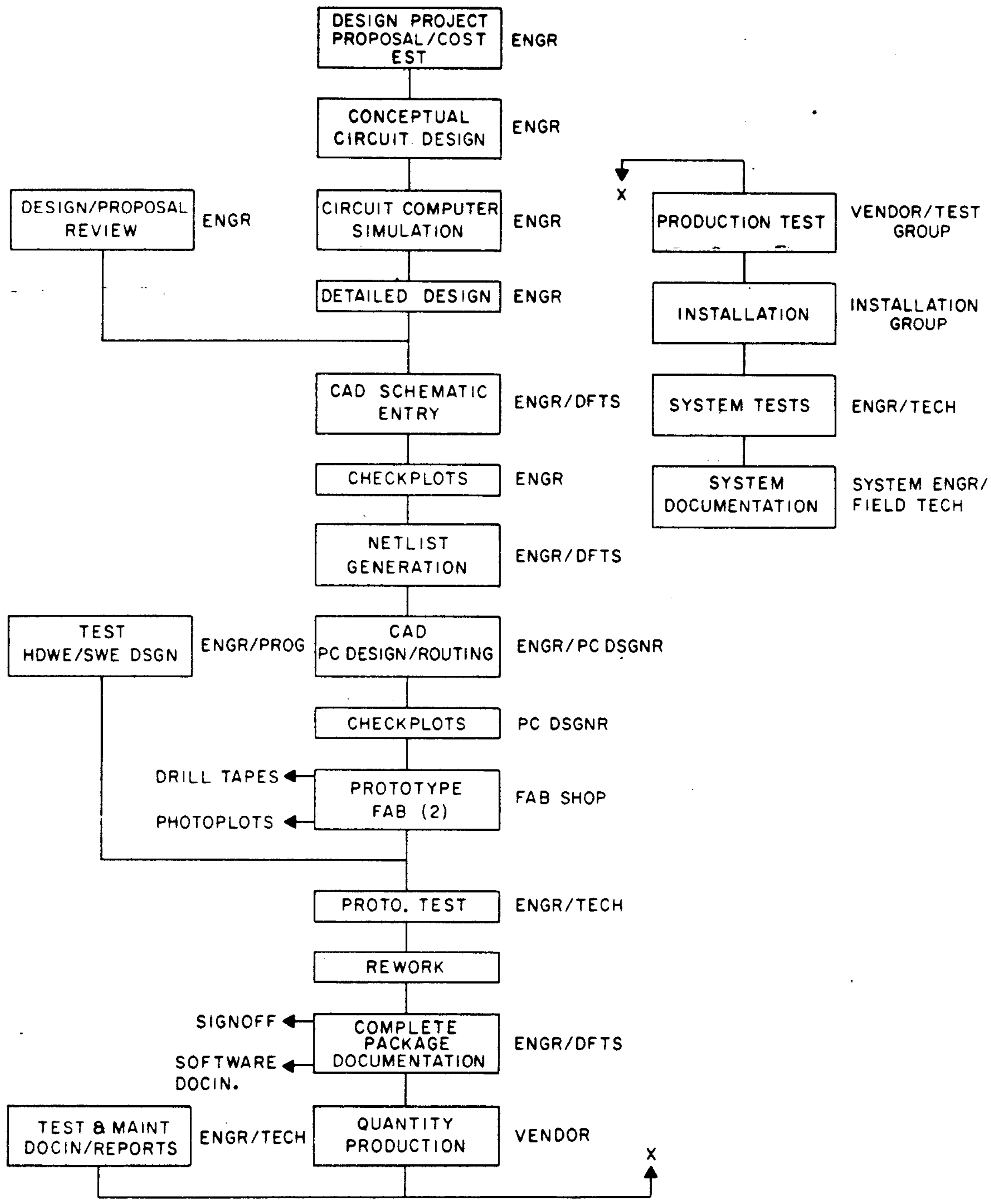

Fig. 10. Electronics design, manufacturing and documentation work flow diagram.

the engineer, support technician, draftspeople, board designers, fabricators, and maintenance personnel, are all required to increase their skills significantly to cope with the new demands and the tools which support them.

Fig. 11. FASTBUS modular standard.

Our recent CAD conversion experience has been relatively successful; however, it has also pointed out that while highly skilled R & D engineers can rather easily acquire the new skills, many technicians, draftspeople, and designers on the average have considerably more difficulty. Some, in fact, for various reasons, including poor system documentation and "unfriendliness," find the new techniques very difficult to learn, and their productively actually remains lower than using manual methods for much longer than one would expect.

At this juncture, management is faced with the necessity of making a continuing strong commitment for retraining technical support people. Furthermore, designers of CAD systems must continue to improve their products to make them easier to learn. In the great rush of new vendors into the CAD market, many offerings, including the SLAC system, leave much to be desired in this area of "user friendless." We not only hope for, but are committed to working toward improvements; and as we become more knowledgeable users, to learn how to specify, measure, and demand performance from the vendors for future acquisitions.

Hopefully, among our exciting design activities and ambitious schedules, we will remember the over-riding importance of the human equation; and hopefully in this arena also we can strive for excellence.

13. Conclusion

Many new electronics design technologies are now economically viable for the field of High Energy Physics. The principal result in the next decade should be the realization of order-of-magnitude larger systems at significantly reduced per-channel costs and improved per-channel reliability. Improvements in speed and overall precision of data acquisition should also continue to improve. To achieve these goals, new tools are needed for chip, hybrid, circuit and system design; for manufacturing, test and maintenance; and for documentation. Laboratories will need to carefully develop integrated data-base systems which facilitate smooth work flow and smooth technological transitions; in particular, attention must be paid to the difficult problems of re-training of skilled people into new skills which will enhance, rather than diminish, their overall capabilities and intellect.

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